



† fat plate has parasitics to ground
 * low noise, low parasitic resistance
 o low capacitance
 □ diode clamps on these pads
 Orbit/MOSIS process, 3μ, 2 poly, 2 metal.
 p well, N igfet.
 n wafer. to V+, all p igfet bulk to V+, all n igfet to gnd, unless noted
 W = 25μ is a flag to use a donut gate igfet with small capacitance drain
 all nodes have 2nd metal dot, for probing, unless noted

CHG	DRWN	BY	DATE	CHANGES	DEL	TO	DRWN	BY	DATE	SCALE	APPR	DATE	SCALE	REVISION
	M			63.9 + 118 = 370							15 May '90			Rev. D
	Q			6										
	I			4(7) + 16 + 1 = 30										
	P/ch			6 * 0.030 / 4 = 45mW										
	LAWRENCE BERKELEY LABORATORY UNIVERSITY OF CALIFORNIA													