48 Channel Stretcher in a single width NIM unit.

Specifications

1- Performance

Linear Input Amplitude:	-5mV to -8V, linear range.
Minimum Input Shaping Time:	500ns.
Gain: .	unity.
Integral Nonlinearirty:	± 0,1%.
Cross-talk:	0.1% max.

2 - Inputs

Linear Input:	negative polarity. -10V max. impedance ≈ 1000Ω.
Gate Input:	common for all channels. standard NIM logic (Gate ON = 0V). a valid gate pulse must be 300ns before peak.
Reset Input:	common for all channels. standard NIM logic (Reset ON = -0.8V) . 1μs minimum width.

3 - Power Requirements

+12	450mA.
-12	180mA.
+ 6	20mA.

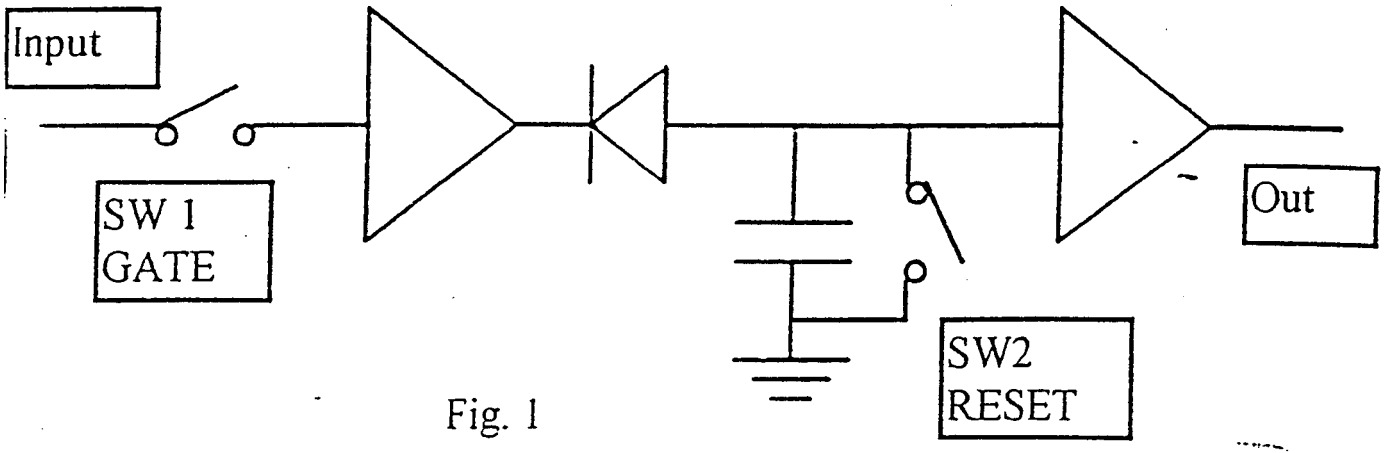


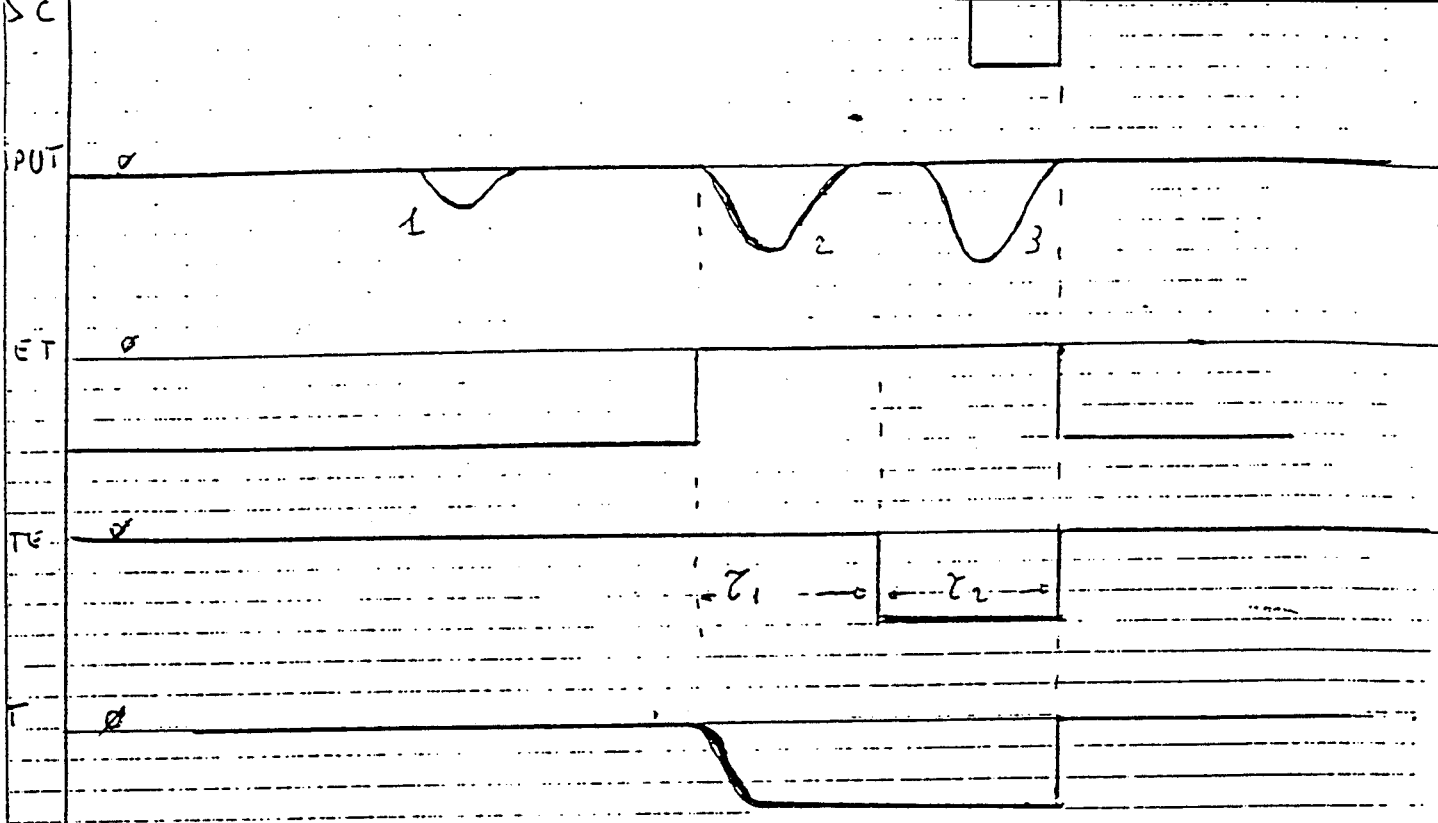
Fig. 1

- the GATE signal controls the switch SW1. It is a NIM signal with 50 Ω.
If the GATE signal is at 0 V --> SW1 = ON (closed)
If the GATE signal is at - -0.8 V --> SW1 = OFF (open)
In the open state the output of the stretcher goes at +2V; these shouldn't be a problem for the QDC because it has a clamping diode and the output of the stretcher has a series resistance that limits the maximum current.

- the RESET signal controls the switch SW2. It is a NIM signal with 50 Ω.
If the RESET signal is at 0 V --> SW2 = OFF (reset is not active)
If the RESET signal is at - -0.8 V --> SW2 = ON (reset is active)
The stretcher keeps the peak of the negative input signal when the GATE is ON and the RESET is OFF.

We suggest you to handle the module as showed in fig. 2.

- Hold the GATE ON (0 V) and the RESET ON (-0.8 V)
- Set the RESET signal in the OFF position (0 V) when you want to begin the time interval in which the signals are accepted.
- When the GATE goes OFF (-0.8 V) the time interval in which the signals are accepted expires and the signals are stretched.
- During the time in which both GATE and RESET are in the OFF state the data are ready to be collected sending a gate to the QDC.
- When the gate function of the QDC is ended, simultaneously set the GATE and the RESET signal in the previous states, GATE ON (0 V) and RESET ON (-0.8 V)



τ_1 = Time interval in which signals are accepted and stretched

τ_2 = Time in which the stretched signals are ready to be converted by the GATE of ADCs

Signal 1 and 3 = rejected

FIG 2