Revision			
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-	Original Release		

See the last page for a revision history

	Name	Title	Date			
Originator	D Conell					
Approved						
Approved				Register Description Document		
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BiRa Systems, Inc.

VME 16 BIT NIM OUTPUT REGISTER

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1 Description of Board

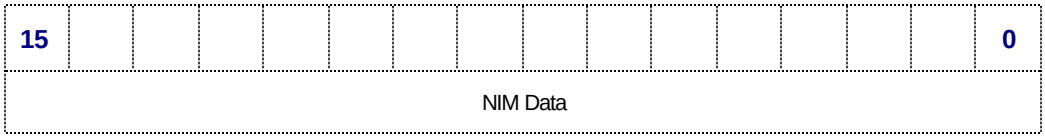
The board provides 16 NIM outputs on a 6U VME module. The output may either be level or strobed. The width of the strobe is adjustable through program IO. The module appears as a 64-byte block in the A16 VME address space. The setting of this block within the A16 space is controlled by dip switch settings. The module performs 16-bit (D16) transfers exclusively. Four registers control the module and are described below.

Terminators are required to produce a true output, 0.8 to -1.2Vdc is a false output and 0.0Vdc is true.

1.1 NIM Data Register

This register selects whether an individual output is true or false. A one sets the output 'true' and a zero results in a 'false' output. This is a read-write register.

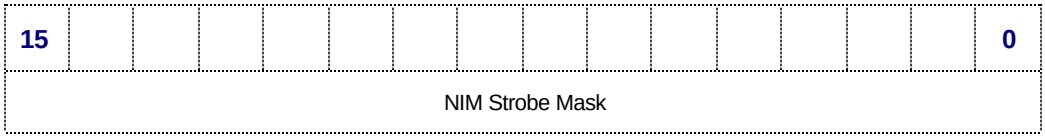
Base Address + 0x0



1.2 NIM Strobe Mask Register

This register selects whether an individual output is a strobed or level output. When high, a bit is a strobed type output, if the bit is TRUE in the data register. This is a read-write register.

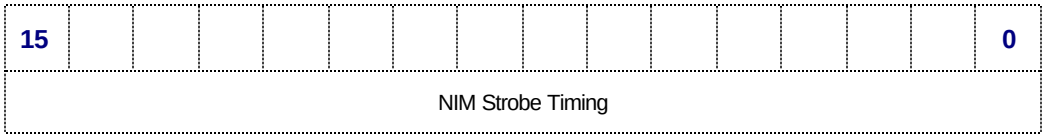
Base Address + 0x2



1.3 NIM Strobe Timing Register

This register selects the global timing of the strobe. When the timing bit (T) of the control register is low, the bit weight of the register is 62.5nS, and full scale is 4096uS. When the timing bit of the control register is high, the bit weight of the register is 4096uS, and full scale is 268.43136 Sec. This is a read-write register.

Base Address + 0x4



1.4 NIM Control Status Register

This register controls the transfer of the NIM data register contents to the NIM outputs. Data is transferred when the control bit (C) is set. The module is ready for new activity when the status bit (S) reads zero. This is a read-write register.

Base Address + 0x6

15														1	0
Reserved														T	C/S