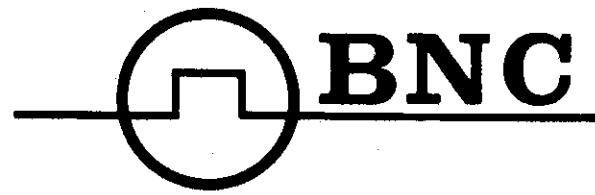


Ramp Generator

Model LG-1

INSTRUCTION MANUAL

BERKELEY NUCLEONICS CORPORATION
1198 Tenth St., Berkeley, California 94710

INDEX

Warranty

Berkeley Nucleonics Corporation warrants all instruments, including component parts, to be free from defects in material and workmanship, under normal use and service for a period of one year. If repairs are required during the warranty period, contact the factory for component replacement or shipping instructions. Include serial number of the instrument. This warranty is void if the unit is repaired or altered by others than those authorized by the Berkeley Nucleonics Corporation.

SPECIFICATIONS

OUTPUT WAVEFORM: Triangular waveform.

AMPLITUDE: 25 mV below the baseline to 11.7 volts above baseline max. Maximum amplitude is adjustable by front panel trimmer from 1 to 11.7 volts. Offset below baseline is adjustable by internal trimmer from 25 mV to 500 mV.

PERIOD: 5 or 50 sec at maximum amplitude of 11.7 volts. Period reduced at smaller amplitude. For other periods consult the factory.

LINEARITY: Integral, better than ±0.01%; Differential, better than ±0.05%, to within 20 mV of turn-around points.

POLARITY: Positive or negative.

OUTPUT IMPEDANCE: 100 ohms.

CONTROL FUNCTIONS:

RESET: Ramp is reset to 25 mV below baseline.

START: Ramp is initiated.

STOP: Ramp terminates at end of cycle.

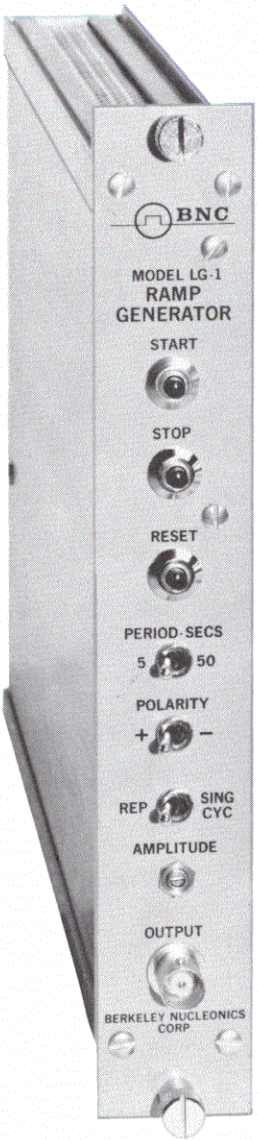
REP/SINGLE CYCLE: Toggle to provide continuous or single cycle ramp.

MAX. OPERATING TEMPERATURE: 55°C.

POWER REQUIREMENTS: +24V at 90 mA, -24V at 75 mA.

MECHANICAL SPECIFICATIONS: Single width AEC module, 1.35" wide, 8.70" high. Conforms to AEC Report TID-20893.

WEIGHT: 2 lbs. net, Shipping 8 lbs.



OPERATING INSTRUCTIONS

SECTION 2

2.1 INTRODUCTION

The Model LG-1 Ramp Generator provides a triangular waveform with a differential linearity better than ± 0.1%. A major application of the Model LG-1 is as a reference for pulse generators to provide a sliding pulse train (linearly increasing and decreasing amplitude pulses). The Berkeley Nucleonics Models BH-1 BL-2, DB-2, PB-3, PB-4, and 9010 may be directly connected to the Model LG-1 via external reference jacks.

Mercury-relay pulse generators may also be used with the Model LG-1 to provide a sliding pulse train. Some mercury-relay pulse generators have external reference connectors, while others may be modified to provide an external reference connector.

2.2 FUNCTION OF CONTROLS

START:	Initiates the ramp cycle.
STOP:	Stops the ramp cycle. The ramp will continue the cycle in progress and stop at the end of the cycle.
RESET:	Resets ramp to preset quiescent voltage where it remains until started.
PERIOD:	Toggle to provide either 5 sec or 50 sec at maximum amplitude of 11.7V. Period is reduced at smaller amplitudes.
POLARITY:	Selects output polarity of ramp.
AMPLITUDE:	Front panel trimmer adjusts the maximum amplitude of the ramp from 1 to 11.7V.
OUTPUT CONNECTOR:	The output waveform appears at both the front and back panel output connectors.

2.3 OPERATION AS A SLIDING PULSE GENERATOR

The Model LG-1 has many applications where an extremely linear ramp is required. One major application is as a reference for a pulse generator to provide a sliding pulse train. The sliding pulse train is used to measure differential linearity of pulse height analyzers. This mode of operation with the Model LG-1 is described as follows:

1. Connect the ramp output to the reference input of the pulse generator. Connect the output of the pulse generator to the input of the pulse height analyzer (PHA).

2. Adjust the pulse shape and repetition rate of the pulse generator. Maximum repetition rate is limited by the dead time of the PHA.

3. Erase the storage in the PHA and set it in the STORE mode.

4. Press the START button on the Model LG-1 and observe the highest channel receiving counts. Adjust the amplitude of the sliding pulse train so that the maximum pulses fall beyond the highest channels. Adjustment may be made either by varying the AMPLITUDE controls on the pulse generator or on the Model LG-1.

5. Set the desired ramp speed (5 or 50 secs). Erase the PHA memory and reset the Model LG-1.

6. Set the REP-SING CYC switch to SING CYC for one cycle or to REP for repetitive sweeps.

7. Press the START button of the Model LG-1 and accumulation of counts in the PHA will begin.

8. When sufficient counts have been accumulated for statistical accuracy desired, press the STOP button on the Model LG-1. The ramp cycle will stop at the next zero crossing of the ramp. If the analyzer is linear, an equal number of counts will be stored in each channel and the display will be a straight line. Deviation from the straight line is an indication of differential nonlinearity.

The differential nonlinearity (DNL) of the analyzer may then be computed by:

$$DNL = 100 \left[1 - \frac{N_x}{N_{(av)}} \right] \%$$

where N_x = number of counts in channel x

$N_{(av)}$ = average number of counts in all channels

N_x is generally taken as the worst case deviation from the average. In some cases one channel address may be defective and it is not included in the measurement.

3.1 CIRCUITRY

Refer to Block Diagram Fig. 2 and Schematic LG-102.

The RAMP GENERATOR is an operational amplifier, Q35-Q39, Q41, Q42, and Q44 connected as an integrator. A constant current from R97 and R103 is applied to the input of the integrator, the gate of Q35. Integration of this constant current produces a signal with a constant rate of change (a ramp) at the output of the operational amplifier. The rate of change of this signal is determined by the integrator input current and the value of the integrating capacitor according to the relation CE = -IT, where C is the capacitance in Farads, E is the output in Volts, I is the input current in Amperes and T is the time in Seconds. The input current is determined by the algebraic sum of the currents in R97 and R103. The capacitance is determined by the selection of C33, C34 or C35 with S1-1.

Operation of the amplifier is as follows: Q35 and Q36 are FET's arranged as a differential amplifier for reduction of common mode effects. Trimmer R115, which is connected to the gate of Q36 via R114, provides an adjustment for zero volts at the amplifier input. (An adjustment for zero is necessary since a voltage offset at the input will produce a current in R107, which added to the currents in R97 and R103 will affect the ramp rates.)

Diodes D40 and D41 limit the positive swing of the sources of Q35 and Q36. This is necessary to avoid a possible reversal of amplification polarity in Q35-Q37 during positive overload conditions. Polarity reversal could occur if there were not a low impedance path from the drain of Q35 to ground when Q35 saturates. The signal on the gate of Q35 would pass uninverted directly to its drain, thereby changing the polarity of the overall gain of the amplifier from negative to positive. A lockup condition would then occur.

The drains of Q35 and Q36 are directly coupled to the bases of Q37 and Q38, also connected as a differential amplifier. The bases of Q37 and Q38 normally operate at about +5 volts. The signal from the collector of Q37 is then coupled to the base of Q39, which is operating with its emitter connected to -15 V. Up to the base of

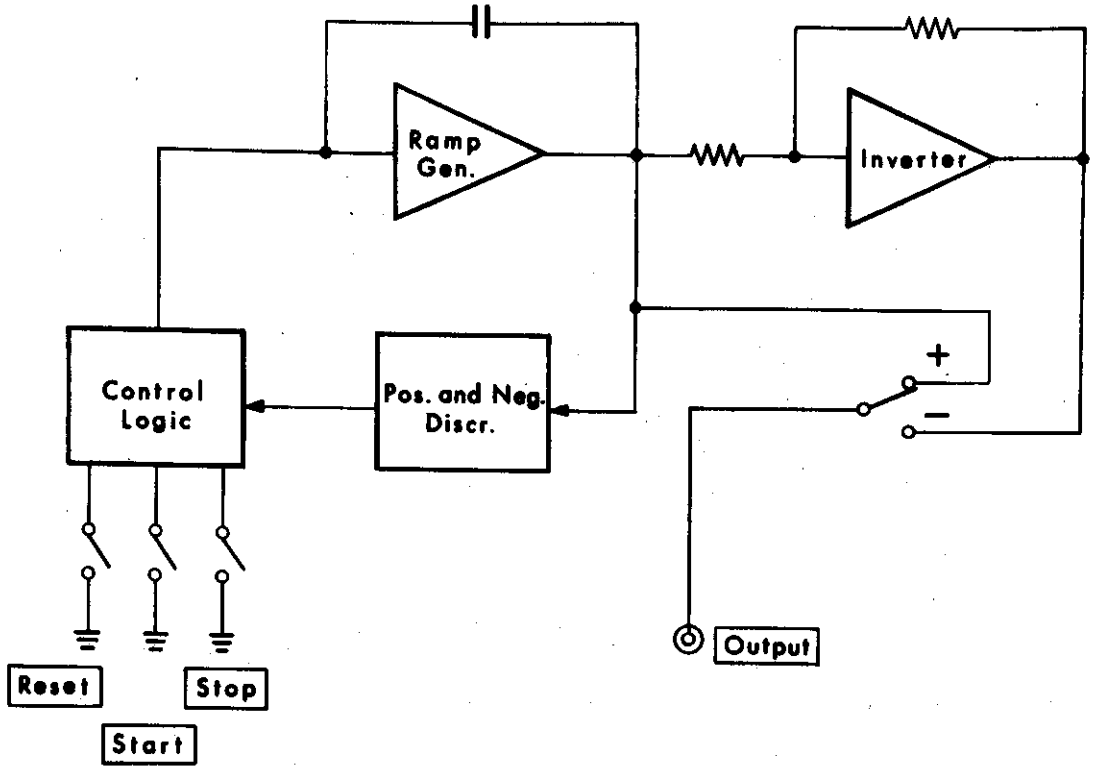


Fig. 2. Block diagram of the Model LG-1.

Q39 the amplifier operates in the current mode, with voltage swings in the millivolt or less region. Q39 provides the voltage gain for the amplifier and drives the output emitter followers Q41 and Q42. Q44 is connected as a current source for the collector of Q39. The current in Q44 is determined by R118 at its emitter. The constant voltage of 9 V across R118 produces a constant current of 2.7 mA in Q44. The 2.7 mA current in Q44 produces a drop of 1.5 V across R117, ensuring that both Q41 and Q42 are turned on at all times. R120 limits the current between the emitters of Q41 and Q42. Q40 and Q43 provide the +15 V and -15 V power supplies for the ramp and inverter output circuits. C37 stabilizes the amplifier over its operating range.

The INVERTER is an operational amplifier, Q45-Q52, connected as a unity gain inverter. Operation of the inverter amplifier is similar to the ramp generator amplifier. Q45 and Q46 are connected as the input differential amplifier, driving Q47 and Q48, also connected as a differential amplifier. C40 operates to stabilize the amplifier. Q47 drives Q49, which provides the voltage gain. Q50 provides a constant current to the collector of Q49. Q51 and Q52 are the output emitter followers, and C41 operates to stabilize the amplifier. The input and feedback resistors for the unity inverter are R122 and R123, respectively.

The POSITIVE DISCRIMINATOR, Q27 and Q28, senses when the positive ramp level from the ramp generator exceeds a preset value. The preset level is set at the junction of R86 and R87 by adjusting R85. When the ramp level at the anode of D26 is below the preset voltage, this diode is cut off, causing R81 to pull the base of Q27 negative. The base of Q27 is clamped by D27 at a level about 0.5 V more negative than its emitter, cutting off Q27. Q28 is conducting, its base held by D29 at a level about 0.5 V below the preset voltage. When the ramp level at the anode of D26 reaches the preset voltage at the anode of D29, Q27 begins to conduct, since the drops across D26 and D29 are equal. When Q27 conducts, its collector goes negative, pulling the base of Q26 negative through R80. Q26 then conducts, providing the drive for one of the control logic functions and thereby reversing the ramp direction.

The NEGATIVE DISCRIMINATOR, Q33 and Q34, senses when the positive ramp level becomes more negative than a preset level. Additionally, Q33 and Q34 establish the quiescent ramp level in the reset condition. Operation of the negative discriminator is as follows: The preset discrimination level is set by R99 to a point between zero and -1 V. This level is applied to the base of Q33, arranged with Q34 as a differential amplifier. When the positive ramp level, sensed by the base of Q34 through R106, is more positive than the discrimination level Q34 is turned on. D39 limits the positive base swing of Q34 to about +0.5 V. When all the current in emitter resistor R105 is passing through Q34, Q34 is saturated. Due to the opposite voltage drops across D39 and the base-emitter junction of Q34, the emitter of Q34 is at about zero volts. The collector level of Q34 will then not exceed +0.5 V under any condition. The collector of Q34 is connected through diode D32 to the base of Q31. Since the voltage on the collector of Q34 must exceed about +1 V in order to turn on Q31 through D32, Q31 is turned off. This establishes a logic level at Q22 for controlling the ramp, as is discussed in the next paragraph.

With all the current from R105 flowing into Q34, Q33 is cut off. The collector of Q33 is pulled positive through R104 and is clamped at about +0.5 V by D36. Current from the -15 V supply passes through R98 to the junction of D37 and D38, tending to pull the collector of Q33 negative. The algebraic sum of the currents in R98 and R104 is +2.7 mA. Due to the voltage drop across D38, the junction of D37 and D38 is at zero volts, so that no current flows through D37 to the input of the ramp generator (the junction of R107 and R108).

When the ramp level drops to the preset level, Q34 begins to turn off and Q33 begins to turn on. The current in R105 is 3.8 mA (the sum of the emitter currents of Q33 and Q34). When the collector current in Q34 drops to 2 mA, the algebraic sum of the current in R92 and the current from Q34 becomes positive, turning on Q31 through D32. Q31 saturates, establishing a logic level at D23 for controlling the ramp. When the ramp control is in the REP (repetitive) condition, the ramp will immediately reverse direction and go positive, limiting the current transfer from Q34 to Q33 to 1.8 mA (3.8 mA in R105, -2.0 mA in Q34). The algebraic sum of the currents at the collector of Q33 will then be limited to +0.9 mA (+3.7 mA in R104, -1 mA in R98, -1.8 mA in Q33), and D36 will continue to conduct.

Under conditions where ramp reversal does not occur (the STOP button has been pressed, SINGLE CYCLE has been selected, or the ramp is reset) the ramp continues to go negative after Q31 has been turned on by the signal from Q34. Current continues to transfer from Q34 to Q33 until 2.7 mA flows in Q33. At this point the algebraic sum of the currents at the collector of Q33 becomes negative and D36 becomes reverse biased. The collector of Q33 then goes negative, tending to reverse bias D38. Current in-

creases from R98 through D37 into the operational amplifier input until the currents from R98 and R103 algebraically sum to zero. At this point the ramp stops until the logics are switched to allow current from R97 to pass to the operational amplifier input. The voltage at which the ramp stops is the quiescent level of the ramp.

The CONTROL LOGIC consists of the Cycle Bistable, the Ramp Bistable, a Logic Gate and the Ramp Switch. The operation of the logics is as follows: When the START button is pressed, the collector of Q21 in the Cycle Bistable Q20 and Q21 is pulled down to ground. The collector of Q20 rises, and the "run" state of the Cycle Bistable is established. The collector of Q21 pulls the cathode of D21 negative, producing about +0.6 V at the junction of D21 and D22. Due to the drop across D22, there will be no current flow through D22, since the base of Q22 can be only zero or positive. Operation of the gate transistor Q22 is then controlled only by Q31 through D23.

When the positive ramp has operated the Negative Discriminator, Q31 is saturated and its collector goes to approximately ground level. No current flows in D23 and Q22 is cut off, allowing its collector to be pulled positive by R70. The current from R70 then passes through D24 to the base of Q23 in the Ramp Bistable Q23 and Q24, turning on Q23. This establishes the "ramp increase" state of the Ramp Bistable. The collector of Q24 then goes positive and current flows through R77 into the emitter of the grounded base buffer Q25. This current appears at the collector of Q25, which is coupled directly to the base of the Ramp Switch Q32. Q32 saturates, pulling its collector down to its emitter level of -11.7 V. D33 is reverse biased, and -0.94 μA flows through R97 into the operational amplifier input. Since +0.47 μA flows continuously into the operational amplifier input from R103, the algebraic sum of the currents in R97 and R103 is -0.47 μA. This current causes the ramp to increase (the positive ramp becomes more positive). As the ramp increases from the negative discrimination level, Q31 turns off and the current in R68 flows through D23 into the base of Q22. This prevents additional signals from the Cycle Bistable from passing to the Ramp Bistable until the negative discrimination level is again reached.

When the positive ramp increases to the point where the Positive Discriminator operates, Q26 saturates and its collector goes to +24 V. The collector current of Q26 passes through R78 to the base of Q24, turning on Q24. This establishes the "ramp decrease" state of the Ramp Bistable. The collector of Q24 goes negative, cutting off Q25. With no current flowing from Q25, R95 pulls the base of Q32 negative, cutting off Q32. The collector of Q32 goes positive and is clamped at about +0.5 V by D33. The current through R97 is then +0.04 μA. The algebraic sum of the currents in R97 and R103 is +0.51 μA, and the ramp decreases (goes negative).

Pressing the STOP button grounds the collector of Q20, cutting off Q21. The collector of Q21 rises, establishing the "stop" state of the Cycle Bistable. When the collector of Q21 rises, R67 pulls the anodes of D21 and D22 positive until current flows through D22 to the base of Q22. Q22 will saturate until the Cycle Bistable is set to the "run" state. The Ramp Bistable now can not be set to the "ramp increase" state, and at the end of the next decreasing part of the ramp, the ramp will stop at its quiescent level.

When the REP - SINGLE CYCLE switch is in the SINGLE CYCLE position, R60 is connected to +24 V. The current from R60 is applied to the base of Q20, turning on Q20. The Cycle Bistable is held in the "stop" state by this current. Pressing the START button momentarily grounds the collector of Q21, allowing Q22 to cut off. This starts a ramp cycle. When the START button is released, the collector of Q21 rises, preventing the Ramp Bistable from being triggered by the Negative Discriminator.

The RESET GENERATOR consists of two transistors: the Logic Reset Q29 and the Ramp Reset Q30. Operation of the Reset Generator is as follows: Pressing the RESET button discharges C31, placing +24 V on the switch side of R88. The current in R88 is applied to the base of Q29, which saturates. Q29 remains turned on for about 0.4 Sec. after the RESET button is released due to the time constant of C31 and R88. This is to ensure that the ramp timing capacitors C33, C34 or C35 are completely reset. The collector of Q29 goes negative, turning off transistors Q20 and Q24 through diodes D20 and D25, respectively. This resets the logic bistables to the "stop" and "ramp decrease" states. When Q29 is cut off, its collector is pulled positive by R90 and R91 and is clamped at +15.5 V by D30. The level from the collector of Q29 passes through R91 to the base of Q30, cutting off Q30. The collector of Q30 is pulled negative by R101 and is clamped at about -0.5 V by D31. Current passes from +15 V through R102 and D34 to the collector of Q30 and is summed algebraically with the current from R101. The sum of these currents is -1.8 mA (-2.4 mA from R101, +0.6 mA from R102) which passes through D31. The junction of D34 and D35 is at zero volts due to the drop across D34, and no current flows through low leakage diode D35.

During the reset cycle the collector of Q29 goes to about ground, and the algebraic sum of the currents in R90 and R91 is negative at the base of Q30, which saturates. D34 is reverse biased and the current from R102 passes through D35 to the operational amplifier input. The positive current from R102 is much greater than the maximum negative current in R97, causing the ramp to rapidly reset to the quiescent value. The ramp limits at the quiescent level when the algebraic sum of the currents in R97, R98, R103 and Q33 becomes zero.

3.2 ADJUST OPERATIONAL AMPLIFIER ZERO.

a. Connect a 1K resistor across the 1 μF ramp timing capacitor C34. (This capacitor is connected to the PERIOD toggle.) Set the controls as follows:

   PERIOD: 50 secs.
   RESET: Momentarily press the RESET button.
   POLARITY: +

b. Connect a voltmeter or oscilloscope at the OUTPUT connector.

c. Adjust the RAMP ZERO trimmer R115 (see Schematic LG-102 for location) on the circuit board to provide 0 V ±10 mV at the OUTPUT connector.

d. Connect the meter to the test point shown on Schematic LG-102. Adjust the INVERTER ZERO trimmer R131 on the circuit board to provide 0 V ±10 mV at the test point.

3.3 ADJUST NEGATIVE DISCRIMINATOR LEVEL.

a. Connect the OUTPUT to an oscilloscope with a coaxial cable. Do not terminate the cable.

b. Set the Model LG-1 controls as follows:

   PERIOD: 50 secs.
   POLARITY: +

c. Press the START button. Adjust R99, negative discriminator trimmer, so that the turn-around point of the ramp is about 25 mV below the zero level.

d. The negative discriminator may be set to any desired level from about 0 V to 500 mV. The total ramp cycle time will increase as the negative discriminator level increases; the ramp rate of rise is constant for any given setting, so that increasing the ramp voltage swing increases the time for a ramp cycle.

Abbreviations

µH	microhenry	cer	disc ceramic
µF	microfarad	comp	composition carbon
pF	picofarad	dep car	deposited carbon
poly	polystyrene	elec	electrolytic
pot	potentiometer	mic	mica
tan	tantalum	myl	Mylar
V	dc working volts	k	kilohm
W	watts	M	megohm
ww	wirewound	mf	metal film

Capacitors

C30	25 µF	elec	50 V	
C31	5 µF	elec	50 V	
C32	25 µF	elec	50 V	
C33	0.1 µF	poly	50 V	10%
C34	1 µF	poly	50 V	10%
C36	25 µF	elec	50 V	
C37	0.01 µF	cer	1 kV	
C38	0.05 µF	cer	50 V	
C39	25 µF	elec	50 V	
C40	0.001 µF	cer	1 kV	
C41	0.1 µF	myl	100 V	10%
C42	0.05 µF	cer	50 V	
C50	25 µF	elec	50 V	
C51	25 µF	elec	50 V	
C52	0.47 µF	myl	100 V	

Diodes

D20	1N4154
D21	1N4154
D22	1N4154
D23	1N4154
D24	1N4154
D25	1N4154
D26	1N4154
D27	1N4154
D28	1N4154
D29	1N4154
D30	1N4154
D31	1N4154
D32	1N4154
D33	1N4154
D34	1N4154
D35	FJT1100 (Fairchild)
D36	1N4154
D37	FJT1100 (Fairchild)
D38	1N4154
D39	1N4154
D40	1N4154
D41	1N4154
D42	1N4154
D50	1N4154
D51	1N4154
D52	1N4154
D53	1N4154

Resistors

R60	4.7 k	1/2 W	comp	5%
R61	470 ohms	1/2 W	comp	5%
R62	4.7 k	1/2 W	comp	5%
R63	470 ohms	1/2 W	comp	5%
R64	470 ohms	1/2 W	comp	5%
R65	4.7 k	1/2 W	comp	5%
R66	470 ohms	1/2 W	comp	5%
R67	22 k	1/2 W	comp	5%
R68	22 k	1/2 W	comp	5%
R69	10 k	1/2 W	comp	5%
R70	4.7 k	1/2 W	comp	5%
R71	470 ohms	1/2 W	comp	5%
R72	4.7 k	1/2 W	comp	5%
R73	470 ohms	1/2 W	comp	5%
R74	470 ohms	1/2 W	comp	5%
R75	4.7 k	1/2 W	comp	5%
R76	470 ohms	1/2 W	comp	5%
R77	100 k	1/2 W	comp	5%
R78	4.7 k	1/2 W	comp	5%
R79	1 k	1/2 W	comp	5%
R80	1.5 k	1/2 W	comp	5%
R81	47 k	1/2 W	comp	5%
R82	8.2 k	1/2 W	comp	5%
R83	1.5 k	1/2 W	comp	5%
R84	46.4 k	1/2 W	mf	1%
R85	3.57 k	1/2 W	mf	1%
R86	5 k	1 W	trimmer	
R87	422 ohms	1/2 W	mf	1%

Resistors

R88	10 k	1/2 W	comp	5%
R89	10 k	1/2 W	comp	5%
R90	47 k	1/2 W	comp	5%
R91	10 k	1/2 W	comp	5%
R92	6.81 k	1/2 W	mf	1%
R93	10 k	1/2 W	comp	5%
R95	1 M	1/2 W	comp	5%
R96	1 M	1/2 W	comp	5%
R97	95.3 k	1/4 W	mf	1%
R98	15 k	1/2 W	comp	5%
R99	1 k	1 W	trimmer	
R100	10 k	1/2 W	mf	1%
R101	10 k	1/2 W	comp	5%
R102	24 k	1/2 W	comp	5%
R103	1 M	1/2 W	mf	1%
R104	3.92 k	1/2 W	mf	1%
R105	5.62 k	1/2 W	mf	1%
R106	10 k	1/2 W	comp	5%
R107	1 M	1/2 W	comp	5%
R108	10 k	1/2 W	comp	5%
R109	332 k	1/2 W	mf	1%
R110	12.1 k	1/2 W	mf	1%
R111	294 k	1/2 W	mf	1%
R112	332 k	1/2 W	mf	1%
R113	4.99 k	1/2 W	mf	1%
R114	51.1 k	1/2 W	mf	1%
R115	20 k	1 W	trimmer	
R116	40.2 k	1/2 W	mf	1%
R117	560 ohms	1/2 W	comp	5%
R118	3.3 k	1/2 W	comp	5%
R119	82 ohms	2 W	comp	5%
R120	47 ohms	1/2 W	comp	5%
R121	82 ohms	2 W	comp	5%
R122	4.99 k	1/2 W	mf	1%
R123	4.99 k	1/2 W	mf	1%
R124	1 k	1/2 W	comp	5%
R125	2.21 k	1/2 W	mf	1%
R126	2.74 k	1/2 W	mf	1%
R127	2.21 k	1/2 W	mf	1%
R128	2.21 k	1/2 W	mf	1%
R129	1 k	1/2 W	mf	1%
R130	51.1 k	1/2 W	mf	1%
R131	20 k	1 W	trimmer	
R132	3.3 k	1/2 W	comp	5%
R133	10 k	1/2 W	comp	5%
R134	560 ohms	1/2 W	comp	5%
R135	47 ohms	1/2 W	comp	5%
R140	510 ohms	1/2 W	comp	5%
R141	560 ohms	1/2 W	comp	5%
R142	680 ohms	1/2 W	comp	5%
R143	750 ohms	1/2 W	comp	5%
R144	49.9 ohms	1/2 W	mf	1%
R145	49.9 ohms	1/2 W	mf	1%
R146	10 ohms	1/2 W	comp	5%
R147	10 ohms	1/2 W	comp	5%
R245	1 M	1/4 W	mf	1%
R246	1 M	1/4 W	mf	1%
R247	1 M	1/4 W	mf	1%
R248	43.2 k	1/4 W	mf	1%

Transistors

Q20	MPS 2924
Q21	MPS 2924
Q22	MPS 2924
Q23	MPS 2924
Q24	MPS 2924
Q25	MPS 3638
Q26	MPS 3638
Q27	MPS 2924
Q28	MPS 2924
Q29	MPS 2924
Q30	MPS 3638
Q31	MPS 2924
Q32	MPS 2924
Q33	MPS 2924
Q34	MPS 2924
Q35	E101 (Siliconix)
Q36	E101 (Siliconix)
Q37	2N3906
Q38	2N3906
Q39	MPS 3707
Q40	2N4234
Q41	2N4237
Q42	MPS 3638
Q43	2N4237
Q44	MPS 3638
Q45	MPS 2924 — Common heat sink.
Q46	MPS 2924 — Order Part No. 7-006
Q47	2N3906
Q48	2N3906
Q49	MPS 2924
Q50	MPS 3638
Q51	MPS 6532
Q52	2N4234