

# Technical Information Manual

Revision n. 1  
14 March 2001

**MOD. V 812**  
*16 CHANNEL  
CONSTANT  
FRACTION  
DISCRIMINATOR*

**NPO:**  
**00101/97:V812x.MUTx/01**

CAEN will repair or replace any product within the guarantee period if the Guarantor declares that the product is defective due to workmanship or materials and has not been caused by mishandling, negligence on behalf of the User, accident or any abnormal conditions or operations.

**CAEN declines all responsibility for damages or injuries caused by an improper use of the Modules due to negligence on behalf of the User. It is strongly recommended to read thoroughly the CAEN User's Manual before any kind of operation.**



*CAEN reserves the right to change partially or entirely the contents of this Manual at any time and without giving any notice.*

---

# TABLE OF CONTENTS

<b>1. GENERAL DESCRIPTION.....</b>	<b>6</b>
1.1. FUNCTIONAL DESCRIPTION.....	6
1.2. BLOCK DIAGRAM.....	7
1.3. TECHNICAL SPECIFICATION TABLE.....	8
<b>2. TECHNICAL SPECIFICATIONS .....</b>	<b>9</b>
2.1. PACKAGING.....	9
2.2. POWER REQUIREMENTS.....	9
2.3. FRONT PANEL.....	10
2.4. EXTERNAL CONNECTORS.....	11
2.4.1. <i>INPUT connectors</i> .....	11
2.4.2. <i>OUTPUT connectors</i> .....	11
2.5. OTHER COMPONENTS.....	12
2.5.1. <i>Displays</i> .....	12
2.5.2. <i>Switches</i> .....	12
2.5.3. <i>Jumpers</i> .....	12
<b>3. VME INTERFACE .....</b>	<b>15</b>
3.1. ADDRESSING CAPABILITY.....	15
3.2. DISCRIMINATOR THRESHOLDS.....	16
3.3. PATTERN OF INHIBIT .....	16
3.4. OUTPUT WIDTH CH. 0 TO 7.....	16
3.5. OUTPUT WIDTH CH. 8 TO 15.....	16
3.6. DEAD TIME CH. 0 TO 7 .....	16
3.7. DEAD TIME CH. 8 TO 15.....	17
3.8. MAJORITY THRESHOLD .....	17
3.9. TEST PULSE .....	17
3.10. MODULE IDENTIFIER WORDS.....	17
<b>4. PRINCIPLES OF OPERATION .....</b>	<b>19</b>
4.1. THE CONSTANT FRACTION DISCRIMINATION TECHNIQUE .....	19
4.2. POWER ON / RESET STATUS.....	19
4.3. SETTING THE DELAY.....	19
4.4. ENABLING/DISABLING THE CHANNELS.....	19
4.5. TEST, VETO AND OR SIGNALS.....	20

4.6.	CHANNELS TEST .....	20
4.7.	SETTING THE THRESHOLD.....	20
4.8.	SETTING THE OUTPUT PULSE WIDTH.....	20
4.9.	SETTING THE DEAD TIME .....	21
4.10.	CURRENT SUM SIGNAL .....	21
4.11.	MAJORITY SETTING.....	22

---

## ***LIST OF FIGURES***

FIG. 1.1: BLOCK DIAGRAM .....	7
FIG. 2.1: FRONT PANEL .....	10
FIG. 2.2: COMPONENTS LOCATION .....	13
FIG. 2.3: JUMPERS LOCATION .....	14
FIG. 3.1: MODULE IDENTIFIER WORDS.....	17
FIG. 4.1: CURRENT SUM SIGNAL .....	21
FIG. 4.2: EXAMPLE OF THREE DAISY CHAINED V812.....	23

---

## ***LIST OF TABLES***

TABLE 1.1: VERSIONS AVAILABLE FOR THE MODEL V812 .....	6
TABLE 1.2: TECHNICAL SPECIFICATION TABLE .....	8
TABLE 2.1: POWER REQUIREMENTS .....	9
TABLE 3.1: ADDRESS MAP .....	15

# 1. General description

## 1.1. Functional description

The CAEN Model V812 is a 16 CHANNEL CONSTANT FRACTION DISCRIMINATOR housed in a single width VME module. The module accepts 16 negative inputs and produces 16 differential ECL outputs with a fan-out of two on four front panel flat cable connectors (a functional block diagram is shown in Fig. 1.1).

Each channel can be turned on or off via VME by using a mask register (Pattern of Inhibit). The pulse forming stage of the discriminator produces an output pulse whose width is adjustable in a range from 15 ns to 250 ns via VME. Moreover, in order to protect against multiple pulsing, it is possible to program via VME a Dead Time during which the discriminator is inhibited from retriggering. The maximum time walk is  $\pm 400$  ps (for input signals in the range from -50 mV to -5 V with 25 ns rise time). The constant fraction is 20%. The constant fraction delay is defined by a delay line network of 20 ns with 5 taps (see fig. 2.2). The discriminator thresholds are settable via VME in a range from -1 mV to -255 mV (1 mV step) through an 8-bit DAC. The module can operate also with small (below 10 mV) input signals, though in this case the Constant Fraction operation is not performed, i.e. the walk is higher. VETO and TEST inputs are available on the front panel. The front panel is provided with a Current Sum output that generates a current proportional to the input multiplicity, i. e. to the number of channels over threshold, at a rate of -1.0 mA per hit (-50 mV per hit into a 50 Ohm load)  $\pm 20\%$ . A "MAJORITY" output provides a NIM signal if the number of input channels over threshold exceeds the MAJORITY programmed value. The logic OR of discriminator outputs is available on a front panel connector. The relevant "OR" LED lights up if at least one of the unmasked channels is over threshold. The module's operations are completely controlled via software for each channel through the VME bus. The most important are:

- setting the discriminator thresholds (8 bit data) from -1 to -255 mV.
- setting pattern of inhibit; each channel can be turned "ON" or "OFF" by using a mask register.
- setting output pulse width
- setting the Majority threshold value.
- selection of the Dead Time value.

The standard version (**Mod. V812**) uses the VME P1 and P2 connectors and the auxiliary connector (PAUX) for the V430 VMEbus crate. A V812 version without PAUX connector (**Mod. V812 B**) is also available.

**Table 1.1: Versions available for the Model V812**

Version	Number of channels	PAUX connector <sup>1</sup>
V812	16	yes
V812 B	16	no

<sup>1</sup> The version with the PAUX connector requires the V430 backplane.

## 1.2. Block diagram

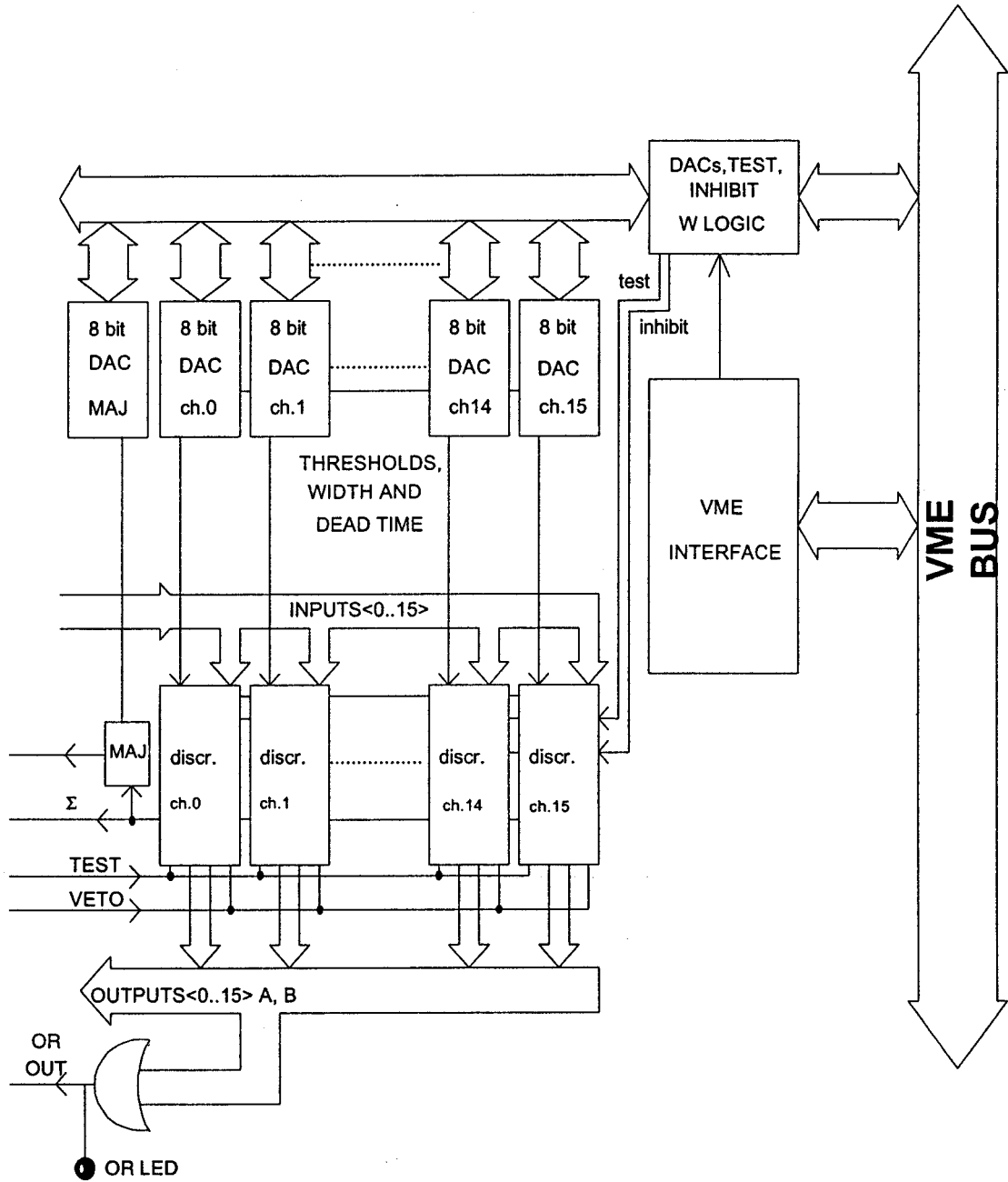


Fig. 1.1: Block Diagram

### 1.3. Technical specification table

Table 1.2: Technical specification table

<b>Packaging</b>	6U-high, 1U-wide VME unit
<b>Power requirements</b>	Refer to § 2.2
<b>Inputs</b>	16 inputs (negative polarity, 50 $\Omega$ impedance)
<b>Max input voltage</b>	-5 V
<b>Min detectable signal</b>	-5 mV
<b>Threshold range</b>	-1 mV to -255 mV (1 mV step)
<b>Constant fraction</b>	20%
<b>Delay</b>	Selectable in 4 ns steps (20 ns full scale)
<b>Outputs</b>	16 outputs with a fan-out of two (ECL, 110 $\Omega$ impedance)
<b>Input/output delay</b>	Set delay+4.5 $\pm$ 2 ns
<b>Output width</b>	Programmable from 15 ns to 250 ns
<b>Dead Time</b>	Programmable from 150 ns to 2 $\mu$ s ( $\pm$ 10%)
<b>Max outputs time walk</b>	$\pm$ 400 ps for input signals in the range from -50 mV to - 5 V with 25 ns rise time
<b>Autowalk</b>	Automatic adjustment of input offset and low frequency input noise of $\pm$ 40 mV
<b>Control inputs</b>	NIM logic signals, high impedance: <b>VETO:</b> allows to veto all channels simultaneously <b>TEST:</b> triggers all the enabled channels at once
<b>Control outputs</b>	<b>MAJORITY:</b> standard NIM logic signal, 50 $\Omega$ impedance; it indicates if the number of input channels over threshold exceeds the MAJORITY level programmed via VME <b>OR:</b> standard NIM signal, 50 $\Omega$ impedance; logic OR of outputs <b><math>\Sigma</math>:</b> current proportional to input multiplicity (-1 mA $\pm$ 20% per hit), high impedance
<b>Displays</b>	<b>DTACK:</b> green LED; lights up at each VME access <b>OR:</b> green LED; it lights up if at least one output signal is present



---

## **2. Technical Specifications**

---

### **2.1. Packaging**

The Mod. V812 is housed in a 6U-high 1U-wide VME unit.

---

### **2.2. Power requirements**

The power requirements of the Mod. V812 are as follows:

**Table 2.1: Power requirements**

	<b>V812</b>	<b>V812 B</b>
<b>+ 12 V</b>	100 mA	100 mA
<b>- 12 V</b>	60 mA	60 mA
<b>+ 5 V</b>	1 A	5.5 A
<b>- 5 V</b>	3 A	

## 2.3. Front Panel

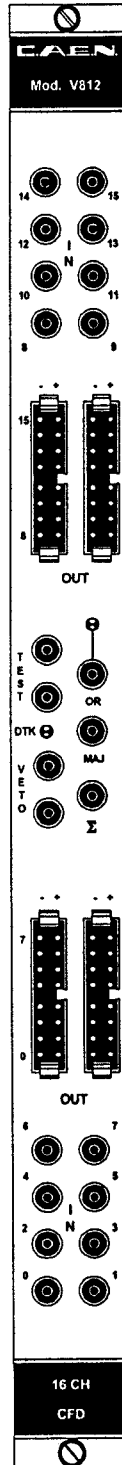


Fig. 2.1: Front Panel

---

## 2.4. External connectors

The location of the connectors is shown in Fig. 2.1. Their function and electromechanical specifications are listed in the following subsections.

---

### 2.4.1. INPUT connectors

#### INPUT CHANNELS:

Mechanical specifications:

16 LEMO 00 type connectors.

Electrical specifications:

Negative polarity, 50 Ohm impedance.

Max input voltage: -5 V.

Min detectable signal: -5 mV.

#### VETO INPUT:

Mechanical specifications:

1 LEMO 00 type connectors.

Electrical specifications:

Standard NIM logic signal, high impedance, 30 ns minimum FWHM; leading edge of the VETO signal must precede of at least 18 ns the leading edge of the input and overlap completely the input signal.

#### TEST INPUT:

Mechanical specifications:

1 LEMO 00 type connectors.

Electrical specifications:

Standard NIM logic signal, high impedance

8 ns minimum FWHM

Max input frequency: 30 MHz

---

### 2.4.2. OUTPUT connectors

#### OUTPUT CHANNELS:

Mechanical specifications:

4 Header 3M 3408-D202 type, 8+8 pin connectors.

Electrical specifications:

Differential ECL level on 110 Ohm impedance; pulse width adjustment from 16.5±1.5 ns to 270±25 ns; maximum time walk is ±400 ps for input signals in the range from -50 mV to -5 V with 25 ns rise time.

Input/Output delay: set delay+4.5±2 ns.

#### OR OUTPUT:

Mechanical specifications:

1 LEMO 00 type connectors.

Electrical specifications:

Standard NIM logic signal, 50 Ω impedance.

Rise/fall time < 4 ns.

Max output frequency: 30 MHz.

**$\Sigma$  OUTPUT:**

Mechanical specifications:

1 LEMO 00 type connectors.

Electrical specifications:

current output (-1 mA  $\pm$  20% per hit), high impedance.

Rise/fall time < 8 ns.

Max output frequency: 30 MHz

**MAJORITY OUTPUT:**

Mechanical specifications:

1 LEMO 00 type connectors.

Electrical specifications:

Standard NIM logic signal, 50  $\Omega$  impedance.

---

## 2.5. Other components

---

### 2.5.1. Displays

The front panel hosts the following LEDs:

**DTACK**

Type: 1 green LED

Function: VME selected; it lights up during a VME access.

**OR**

Type: 1 green LED

Function: it lights up if at least one output signal is present.

---

### 2.5.2. Switches

**ROTARY SWITCHES**

Function: they allow to select module's VME address; please refer to Fig. 2.2 for their setting.

---

### 2.5.3. Jumpers

**JP1**

Function: it allows to select the Majority logic (Internal, External); please refer to Fig. 2.3 for the jumper location on the V812 board.

**JP2...JP17**

Function: they allow to set the Delay. The Delay values range up to 20 ns with 4 ns steps (please refer to Fig. 2.3 for the jumpers location on the V812 board). Factory setting is 20 ns.

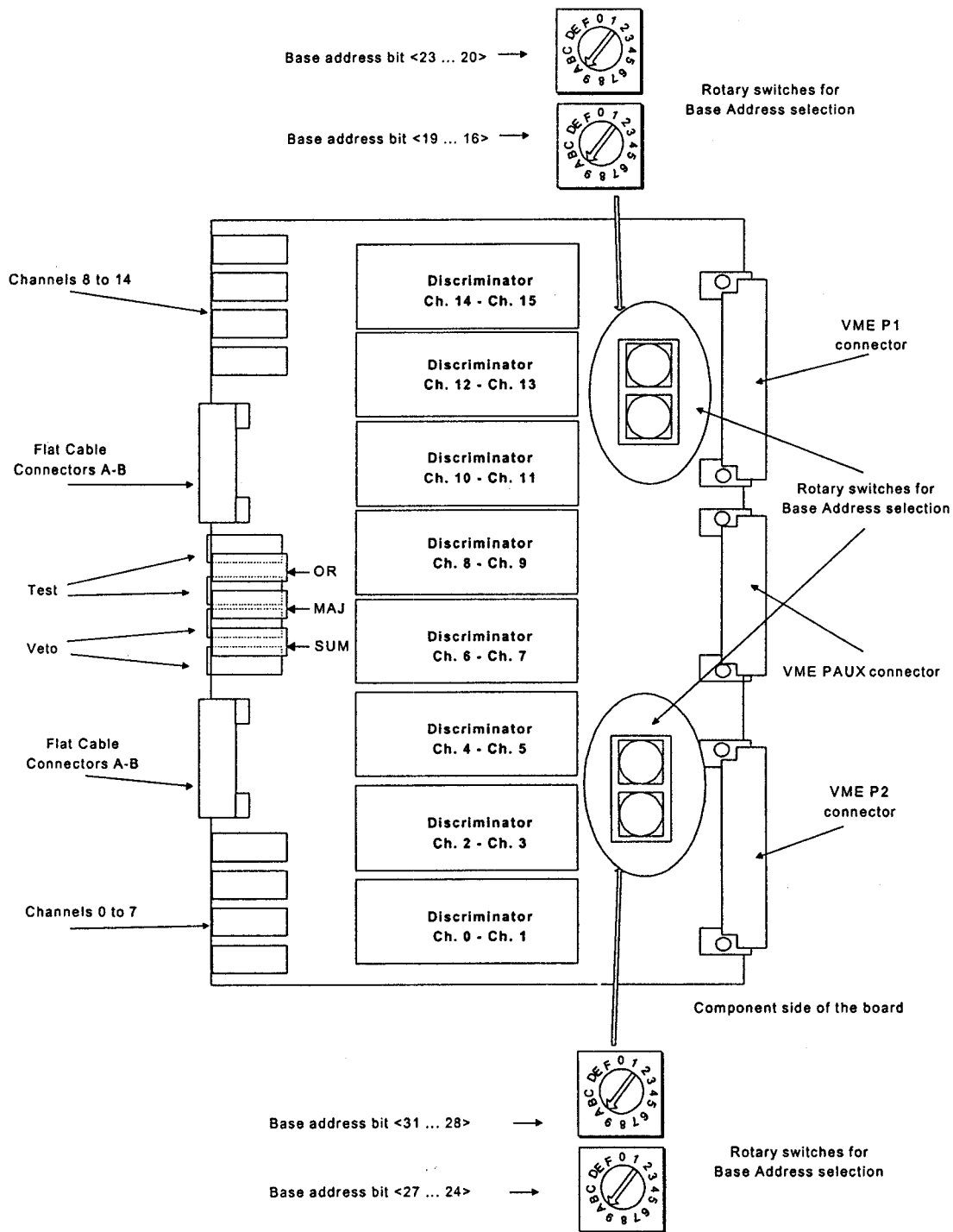


Fig. 2.2: Components location

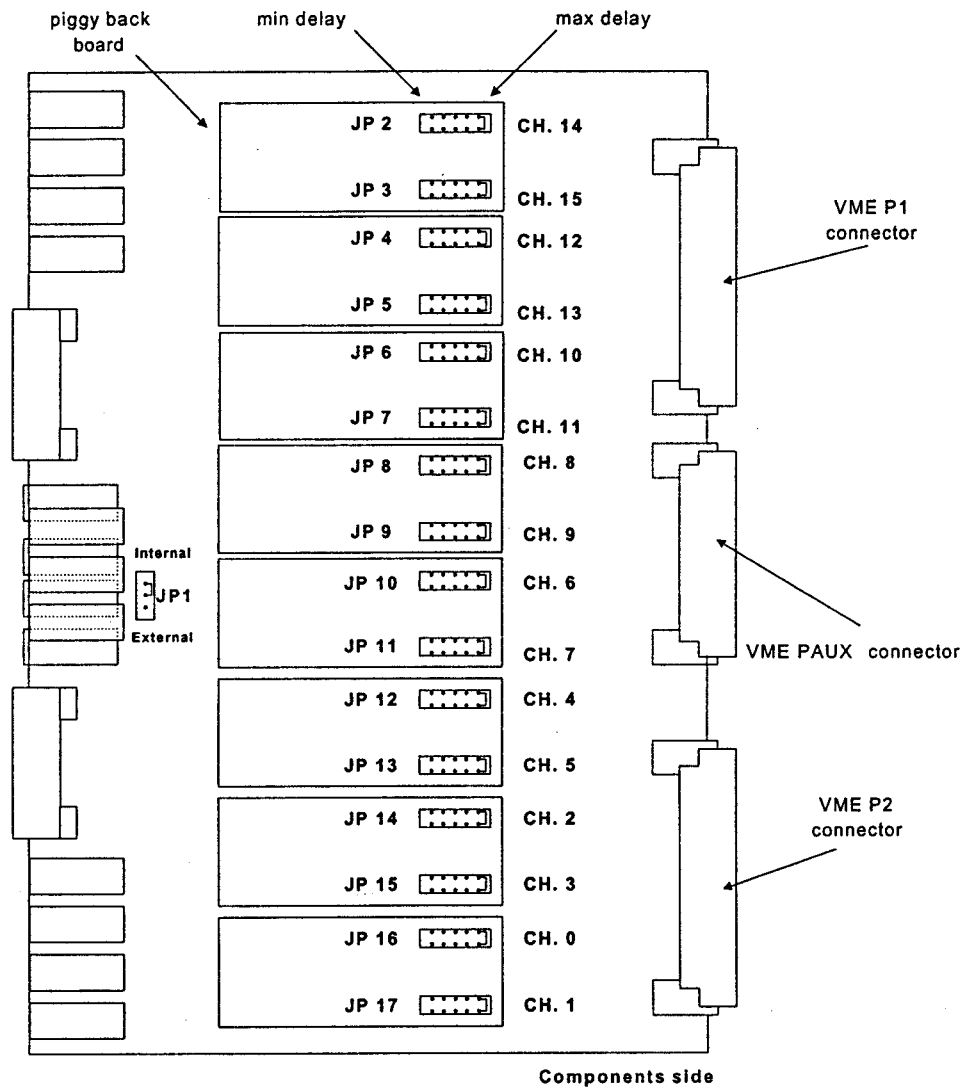


Fig. 2.3: Jumpers location

### 3. VME Interface

#### 3.1. Addressing Capability

The V812 module works in A24/A32 mode. This implies that the module's address must be specified in a field of 24 or 32 bits. The address modifiers codes recognized by the module are:

AM = %39	Standard user data access
AM = %3D	Standard supervisor data access
AM = %09	Extended user data access
AM = %0D	Extended supervisor data access

The module's Base address is fixed by 4 internal rotary switches housed on two piggy-back boards plugged into the main printed circuit board (see Fig. 2.2).

The Base address can be selected in the range:

% 00 0000 <-> % FF 0000	A24 mode
% 0000 0000 <-> % FFFF 0000	A32 mode

The module's address lines A09+A15 are not connected, so their content is meaningless: for example writing to either Base + 104C or Base + 284C the same register is accessed.

**Table 3.1: Address Map**

ADDRESS	REGISTER/CONTENT	TYPE
Base + %00	Threshold register Ch. 0	Write only
Base + %02	Threshold register Ch. 1	Write only
Base + %04	Threshold register Ch. 2	Write only
Base + %06	Threshold register Ch. 3	Write only
Base + %08	Threshold register Ch. 4	Write only
Base + %0A	Threshold register Ch. 5	Write only
Base + %0C	Threshold register Ch. 6	Write only
Base + %0E	Threshold register Ch. 7	Write only
Base + %10	Threshold register Ch. 8	Write only
Base + %12	Threshold register Ch. 9	Write only
Base + %14	Threshold register Ch. 10	Write only
Base + %16	Threshold register Ch. 11	Write only
Base + %18	Threshold register Ch. 12	Write only
Base + %1A	Threshold register Ch. 13	Write only
Base + %1C	Threshold register Ch. 14	Write only
Base + %1E	Threshold register Ch. 15	Write only
Base + %40	Output width register Ch. 0 to 7	Write only
Base + %42	Output width register Ch. 8 to 15	Write only
Base + %44	Dead Time register Ch. 0 to 7	Write only
Base + %46	Dead Time register Ch. 8 to 15	Write only
Base + %48	Majority threshold register	Write only
Base + %4A	Pattern inhibit register	Write only
Base + %4C	Test pulse register	Write only
Base + %FA	Fixed code	Read only
Base + %FC	Manufacturer & Module type	Read only
Base + %FE	Version & Serial number	Read only

---

### **3.2. Discriminator thresholds**

(Base address + %00 to %1E write only)

These registers contain the discriminator threshold values on 8 bit words. The threshold values can be programmed in a range from -1 mV to -255 mV with 1 mV steps, writing an integer number between 1 and 255 into the register, although a minimum threshold of -5 mV is required; the channel thresholds are individually settable.

---

### **3.3. Pattern of Inhibit**

(Base address + %4A write only)

This register contains the Pattern of Inhibit, a 16 bit word indicating which channels are either enabled or disabled (bit X=1 ⇒ Ch. X enabled...bitX=0 ⇒ Ch. X disabled).

---

### **3.4. Output width Ch. 0 to 7**

(Base address + %40 write only)

This register contains the output pulse width value of the channels 0 through 7 on a 8 bit word. This value can be adjusted in the range from 15 ns to 250 ns, writing an integer number between 0 and 255 into the register. The set value corresponds to the width as follows: 255 leads to a 250 ns pulse duration, 0 leads to a 15 ns pulse duration, with a non-linear relation for intermediate values.

---

### **3.5. Output Width Ch. 8 to 15**

(Base address + %42 write only)

This register contains the output pulse width value of the channels 8 through 15 on a 8 bit word. This value can be adjusted in the range from 15 ns to 250 ns, writing an integer number between 0 and 255 into the register. The set value corresponds to the width as follows: 255 leads to a 250 ns pulse duration, 0 leads to a 15 ns pulse duration, with a non-linear relation for intermediate values.

---

### **3.6. Dead Time Ch. 0 to 7**

(Base address + %44 write only)

This register is used to select the Dead Time value common to all channels from 0 to 7. This command allows to select on 8 bit (set values: 0 to 255) the Dead Time value between 150 ns and 2 μs. The set value corresponds to the pulse width as follows: 255 leads to a 2 μs value, 0 leads to a 150 ns value.

**N.B.: The actual Dead Time is equal to the greater between output width and Dead Time set values**



### 3.7. *Dead Time Ch. 8 to 15*

(Base address + %46 write only)

This register is used to select the Dead Time value common to all Channels from 8 to 15. This command allows to select on 8 bit (set values: 0 to 255) the Dead Time value between 150 ns and 2 μs. The set value corresponds to the pulse width as follows: 255 leads to a 2 μs value, 0 leads to a 150 ns value.

**N.B.:** the actual Dead Time is equal to the greater between output width and Dead Time set values.

### 3.8. *Majority threshold*

(Base address + %48 write only)

This register allows to set the Majority threshold between 1 and 16 for Internal Majority and between 1 and 20 for External Majority by writing a proper value in the Base address + %48 (set values: 1 to 244).

The relation to use is the following:

$$MAJTHR = NINT[(MAJLEV*50 - 25)/4]$$

where NINT is the nearest integer function (allowed values for MAJLEV: 1 to 20) e.g., if the User wants to use a majority level of 5, the correct MAJTHR value to use is 56.

### 3.9. *Test pulse*

(Base address + %4C write only)

A test pulse on all output channels can be generated by performing a write access at Base address + %4C; the test pulse is generated independently from the number written into this register.

### 3.10. *Module identifier words*

(Base address + %FA, + %FC, + %FE, read only)

Three words located at the address Base + %FA, + %FC, + %FE of the page are used to identify the module, as shown in Fig. 3.1:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
Version				Module's serial number												Base + % FE
Manufacturer number						Module type										Base + % FC
% FA Fixed code								% F5 Fixed code								Base + % FA

**Fig. 3.1: Module Identifier Words**

At the address Base + %FA the two particular bytes allow the automatic localization of the module.

For the Mod. V812 the word at the address Base + %FC has the following configuration:

Manufacturer N° = 000010 b  
Type of module = 0001010001 b

The word located at the address Base + %FE identifies the single module via a serial number, and any change in the hardware (for example the use of faster conversion logic) will be shown by the version number.

---

## **4. Principles of operation**

---

### **4.1. The Constant Fraction Discrimination technique**

The Constant Fraction Discrimination technique is based on summing a delayed, full height input signal to an inverted and attenuated signal. The resulting signal is fed into a zero-crossing comparator, thus obtaining a precise timing information that virtually eliminates any walk errors induced by constant rise time and varying amplitude signals. For correct operation the maximum of the attenuated pulse has to cross the delayed pulse at the selected fraction. This condition leads to the following relation:

$$T_{\text{delay}} = T_{\text{rise}} * (1 - F)$$

where:

$T_{\text{delay}}$  = selected delay on the Constant Fraction Discriminator

$T_{\text{rise}}$  = rise time of the input signals

F = Constant Fraction value

The Mod. V812 Constant Fraction Discriminator features a factory setting of 20% for the fraction and 20 ns for the full scale delay. The delay can be selected in 4 ns steps up to 20 ns

---

### **4.2. Power ON / Reset Status**

At Power ON the contents of all the module's registers are not determined. A setting of the registers must be performed before any other operation.

---

### **4.3. Setting the Delay**

For each channel, a 5-positions jumper allows to set the Delay according to the formula expressed in § 4.1. The Delay values range up to 20 ns with a step of 4 ns; in order to gain access to the jumpers it's necessary to unplug the relevant piggy back board (see for the jumpers location on the V812 board). Factory setting is 20 ns. The fraction is a fixed 20% value.

---

### **4.4. Enabling/Disabling the channels**

The User can enable or disable each of the 16 channels via VME by performing a VME write access at Base address + %4A. A channel is enabled if the corresponding bit of the Pattern of Inhibit is high (e. g., bin. 1111 1111 1111 0011, or hex FFF3, disables channels 2 and 3 of the discriminator).

---

## 4.5. Test, Veto and Or signals

Some operations can be performed by sending two external NIM signals:

- **TEST**: an input signal sent through this connector triggers all the enabled channels at once. This feature allows to test of the module as well as to generate a pattern of pulses suitable to test any following electronics.
- **VETO**: an input signal sent through this connector allows to veto all channels simultaneously. A veto pulse of width T will inhibit the input channels for a period with a T duration. Its leading edge must precede the input signal leading edge by at least 8 ns and overlap completely the input signal.

**Note:** TEST and VETO are high impedance inputs and each one is provided with two bridged connectors for daisy chaining; the chain has to be terminated on 50 Ohm on the last module; the same is needed also if one module only is used, whose inputs have thus to be properly matched

- An **OR** output connector provides also the logical OR of the output channels. The relevant "OR" LED lights up if at least one of the enabled channels is over threshold.

---

## 4.6. Channels test

It is possible to obtain pulses on all channels:

- by sending a NIM pulse through one of the two "TEST" connectors located on the front panel.
- by performing a Write operation at (Base address + %4C).

---

## 4.7. Setting the threshold

For each channel of the V812 the discriminator threshold is set up via an 8 bit DAC. The threshold values can be programmed in a range from -1 mV to -255 mV with -1 mV steps (set values: 1 to 255). As in all Constant Fraction Discriminators, these thresholds are to be set above the noise level: they do NOT correspond to the actual level that triggers the discriminator outputs, the latter being a "constant fraction" of the input signals. In order to write the Threshold for each channel, the User must perform a VME access at (Base address + %00 to %1E).

---

## 4.8. Setting the output pulse width

The output pulse width is adjustable on 8 bit from 15 to 250 ns (set values: 0 to 255) and the chosen value is applied to each group of 8 channels each. It can be set at Base address + %40 for channels 0 to 7 and at Base address + %42 for channels 8 to 15. The

set value corresponds to the Width as follows: 255 leads to a 250 ns value, 0 leads to a 15 ns value, with a non-linear interpolation for intermediate values.

---

## 4.9. Setting the Dead Time

It is possible via VME to set a Dead Time value in common to a group of 8 channels. This prevents the triggering of the discriminator by unwanted pulses occurring within the Dead Time programmed value. It can be set by a VME access at (Base Address + %44) for channels 0 to 7 and at (Base Address + %46) for channels 8 to 15 (set values: 0 to 255). The set value corresponds to the Dead Time as follows: 255 leads to a 2  $\mu$ s value, 0 leads to a 150 ns value with a non-linear interpolation for intermediate values.

**N.B.:** The actual Dead Time is equal to the greater between Output Width and Dead Time set

---

## 4.10. Current Sum signal

The front panel also houses the **Current Sum ( $\Sigma$ )** output connector which provides a current proportional to the input signal multiplicity, i.e. to the number of channels over threshold, at a rate of -1.0 mA per hit (-50 mV per hit into a 50 Ohm load)  $\pm 20\%$ .

**Note:** The  $\Sigma$  output requires a 50 Ohm termination for a correct operation of the Majority logic.

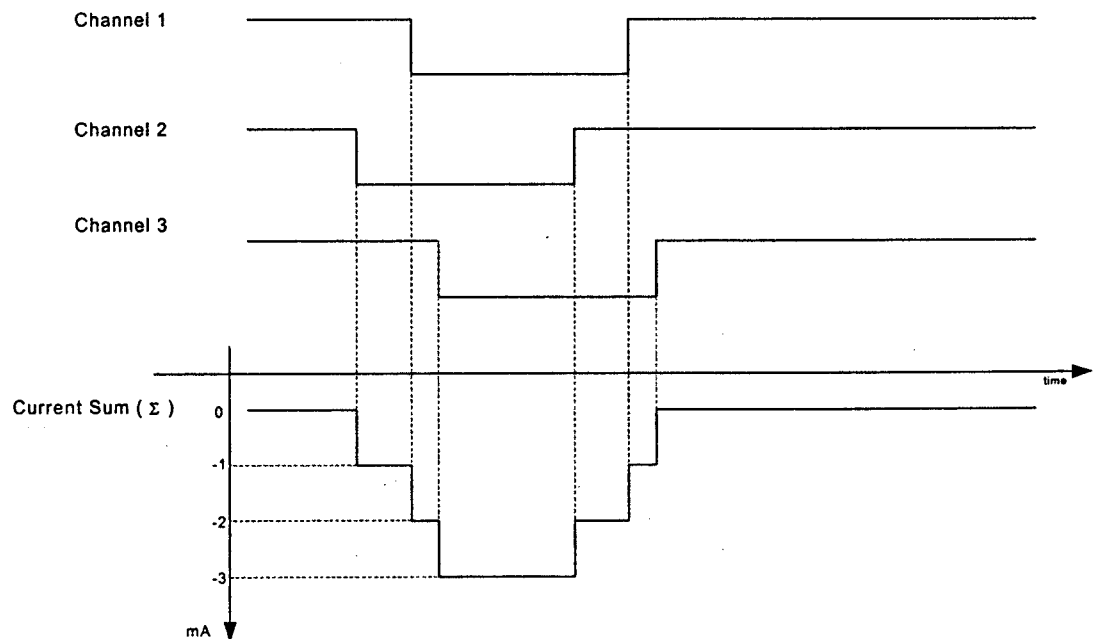


Fig. 4.1: Current Sum signal

## 4.11. Majority setting

Majority output provides a standard NIM signal if the number of channels over threshold exceeds the programmed majority level (MAJLEV). MAJLEV can be programmed between 1 and 16, writing a proper value (MAJTHR) in the Majority threshold register (see § 3.8); valid values range between 0 and 255. MAJTHR can be calculated in the following way:

$$\text{MAJTHR} = \text{NINT}[(\text{MAJLEV} * 50 - 25) / 4]$$

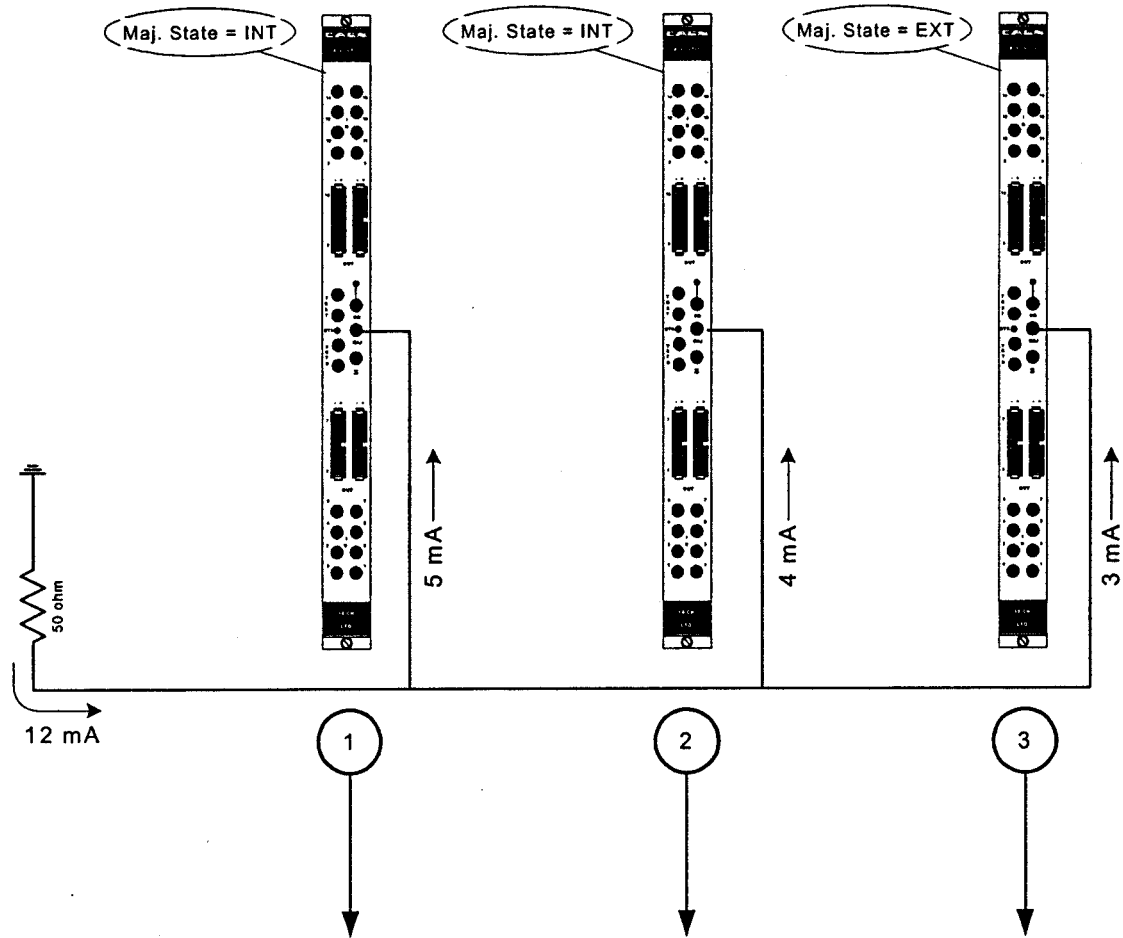
where NINT is the Nearest Integer.

MAJLEV	MAJTHR	MAJLEV	MAJTHR
1	6	11	131
2	19	12	144
3	31	13	156
4	44	14	169
5	56	15	181
6	69	16	194
7	81	17	206
8	94	18	219
9	106	19	231
10	119	20	244

Table 4.1: Majority Level setting values

The Majority logic can be switched from an "Internal" to an "External" position by means of an internal Jumper (see Fig. 2.3).

- **Internal:** With the jumper on the "Internal" position Majority output provides an active signal if the number of the active channels of the module exceeds the programmed majority level (MAJLEV). In this case valid values of MAJLEV are from 1 to 16
- **External:** Several modules can be connected in daisy chain via the  $\Sigma$  outputs. In this case, by setting the Jumper to the "External" position, the Majority logic will act on the sum of the  $\Sigma$  outputs of the connected modules. The majority signal will be active if the sum of chained modules active channels exceeds or is equal to the programmed MAJLEV. (An example with three chained modules is shown in Fig. 4.2). The  $\Sigma$  output line must be terminated with 50 Ohm.



Module Number	1	2	3
Majority State	INT	INT	EXT
Majority Level (MAJLEV)	2 (referred to internal over th. channel)	5 (referred to internal over th. channel)	10 (referred to all chained modules' over th. channels)
Number of Module's active Channels	5	4	3
Majority Output	ACTIVE (5 > MAJLEV)	NON Active (4 < MAJLEV)	ACTIVE (5+4+3 > MAJLEV)

Fig. 4.2: Example of three daisy chained V812