Technical Information Manual

Revision n. 1
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MOD. V977

16 CHANNEL
I/O Register (Status A)
MANUAL REV.1

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1. Overview

1.1. Module description

The Mod. V977 is a 1-unit wide VME module that can work either as 16 channel general purpose I/O Register or as Multihit Pattern Unit; the operating mode is selected via VME and is signalled via front panel LED.

The module has 16 channels; each channel is provided with one input and one output connector. Input signals can be indifferently NIM or TTL; an on-board switch allows to select between NIM and TTL signals for the outputs.
2 LEDs signal the I/O status of each channel.

The module features an additional channel (TEST CHANNEL), which allows to send a test pulse via a front panel pushbutton. The TEST output signal can be either NIM or TTL, selected with the same on-board switch of the channels output.

Input signals can be individually masked via VME or globally via a front panel GATE input. The channel status can be cleared either via VME or via the front panel common CLEAR input. GATE and CLEAR signals can be indifferently NIM or TTL.

The channels global OR and /OR outputs are available as front panel signals and can be eventually masked; OR and /OR can be either NIM or TTL, selected with the same on-board switch of the channels output.

The module houses also a fully programmable VME RORA INTERRUPTER that generates a VME interrupt request when the OR of a selected set of output channels has a TRUE status.

The module uses the VME P1 and P2 connectors, then it fits into both standard and V430 VMEbus crates.

All the models have a special circuitry that allows the board to be removed from and inserted in a powered crate without switching the crate off (Live Insertion).

2. Specifications

2.1. Packaging

1-unit wide VME unit. Height: 6U.

2.2. External components

CONNECTORS:

	Function	Logic	Type connector	Note
16	CHANNELS INPUTS	NIM or TTL	LEMO 00	50 Ω impedance
16	CHANNELS OUTPUTS	NIM or TTL (selectable)	LEMO 00	
1	TEST OUTPUT	NIM or TTL (selectable)	LEMO 00	
1	CLEAR INPUT	NIM or TTL	LEMO 00	50 Ω impedance
1	GATE INPUT	NIM or TTL	LEMO 00	50 Ω impedance
2	OR and NOT OR OUTPUT	NIM or TTL (selectable)	LEMO 00	

LEDS

	Name	Function	Color
16	I/O STATUS	Depends on the module's programming status (see § 3.1)	Green
16	I/O STATUS	Depends on the module's programming status (see § 3.1)	Green
1	DTACK	DATA ACKNOWLEDGE command; lights up each time a VME access is performed.	Green
1	TEST	Lights up as a test signal is sent via pushbutton	Green
1	PATTERN	Indicates the module's programming status; lights up as the module is programmed in PATTERN mode (see § 3.1)	Yellow
1	NIM/TTL	Indicates the selected outputs level: RED=NIM GREEN=TTL	Red/Green

All LEDs also lights up for a while at power ON to indicate that the board is configuring.

PUSHBUTTON:

No.1, to send the TEST input pulse.

2.3. Internal components

SWITCHES (see Fig. 4.1):
No.4, rotary switches for the module VME Base address selection.
No.1 jumper for the output signal type selection (up: NIM, down: TTL).

2.4. Power requirements

Table 2.1: Power requirements

Power supply	Current absorption
+5 V	2.3A

2.5. Technical specification tables

Table 2.2: Technical features

Packaging	1U-wide VME unit
Input channels	16 NIM/TTL levels, 50 Ω impedance
Output channels	16 NIM/TTL levels (selectable), to be terminated on 50 Ω
Min. input width	2 ns
I/O delay	T.B.D.
Double pulse resolution	5 ns
Output rise/fall time	NIM: 1/1 ns; TTL: 3/3 ns

2.6. Front Panel

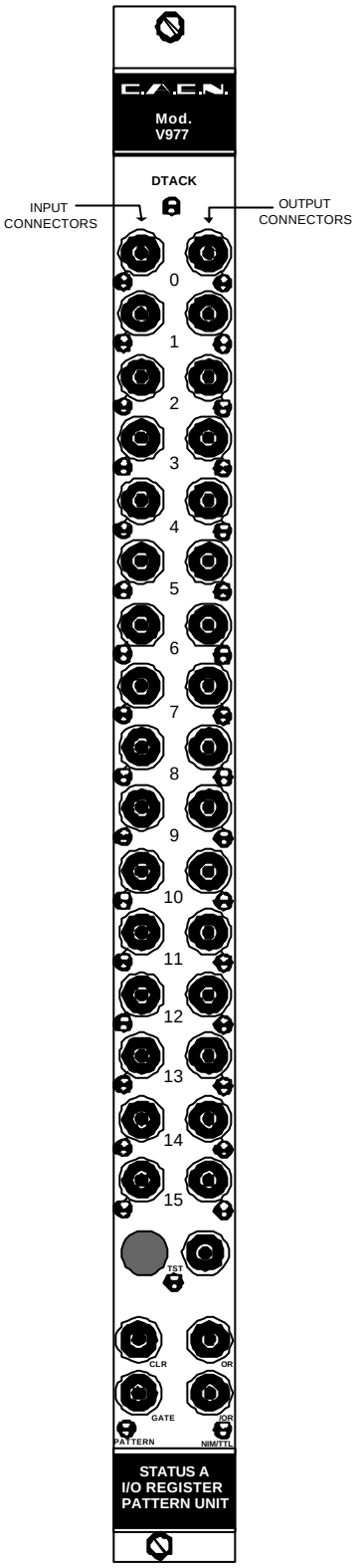


Fig. 2.1: Mod. V977 Front Panel

3. Operating modes

3.1. Functional description

The Mod. V977 is a 16 channel general purpose I/O Register or as Multihit Pattern Unit
The following figure shows the simplified scheme of a single channel:

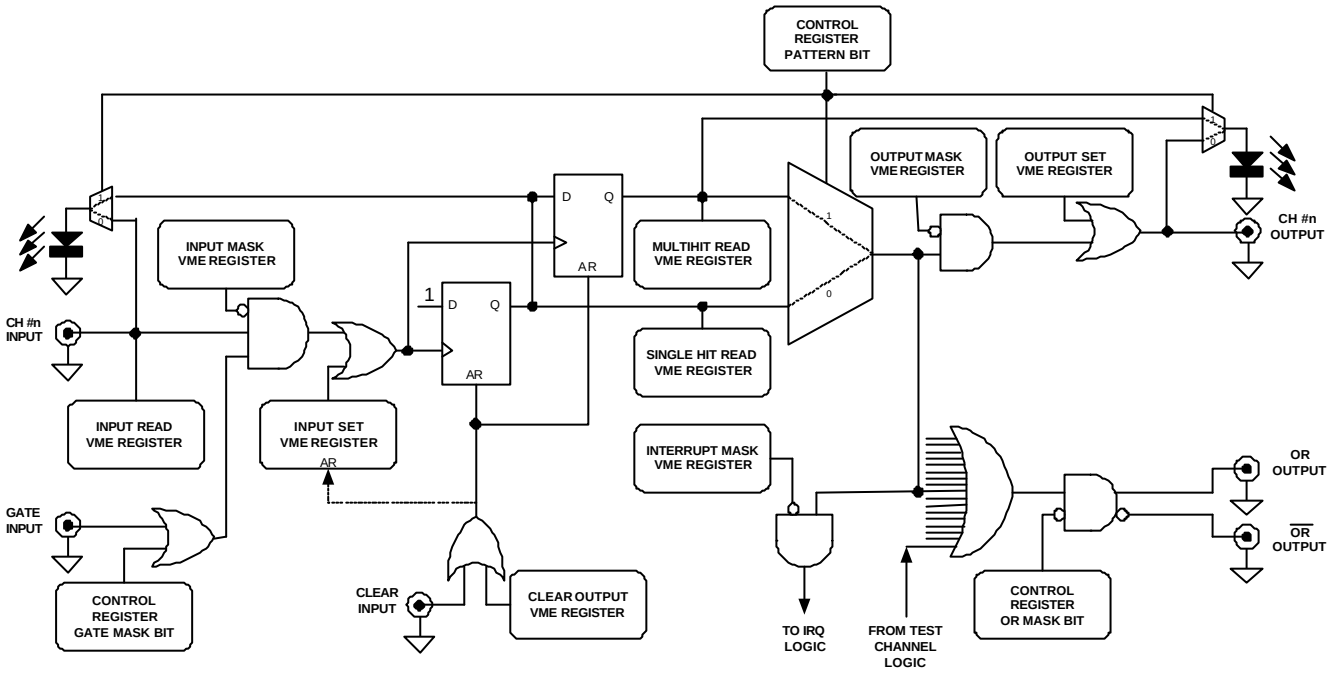


Fig. 3.1: Mod. V977 channel structure

The core of each channel is composed by a couple of FLIP-FLOPs, which perform the memory functions. The two cascaded FLIP-FLOPs, as shown in Fig. 3.1, allow to detect the following events: none, one or two input hits. The FLIP-FLOPs status of all channels can be read via VME, in the SINGLEHIT READ REGISTER and MULTIHIT READ REGISTER, which are related respectively to the first and to the second cascaded FLIP_FLOP. The content of such register can also be read by accessing the SINGLEHIT READ-CLEAR REGISTER and MULTIHIT READ-CLEAR REGISTER: in this case the FLIP-FLOPs are cleared after readout.
The FLIP-FLOPs of all channels can also be cleared both via VME, by accessing the CLEAR OUTPUT REGISTER, and via the front panel CLEAR signal.
The FLIP FLOPs are set either via an input hit or via VME write access (INPUT SET REGISTER). By accessing the CLEAR OUTPUT REGISTER, the INPUT SET REGISTER is cleared.
The capabilty of receiving input hits can be masked via VME through the INPUT MASK REGISTER (individually for each channel), or via the input GATE signal (common to all channels), which can be masked in its turn.
The status of the inputs can also be read directly via VME in the INPUT READ REGISTER.
The status of the channel LEDs and of the outputs depend on the module's programming.

3.1.1. I/O register mode

The module operates as I/O register if the PATTERN bit of the CONTROL REGISTER is set to 0 (default setting).
In this case the simplified channel scheme is shown in Fig. 3.2.

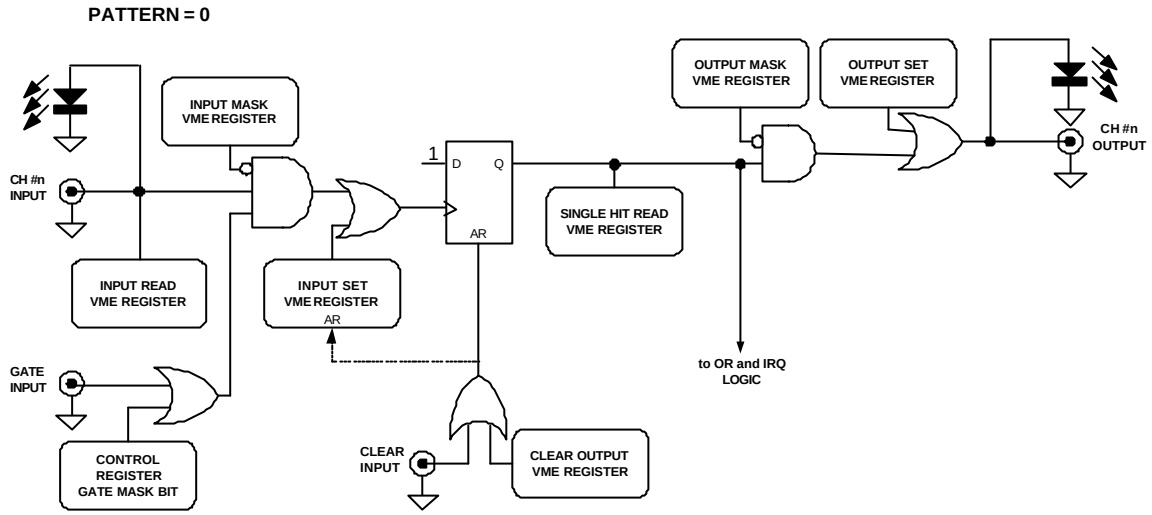


Fig. 3.2: I/O register mode

In this operating mode the output of one channel is active when a single hit (from front panel or VME generated) is received. The output can also be set by a write access to the OUTPUT SET REGISTER.
The outputs can also be masked, individually for each channel, through the OUTPUT MASK REGISTER.
In this operating mode, the two channel LEDs identify the channel status in the following way:
Left LED: input signal active;
Right LED: output signal active.

3.1.2. Multihit pattern unit mode

The module operates as multihit pattern unit if the PATTERN bit of the CONTROL REGISTER is set to 1.
In this case the simplified channel scheme is shown in Fig 3.3.

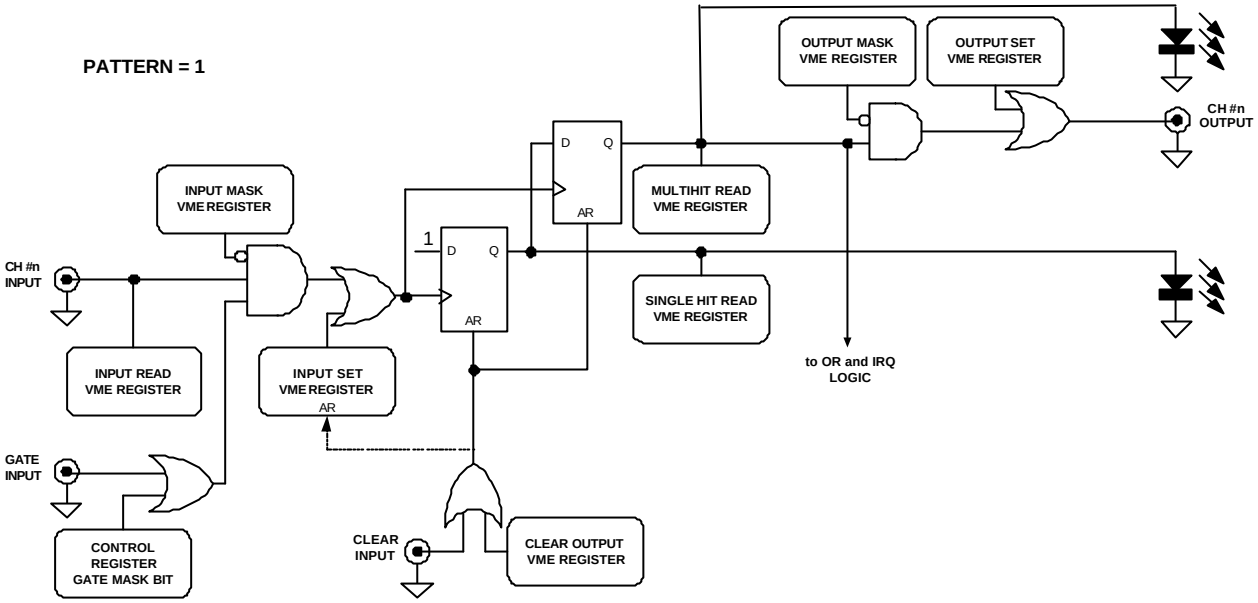


Fig. 3.3: Multihit pattern unit mode

In this operating mode the output of one channel is active when a double hit (from front panel or VME generated) is present. The output can also be set by a write access to the OUTPUT SET REGISTER.
The outputs can also be masked, individually for each channel, through the OUTPUT MASK REGISTER.
In this operating mode, the two channel LEDs identify the channel status in the following way:
Left LED: single hit received;
Right LED: double hit received and output signal active.

3.1.3. Test channel

The module is provided with an extra channel (TEST CHANNEL), which differs from the others since the input pulse is sent by a pushbutton. The TEST channel is completely handled by the Test control register (see § 4.20).

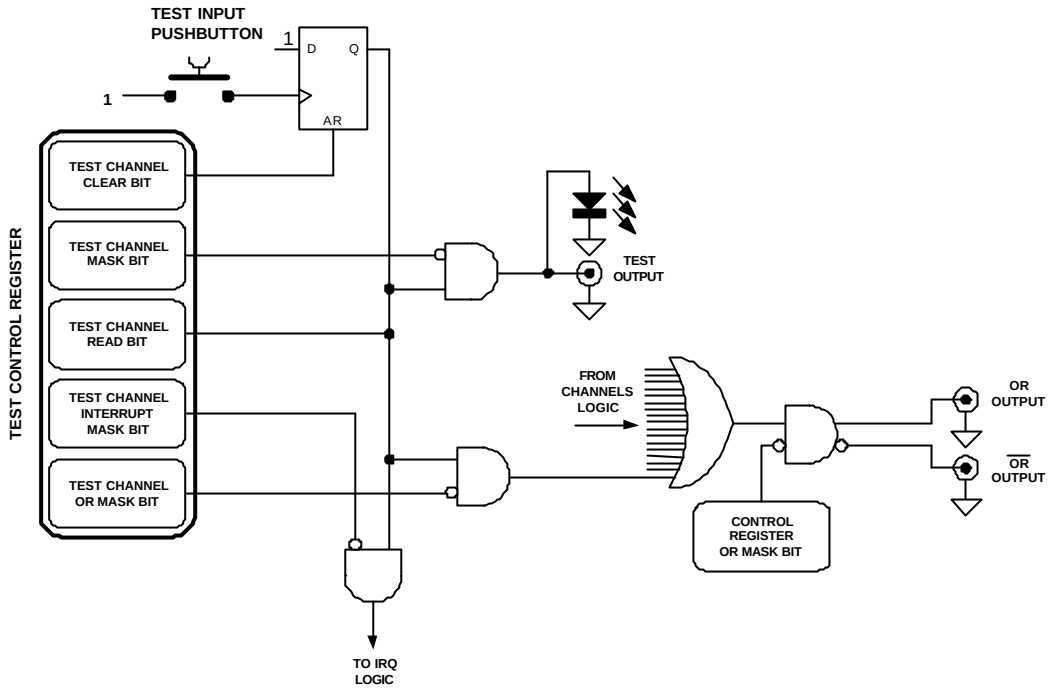


Fig. 3.4: Test channel

3.2. OR logic

As shown in Fig. 3.1 the channels OR and /OR are available as front panel signals and can be eventually masked;
Also the TEST signal participates to the OR logic (it can also be masked).

3.3. Interrupter capability

The Mod. V977 house a VME INTERRUPTER. The module responds to D16 Interrupt Acknowledge cycles providing a word whose 8 LSB are the STATUS/ID.
The interrupt STATUS/ID is 8-bit wide, and it is contained in the 8 LSB of the Interrupt Vector Register (see § 4.16).
The module's interrupter produces its request on one of the 7 IRQ lines. The interrupt level is programmable via VME (see § 4.15).
An Interrupt is generated when the OR of channels' output is True. The channels outputs sent to the interrupt logic can be masked via the INTERRUPT MASK REGISTER. The TEST channel can participate to the IRQ logic as well (see § 4.10)

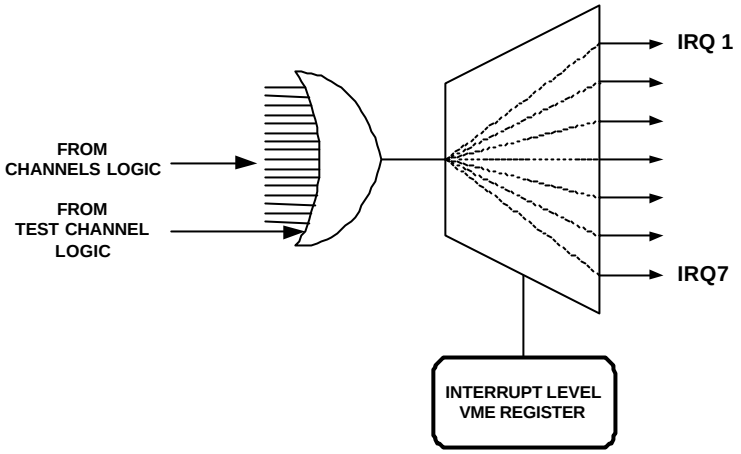


Fig. 3.5: Interrupter scheme

4. VME Interface

4.1. Addressing capability

The module works in A32/A24 mode. This means that the module address must be specified in a field of 32 or 24 bits. The Address Modifiers code recognized by the module are:

AM=%39:	A24 non privileged data access
AM=%3D:	A24 supervisory data access
AM=%09:	A32 non privileged data access
AM=%0D:	A32 supervisory data access

The module's Base Address is fixed by 4 internal rotary switches housed on two piggy-back boards plugged into the main printed circuit board (see Fig. 4.1).
The Base Address can be selected in the range:

0x000000	←→	0xFF0000	A24 mode
0x00000000	←→	0xFFFF0000	A32 mode

The address map of the page is shown in table 4.1.

4.2. Data transfer capability

The V977 registers are accessible in D16 mode

Table 4.1: Address Map for the Mod. V977

ADDRESS	REGISTER/CONTENT	ADDR	DATA	R/W
Base + %0000	INPUT SET	A24/A32	D16	read/write
Base + %0002	INPUT MASK	A24/A32	D16	read/write
Base + %0004	INPUT READ	A24/A32	D16	read only
Base + %0006	SINGLEHIT READ	A24/A32	D16	read only
Base + %0008	MULTIHIT READ	A24/A32	D16	read only
Base + %000A	OUTPUT SET	A24/A32	D16	read/write
Base + %000C	OUTPUT MASK	A24/A32	D16	read/write
Base + %000E	INTERRUPT MASK	A24/A32	D16	read/write
Base + %0010	CLEAR OUTPUT	A24/A32	D16	write only
Base + %0012	RESERVED	-	-	-
Base + %0014	RESERVED	-	-	-
Base + %0016	SINGLEHIT READ-CLEAR	A24/A32	D16	read only
Base + %0018	MULTIHIT READ-CLEAR	A24/A32	D16	read only
Base + %001A	TEST CONTROL REGISTER	A24/A32	D16	read/write
Base + %001C	RESERVED	-	-	-
Base + %001E	RESERVED	-	-	-
Base + %0020	INTERRUPT LEVEL	A24/A32	D16	read/write
Base + %0022	INTERRUPT VECTOR	A24/A32	D16	read/write
Base + %0024	SERIAL NUMBER	A24/A32	D16	read only
Base + %0026	FIRMWARE REVISION	A24/A32	D16	read only
Base + %0028	CONTROL REGISTER	A24/A32	D16	read/write
Base + %002A	DUMMY REGISTER	A24/A32	D16	read/write
Base + %002C	RESERVED	-	-	-
Base + %002E	SOFTWARE RESET	A24/A32	D16	write only

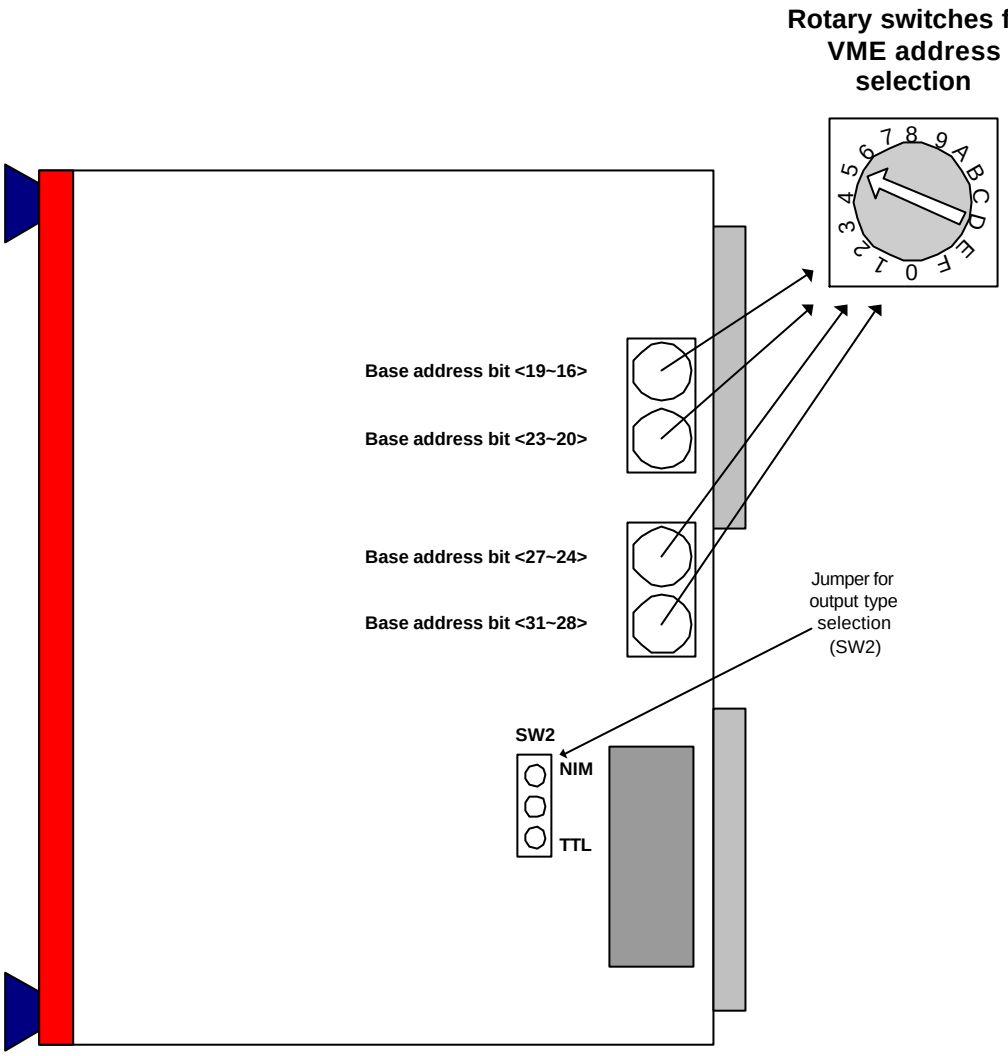


Fig. 4.1: Mod. V977 Base address setting and output selection

4.3. Input set register

(Base address + %0000 read/write)

Each register's bit corresponds to one channel. If one bit is set to 1 the relevant channel FLIP-FLOP (see § 3.1) is set, regardless the corresponding input connector's status.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INPUT SET															

In Multihit pattern unit mode, this register allows to obtain a "double hit" on a channel via VME, by setting and then resetting two times the corresponding bit in this register.
This register default content is 0x0000.

4.4. Input mask register

(Base address + %0002 read/write)

Each register's bit corresponds to one channel. If one bit is set to 1, the related input signal is "masked"; i.e. if a channel is masked the relevant FLIP-FLOP does not receive the front panel signal. The FLIP-FLOPs' Qs can be activated anyway via the relevant bit in the INPUT SET register (see § 4.3).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INPUT MASK															

This register default content is 0x0000: all channels inputs are enabled.

4.5. Input read register

(Base address + %0004 read only)

Each register's bit corresponds to one channel: it reproduces the relevant input connector's logic level, regardless the INPUT MASK register's status.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INPUT READ															

4.6. Single-hit read register

(Base address + %0006 read only)

Each register's bit corresponds to one channel: it reproduces the relevant FLIP-FLOPs' Qs, regardless the OUTPUT MASK register's status. Each bit is set to one as the corresponding channel as received one hit (from front panel or VME generated).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SINGLEHIT READ															

4.7. Multi-hit read register

(Base address + %0008 read only)

Each register's bit corresponds to one channel. Each bit reproduces the relevant FLIP-FLOPs' Qs, regardless the OUTPUT MASK register's status. This register is used only if the module operates in multihit pattern unit mode and signals if one channel has received a double input hit (from front panel or VME generated).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MULTIHIT READ															

4.8. Output set register

(Base address + %000A read/write)

Each register's bit corresponds to one channel. If one bit is set to 1, the corresponding channel output is active, regardless the corresponding input connector's and FLIP-FLOPs' Qs status.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUT SET															

This register default content is 0x0000.

4.9. Output mask register

(Base address + %000C read/write)

Each register's bit corresponds to one channel. If one bit is set to 1, the relevant output is "masked" and no output signal is produced regardless the FLIP FLOPs status. The output signal can be produced anyway via the relevant bit in the OUTPUT SET register (see § 4.8).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUT MASK															

This register default content is 0x0000: all channels outputs are enabled.

4.10. Interrupt mask

(Base address + %000E read/write)

Each register's bit corresponds to one channel, and it is "masked" as the corresponding bit is set to 1. The interrupt request (whose level is set by the INTERRUPT LEVEL register value) is produced when the OR of the channels non mascherati has a TRUE status.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTERRUPT MASK															

This register default content is 0x0000: all channels are unmasked.

4.11. Output clear register

(Base address + %0010 read/write)

A dummy write access to this register clears all the channels FLIP-FLOP.

4.12. Singlehit read-clear register

(Base address + %0016 read only)

Each register's bit corresponds to one channel. This is a different way to access the SINGLE HIT READ REGISTER: a read access to this register clears the first FLIP-FLOP (see § 3.1) of all channels.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SINGLEHIT READ-CLEAR															

4.13. Multihit read-clear register

(Base address + %0018 read only)

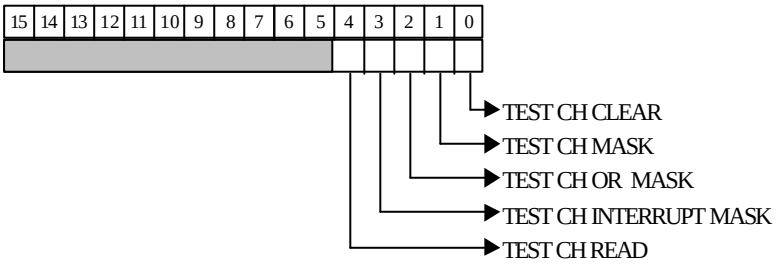
Each register's bit corresponds to one channel. This is a different way to access the MULTI HIT READ REGISTER: a read access to this register clears the second FLIP-FLOP (see § 3.1) of all channels.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MULTIHIT READ-CLEAR															

4.14. Test control register

(Base address + %001A read/write)

This register handles all the TEST INPUT channel operations.



CLEAR BIT: write only. By setting this bit to 1, the TEST CHANNEL FLIP-FLOP is cleared.

MASK BIT: read/write. If this bit is set to 1, the TEST output is "masked": it does not produce an output signal (default setting = 0).

OR MASK BIT: read/write. If this bit is set to 1, the Q signal of the TEST channel is not sent to the OR logic (default setting = 0).

INTERRUPT MASK BIT: read/write. If this bit is set to 1, the Q signal of the TEST channel is not sent to the INTERRUPT logic (default setting = 0).

READ BIT: read only. It reproduces the pushbutton status, regardless the MASK bit status.

4.15. Interrupt level

(Base address + %0020 read/write)

The 3 LSB of this register contain the value of the interrupt level (Bits 3 to 15 are meaningless).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
													LEVEL		

Default setting is 0x0; in this case interrupt generation is disabled.

4.16. Interrupt vector

(Base address + %0022 read/write)

This register contains the STATUS-ID that the V977 places on the VME data bus during the interrupt-acknowledge cycle (Bits 8 to 15 are meaningless).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								STATUS/ID							

Default setting is 0xDD.

4.17. Serial number

(Base address + %0024 read only)

This word reproduces the module's serial number.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SERIAL NUMBER															

4.18. Firmware revision

(Base address + %0026 read only)

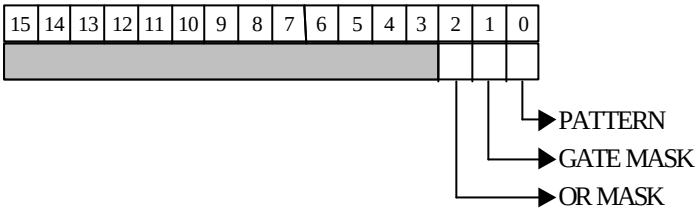
This word reproduces the module's firmware revision in the Rev. X.Y format.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X								Y							

4.19. Control register

(Base address + %0028 read/write)

This register controls the functions common to all channels.



PATTERN BIT: read/write;
= 0: the module works as I/O REGISTER (default setting);
= 1: the module works as a MULTIHIT PATTERN UNIT;

GATE MASK: read/write;
= 1: the GATE sent via FRONT PANEL signal is masked (default setting);
= 0: the GATE sent via FRONT PANEL signal is enabled; incoming hits are accepted only as the GATE is active.

OR MASK: read/write;
= 0: the OR and /OR FRONT PANEL outputs are enabled (default setting);
= 1: the OR and /OR FRONT PANEL outputs are masked.

4.20. Dummy16

(Base address + %002A read/write)

This register allows to perform 16 bit test accesses for test purposes.
Default setting is 0x5555.

4.21. Software reset

(Base address + %002E write only)

A dummy write access to this register allows to generate a single shot RESET of the module, which restores the default conditions.

References

[1] VMEbus Specification Manual Revision C.1 October 1985

[2] VMEBus for Physics Application, Recommendations & Guidelines, Vita23-199x, draft 1.0, 22 May 1997.