BASELINE RESTORER/PILEUP REJECTOR
MODEL 1464

INSTRUCTION MANUAL

January, 1970

Canberra Industries
45 Gracey Ave.
Meriden, Connecticut 06450

Telephone: 203-238-2351

Serial No. _____

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canberra nuclear instruments

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CANBERRA INDUSTRIES, INC.
45 Gracey Avenue
Meriden, Connecticut 06450
Tel: 203-238-2351

BASELINE RESTORER/PILEUP REJECTOR

SECTION 1
INTRODUCTION

The Model 1464 Baseline Restorer/Pileup Rejector brings to the nuclear researcher a highly sophisticated module to aid in solving the problems of high rate, high resolution spectroscopy.

1.1 BASELINE RESTORER

The Baseline Restorer (which can be used without Pileup Rejection) provides a unique restoration technique that prevents the addition of correlated noise to the signal while still providing rapid restoration of the baseline. These two requirements are incompatible using presently available passive and active diode restorers.

The normal time constant of the restorer is sufficiently low to remove the baseline fluctuations caused by microphonics and secondary time constants in the main shaping amplifier. In order to obtain this restoration, the only restriction on the linear input signal is that it be a positive unipolar pulse. The Model 1464 does not add nonlinearity at low amplitudes as only purely resistive elements are used for restoration.

Since there is a signal delay of two microseconds built into the Baseline Restorer and it has an external gate, it is possible to use the Model 1464 as a gated restorer controlled by a single channel analyzer (Canberra Model 1431, 1436, or 1437).

1.2 PILEUP REJECTOR

The Pileup Rejector determines whether an input pulse is contaminated by a second pulse due to pileup, or whether it follows a previous pulse in less time than that selected by the deadtime control. A third restriction is that the detector signal must not have a rise time greater than normal. If any of these events occur, that pulse is eliminated from the output of the Model 1464 Baseline Restorer/Pileup Rejector. Therefore, when the Pileup Rejector is switched on, the output of the Model 1464 consists only of those pulses which contain accurate energy information.

Outputs are available at the rear panel which provide logic pulses for each signal pulse rejected; a standard fast negative NIM logic pulse, for each preamplifier pulse above the discriminator threshold; and a busy logic pulse which lasts from the beginning of an accepted pulse until the end of the deadtime selected.

BASELINE RESTORER/PILEUP REJECTOR
MODEL 1464

CONTENTS

CHANGE INFORMATION

MODEL	SERIAL NUMBER
1464	1270144 and higher

REVISION

A "PERIOD OUT" logic signal has been added to the Model 1464, effective with module serial number 1270144 and higher.

PURPOSE

a. DC operation of the Multichannel Analyzer is essential for optimum energy resolution results when using the Model 1464. To enable DC operation, certain MCA's require a second input to open the ADC's Linear gate whenever a Linear signal is present at its input. The addition of a Model 1464 rear panel PERIOD OUTput connector provides the necessary and proper logic information for opening the Multichannel Analyzer ADC'S Linear gate. This extra feature eliminates the necessity of supplying an "outside" non-delayed logic signal and further enhances compatibility with MCA's.

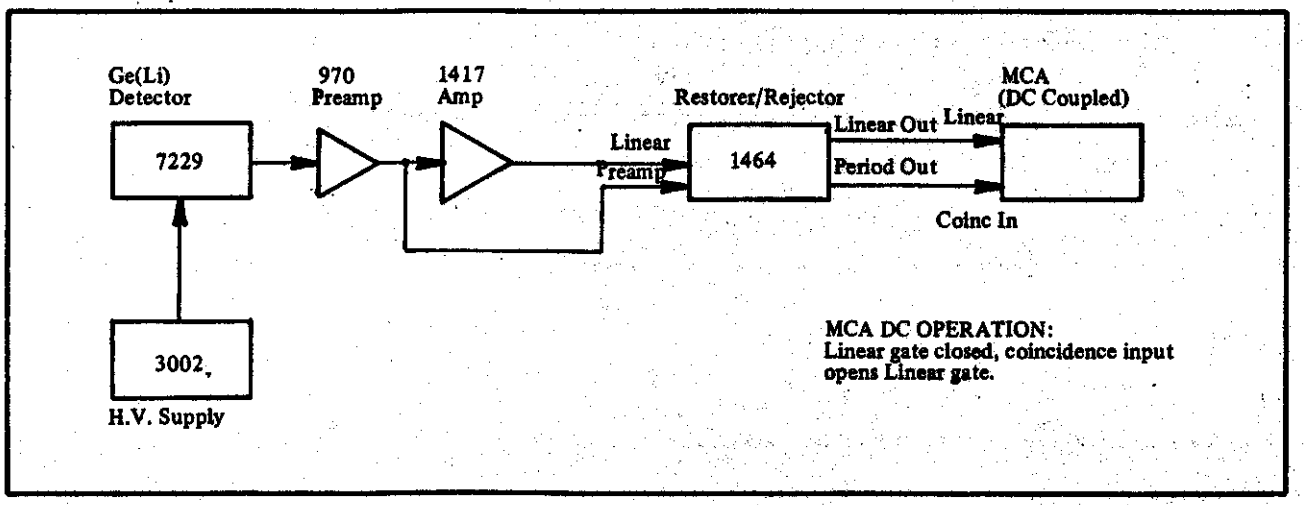
b. When the Model 1464 is operated in the Pileup Rejector Mode, the relatively fast rise time of the Linear output signal will cause spectrum broadening of the energy line width with certain MCA's (such as the HP 100MHz ADC and Northern Scientific Analyzers). By utilizing the PERIOD OUT logic pulse as a coincidence input signal to control the MCA Linear gate, the high resolution capabilities of the Model 1464 can be realized.

SPECIFICATIONS

PERIOD OUT - positive 5.0 volt amplitude logic pulse, width duration essentially the same as the Linear Output signal, Leading edge in time coincidence with Linear Output signal, output impedance 91 ohms series-connected, DC coupled, rear panel BNC connector.

CONNECTIONS

The block diagram below illustrates typical system connections to an MCA.



SECTION 2

SPECIFICATIONS

2.1 INPUTS

PREAMP INPUT

Positive or negative 0-1.5 volt tail pulse from the system preamplifier (via a "tee" connection to the amplifier input)
Maximum rise time: 250 nanoseconds
Minimum fall time constant: 30 microseconds
Input impedance: 1000 ohms, DC coupled

AMP INPUT

Positive 0-10 volt unipolar pulse from a main amplifier; may be AC or DC coupled
Maximum rise time: 5 microseconds
Minimum width: 0.5 microseconds at half-height
Input impedance: 250 ohms, DC restorer coupled

EXT. GATE INPUT

+0.5V to -2V will inhibit output, +4V pulse or greater or open circuit will enable output for duration of gate signal.
Input impedance: 500 ohms at 3.0 volts

2.2 OUTPUTS

SIGNAL OUTPUT

RESTORER ONLY: DC Restored, same as AMP input waveshape
RESTORER/REJECTOR: DC Restored, 2 microsecond wide strobe of AMP input peak
Delay: 2 microseconds
Linear output range: 0-10 volt maximum
Rise time: 200 nanoseconds
Output impedance: less than 1 ohm, DC coupled
Polarity: positive or negative, as selected

REJECT PULSE OUTPUT

Positive 5 volt logic pulse
Width: greater than 50 nanoseconds
Rise time: less than 25 nanoseconds
Output impedance: 25 ohms, DC coupled

TIMING OUTPUT

AEC standard negative 0.8 volt fast logic pulse
Width: 20 nanoseconds
Maximum rise time: 5 nanoseconds
Less than 4 nanoseconds walk for 10:1 input amplitude range

BUSY SIGNAL

Positive 5 volt logic pulse; starts when an input is accepted. Duration equal to twice input signal width plus deadtime selected

2.3 PERFORMANCE

INTEGRAL NONLINEARITY	Less than 0.075% from 0.1 to 10 volt output
GAIN STABILITY	Stability better than 0.01%/°C
DC STABILITY	Stability better than 1mV/°C; better than over 24 hours with constant temperature
NOISE	Less than 0.5mV noise added in quadrature amplifier input signal

Using the Canberra Model 1464, the following typical performance improvement may be expected

	RESOLUTION					
COUNT RATE	WITHOUT 1464		WITH 1464 RESTORER ONLY		WITH RESTORER/REJECT	
	FWHM	FW .1M	FWHM	FW .1M	FWHM	FW .1
2,000cps	2.50keV	4.55keV	2.20keV	4.20keV	2.10keV	4.25ke
10,000	2.65	5.00	2.25	4.35	2.15	4.10
20,000	2.65	5.20	2.40	4.70	2.20	4.10
40,000	3.30	7.50	2.75	5.90	2.55	5.00
80,000	6.20	NA	2.85	6.25	2.60	5.25
100,000	7.50	NA	3.15	10.50	2.60	5.50

Tested with:
Canberra Model 7219 Ge(Li) Coaxial Detector (4.6% eff.)
Canberra Model 1408C Preamplifier
Canberra Model 1417 Amplifier (2 microsecond unipolar shaping)
Source:
Co^{60}: Resolution measured at 1.33MeV

COMPARISON OF PERFORMANCE FOR SPECTROSCOPY SYSTEM WITH AND WITHOUT MODEL 1464

2.4 CONNECTORS

PREAMP INPUT AMP INPUT OUTPUT	Front panel BNC UG-1094/U
REJECT PULSE OUTPUT TIMING OUTPUT BUSY OUTPUT	Rear panel BNC UG-1094/ U

2.5 POWER

+24V – 75mA +12V – 210mA
-24V – 75mA -12V – 210mA

2.6 PHYSICAL

SIZE	Standard dual-width module (2.70 inches wide) TID-20893
WEIGHT	2.2 lb.

SECTION 3

CONTROLS AND CONNECTORS

3.1 FRONT PANEL CONTROLS

SHAPING
Set to the same time constant as that which is set in the amplifier.

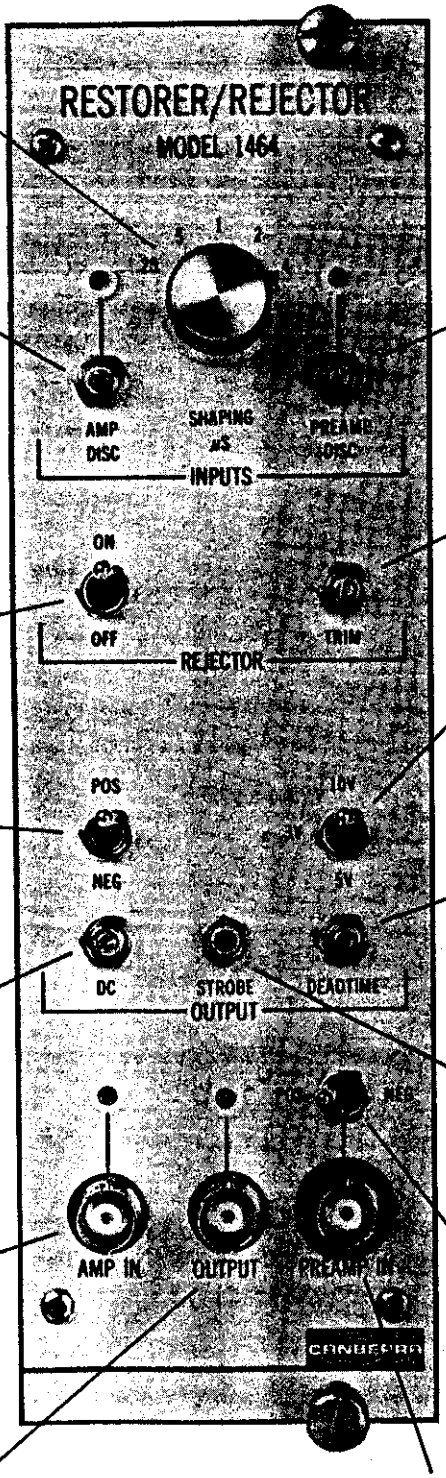
AMP DISC.
Set to a threshold just above the noise in the system. Level is adjustable from less than 10 millivolts to greater than 200 millivolts.

ON/OFF
ON: Rejection is applied to all pulses which pile up and to all pulses which are preceded by a previous pulse occurring in less than the deadtime setting.
OFF: The unit functions as a DC restorer only.

POS/NEG
Set to the desired polarity of the output signal.

DC
Adjust to set the DC level of the output signal from +2 to -2 volts to match the DC level at the input of the DC coupled multichannel analyzer.

AMP IN
Connect a signal from a previous shaping amplifier for DC restoration. Signal must be unipolar positive going, 10 volts maximum and pole/zero compensated. Input impedance is 200 ohms.



PREAMP DISC
When a signal is connected to the PREAMP IN, set this control to the minimum signal level at which the rejector will operate. The level is adjustable from 1 millivolt to greater than 15 millivolts.

TRIM
Set to reject pulses occurring closer than 0.2 microseconds of each other. (Can also be used to reject long rise time detector pulses.)

10V/3V/5V
Set at the maximum OUTPUT signal for a 10V AMP IN signal.

DEADTIME
Set to the minimum time interval required between two pulses before the second pulse is accepted. (Adjustable from 2 to greater than 60 microseconds.)

STROBE
With the REJECTOR ON/OFF switch set at ON, the STROBE control is adjusted to strobe the output signal at its peak.

POS/NEG
Set to the polarity of the preamplifier output signal.

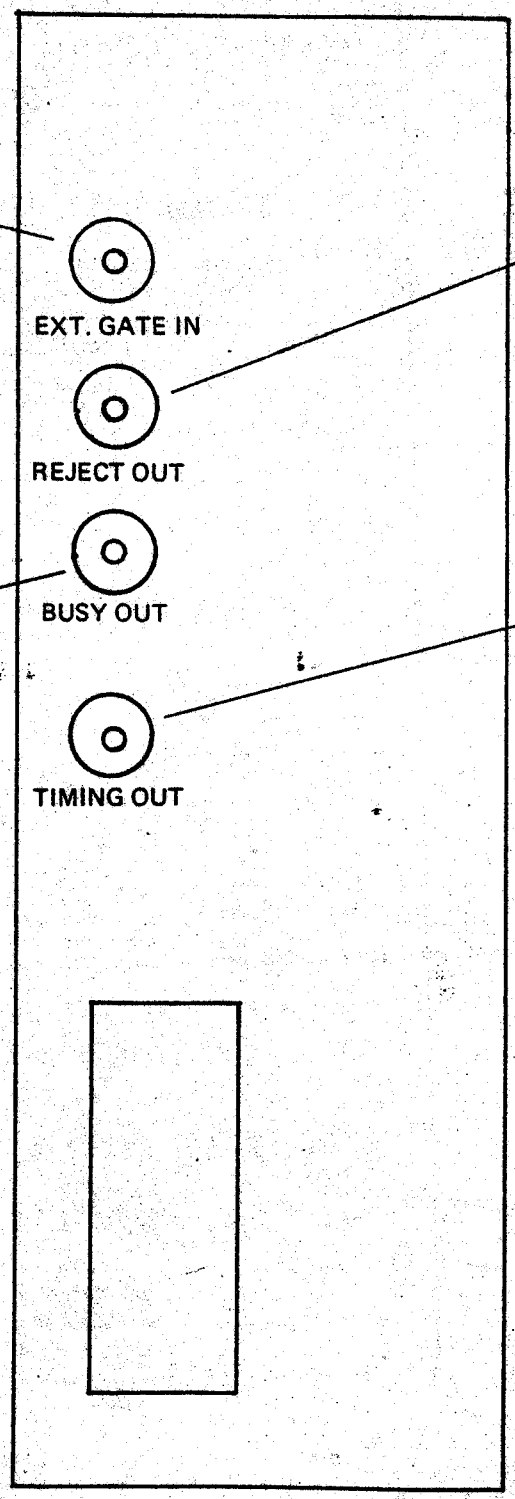
OUTPUT
Provides a signal with the following specifications: DC restored, ±10 volts maximum amplitude into 100 ohms; DC coupled; output impedance is less than 0.1 ohm.

PREAMP IN
Accepts a signal from the system preamplifier. Signal requirements are: Positive or negative 0-1.5 volt tail pulse; maximum rise time, 250 nanoseconds; minimum fall time constant, 30 microseconds; input impedance 1000 ohms, DC coupled.

3.2 REAR PANEL CONNECTORS

EXT. GATE IN
This input accepts an external gating signal for the Restorer/Rejector. Ground or zero volts DC inhibits the restorer; +3 volts or greater (or open circuit) enables the restorer. The gating signal requirements are: INHIBIT, +0.5 to -2 volts; ENABLE, +4 volts or open circuit. The input impedance is 500 ohms at +3 volts.

BUSY OUT
A +5 volt logic pulse with a duration of the deadtime selected plus twice the amplifier input pulse width occurs at this connector each time an amplifier input is accepted.



REJECT OUT
A +5 volt logic pulse occurs at this connector each time an input signal either causes pile-up rejection or occurs during the dead time. The output pulse width is greater than 50 nanoseconds.

TIMING OUT
A standard AEC fast logic pulse occurs at this connector whenever an input signal is received at the PREAMP input. The pulse pair resolving time is 200 nanoseconds plus the rise time of the input signal.

SECTION 4

OPERATING INSTRUCTIONS

4.1 GENERAL

The purpose of this section is to familiarize the user with the controls of the Model 1464 Baseline Restorer/Pileup Rejector so that the best performance can be obtained.

4.2 SETUP

1. Insert the module in an AEC compatible base unit/power supply such as the Canberra Model 1400. Turn on the power switch.

2. Connect the unipolar prompt output from a pulse shaping main amplifier, such as a Canberra Model 1416 or Model 1417, to the AMP IN connector of the Model 1464.

3. Using a BNC "tee", connect the preamplifier signal at the input of the shaping amplifier to the PREAMP IN connector of the Model 1464. Set the polarity switch above the connector to the polarity of the preamplifier signal.

4. Set the controls of the Model 1464 as follows:

INPUTS

AMP DISC:Fully counterclockwise.
PREAMP DISC:Fully counterclockwise.
SHAPING:To the same time constant as the main amplifier.

REJECTOR

ON/OFF:OFF.
TRIM:Fully clockwise.

OUTPUT

POS/NEG:POS.
DC:Leave at factory adjustment.
STROBE:Fully counterclockwise.
DEADTIME:Fully counterclockwise.
10V/3V/5V:10V.

5. Use a "live" source. Adjust the main amplifier output to 10 volts, or less.

6. Connect the OUTPUT of Model 1464 to the B input of the oscilloscope.

4.3 INITIAL CHECKOUT

1. Connect an oscilloscope probe (A input) to the test point at AMP IN. Observe the output of the shaping amplifier; set the oscilloscope for 0.1V sensitivity and 50 usec./cm. sweep. Adjust Pole/Zero compensation of the shaping amplifier for correct compensation.

2. Connect the oscilloscope probe (A input) to the test point labelled AMP DISC. Observe a negative pulse of 3 to 4 volts. (See Figure 4-1a.)

Slowly rotate the AMP DISC control clockwise. Notice that the AMP DISC pulses broaden; continue rotation until AMP DISC pulses get very narrow and an output baseline appears (see Figure 4-1b). This indicates that the DISC level is too low. Back off on the DISC level control until the output baseline disappears and only negative pulses are seen. (See Figure 4-1c.)

Signal waveshapes at the OUTPUT test point will now be as shown in Figure 4-1d.

3. Connect the oscilloscope probe (A input) to the test point labelled PREAMP DISC. Adjust the oscilloscope sensitivity for 0.5V/cm. and the sweep for 0.1 usec/cm. Observe a positive-going pulse approximately 0.4 usec long (see Figure 4-2a). Turn the PREAMP DISC control clockwise until noise pulses are observed (see Figure 4-2b) then back off on the control until only peak noise pulses are seen (see Figure 4-2c).

Internal to the Model 1464 is a switch for altering the gain of the amplifier in the preamplifier discriminator circuit. This is normally set for maximum gain. If, when observing the preamplifier discriminator output, the appearance is as shown in Figure 4-2b with the DISC control fully counterclockwise, the gain switch should be shifted to its low position (or the preamplifier gain reduced if this is possible). Access to the internal gain control is obtained by removing the right side cover of the Model 1464 and changing the switch located at the bottom left of the unit to the up position (see Figure 4-3).

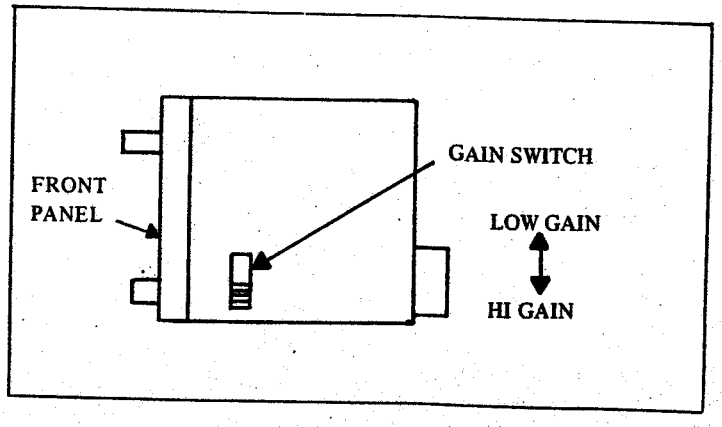


FIGURE 4-3. LOCATION OF GAIN SWITCH

4. Display the OUTPUT signal on the oscilloscope (time scale of 1 usec/cm). With REJECTOR switch at ON, observe that the output width is now only 2 microseconds and is located at the leading edge of the waveform. Turn the STROBE control clockwise until the output pulse is centered on the peak of the output waveform.

5. Turn the REJECTOR TRIM control counterclockwise until the output pulse begins to disappear, then back off slightly. This sets the rejection of long rise time pulses and rejection of pulse pairs.

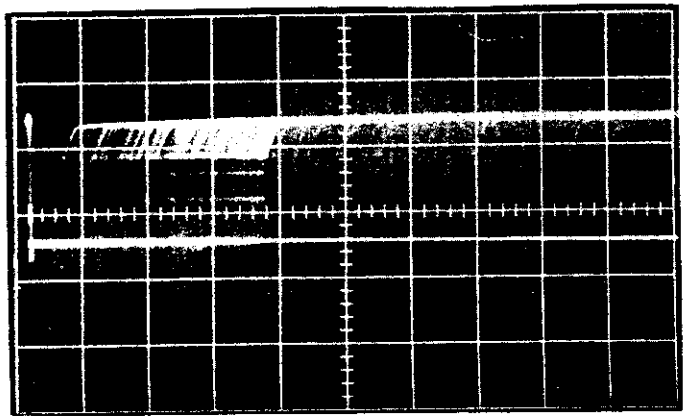


FIGURE 4-1a. DISC control fully counterclockwise. (AMP DISC TEST POINT.)

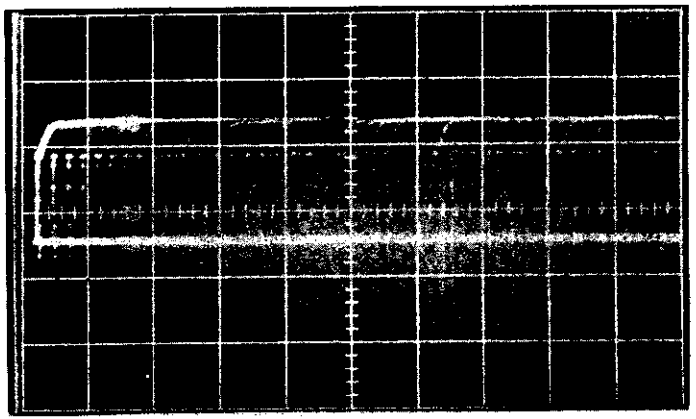


FIGURE 4-1b. DISC control too far clockwise–Note width of discriminator pulses has narrowed. (AMP DISC TEST POINT.)

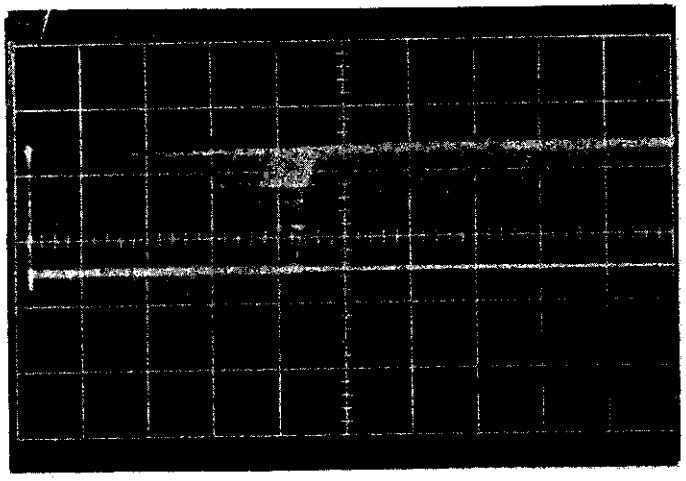


FIGURE 4-1c. DISC control setting correct. (AMP DISC TEST POINT.)

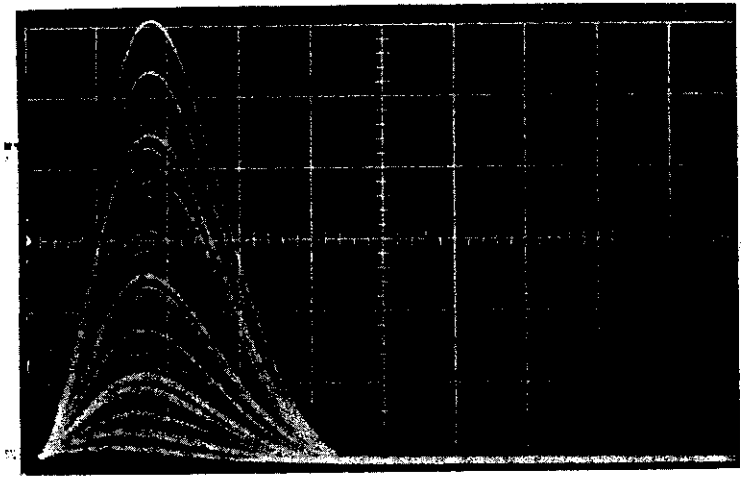


FIGURE 4-1d. Signal output. DISC control setting correct. (Co^{60} 2V/cm).

FIGURE 4-1. Results of various DISC control settings.

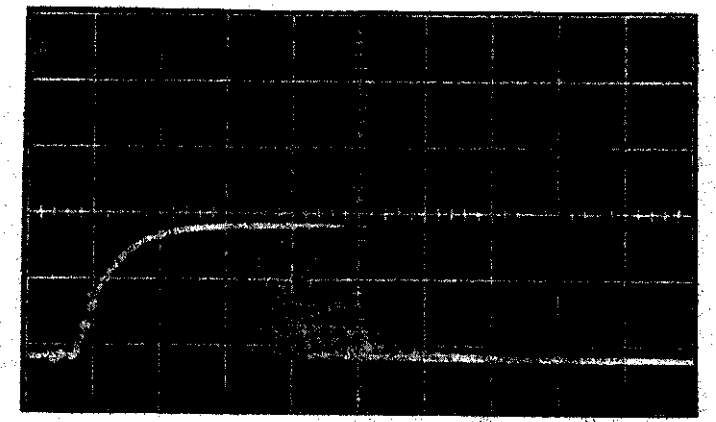


FIGURE 4-2a. DISC control fully counterclockwise.

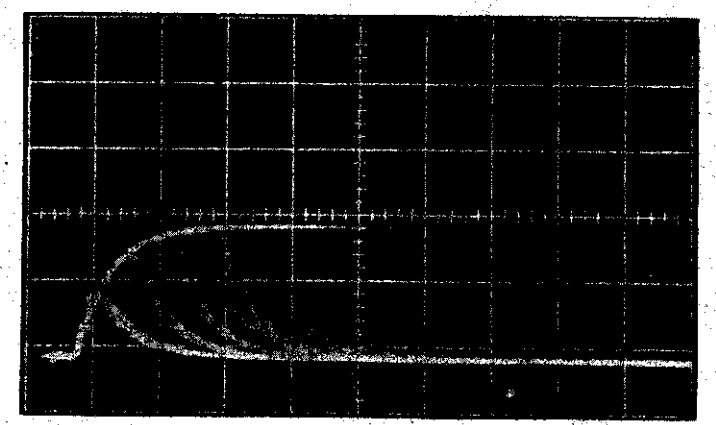


FIGURE 4-2b. DISC control too far clockwise.

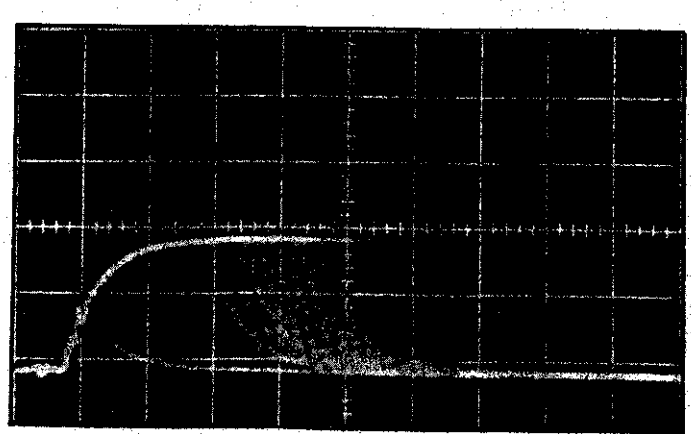


FIGURE 4-2c. Correct setting of DISC control. (Note small amplitude triggers due to noise).

FIGURE 4-2. PREAMP DISC settings–Preamp Disc test point. (Vert. 0.5V/cm. Horiz. 0.1 microsecond/cm.) Cs^{137} source.

6. Set the time scale of the oscilloscope to 5 usec/cm: observe the OUTPUT. Note the time between the first pulse and when the pulses start reappearing. This is the Busy Time of the Model 1464. Turn the DEADTIME control clockwise and note the lengthening of the Busy Time. Busy Time is the sum of the delay time, pulse width, clamp time and DEADTIME selected.

7. Connect the output of the Model 1464 to a multichannel analyzer. Use DC coupling; this is important. Use the output POLARITY switch, the OUTPUT VOLTAGE selector and DC level control to match the requirements of the analyzer. Use the Model 1464 as a Restorer or Restorer/Rejector by using the REJECTOR ON/OFF switch.

All decisions for rejection are made by the signal at the PREAMP IN connector. If the PREAMP IN connector is not used, the REJECTOR ON/OFF switch must be in the OFF position and the DEADTIME control set fully counterclockwise. The 1464 will then be a DC Restorer only.

4.4 EXTERNAL GATING

To be able to gate the 1464, the external gating signal must begin less than 1 microsecond after the peak of the amplifier input signal and last for at least 2.5 microseconds . A positive going pulse 4 volts or greater (or open circuit) is required to enable the output, starting from a quiescent level between +0.5 and -2 volts, at a current of -4 milliamps.

If the Restorer/Rejector is-used then the output signal will be two microseconds wide. The gate signal must have sufficient width to "bracket" this width. (See Figure 4-4.)

If the DC restorer is used alone, the output signal will be the width of the enabling gate signal, which should be centered on the output pulses by changing the delay of the gate signal. (See Figure 4-5.)

4.5 BUSY SIGNAL

The busy signal is a +5 volt pulse during the Busy time and a -0.7 volt DC level during quiescent periods. It is capable of supplying 10 milliamps in the high state and 1 milliamp in the low state. A one milliamp meter connected to this output will provide the user with an indication of %, the percentage of total deadtime. Alternatively, this output may be suitably interfaced to an analyzer "live time" counting circuit to provide live time counting which allows for both analyzer and Restorer/Rejector dead times.

The Busy signal period is shown in Figure 4-6 and 4-7 for both the Restorer only and Restorer/Rejector modes. The deadtime part of this signal is always updated if a new pulse is received during the DEADTIME period.

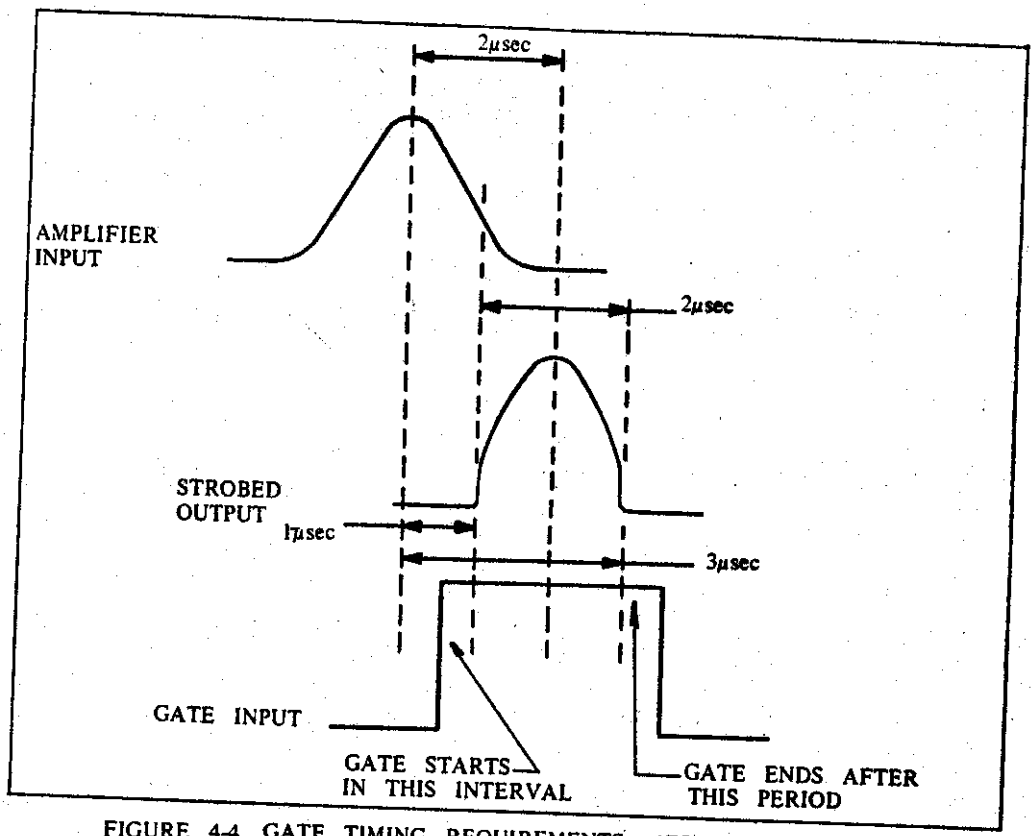


FIGURE 4-4. GATE TIMING REQUIREMENTS, RESTORER/REJECTOR

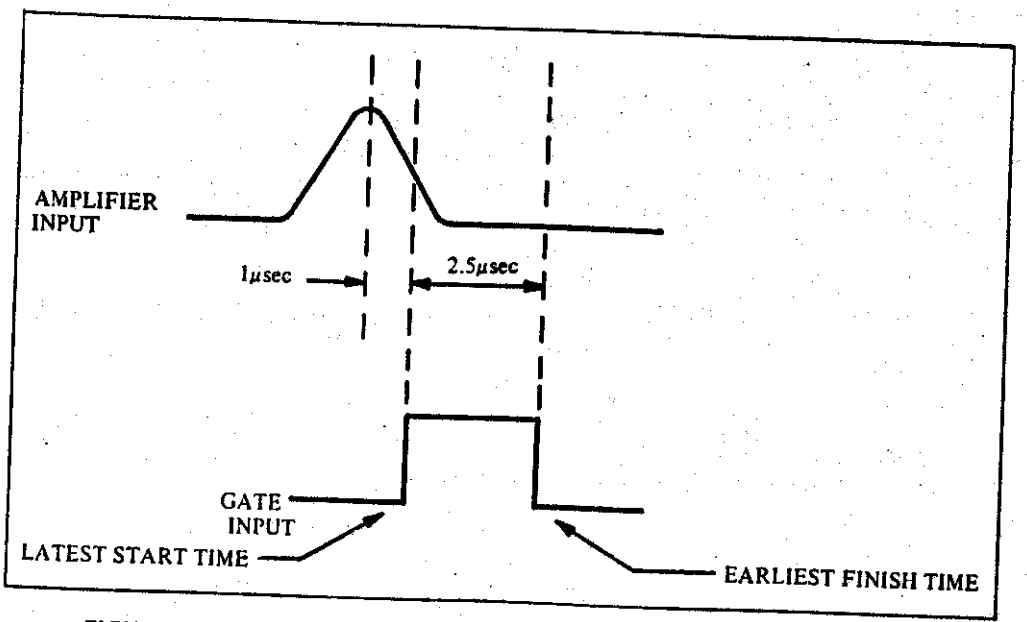


FIGURE 4-5. GATE TIMING REQUIREMENTS, RESTORE ONLY MODE

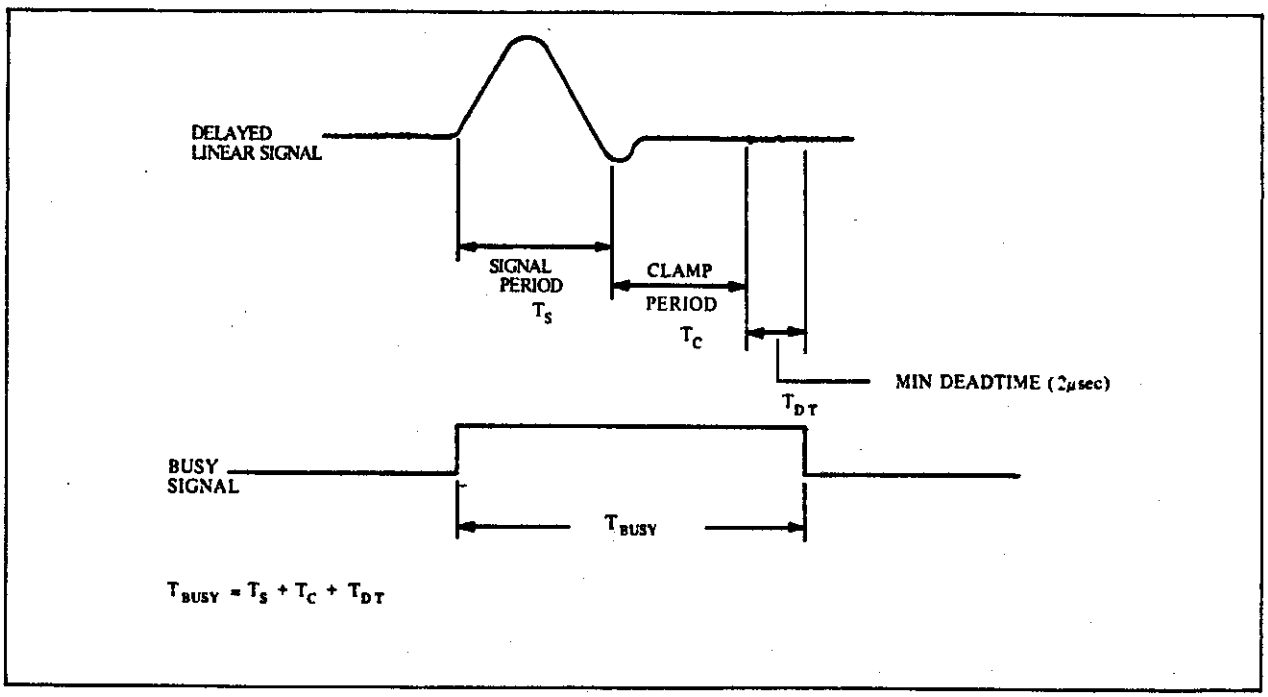


FIGURE 4-6. RESTORER MODE BUSY SIGNAL TIME

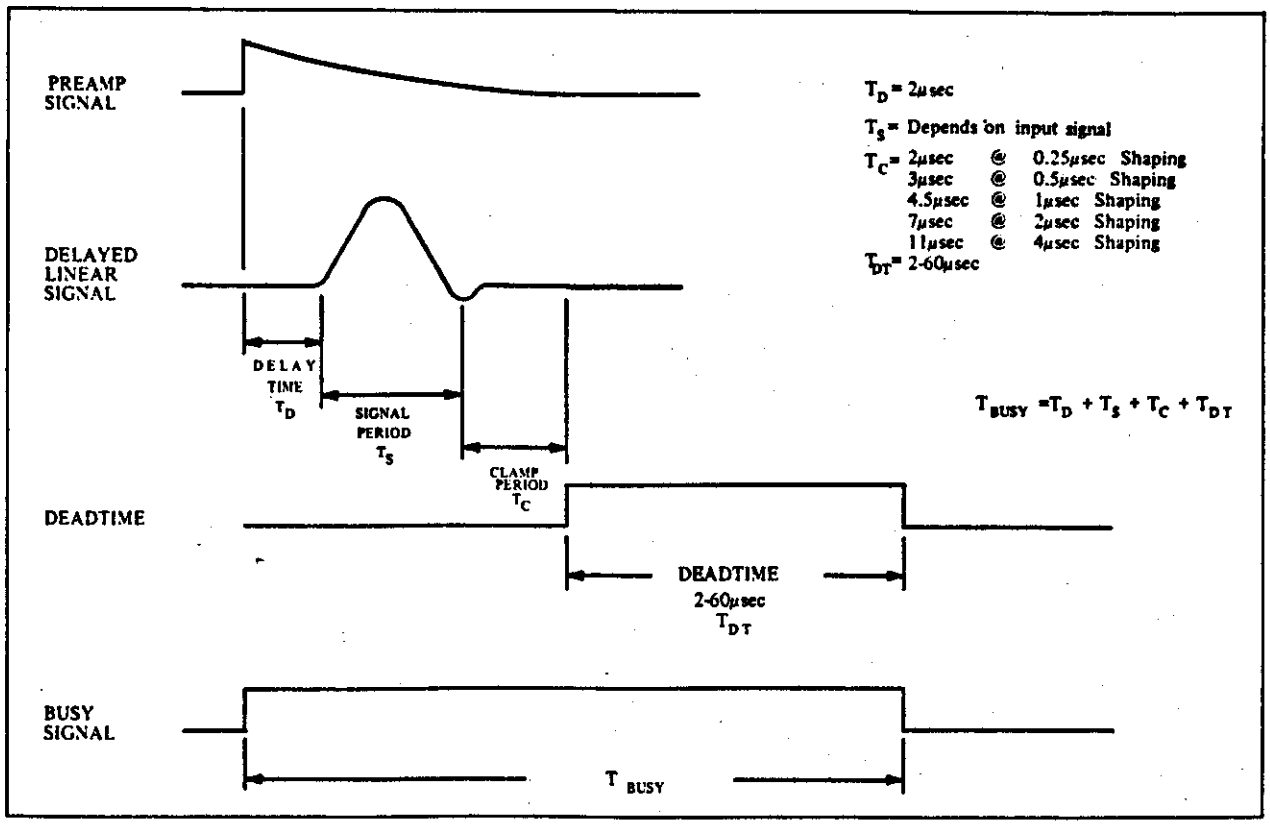


FIGURE 4-7. RESTORER/REJECTOR MODE BUSY SIGNAL

SECTION 5

THEORY OF OPERATION

5.1 GENERAL

Drawings D11995 (sheets 1 through 3) are used in the following discussions. D11995 (1) is the block diagram of the Model 1464; D11995 (2) is the Restorer section; D11995 (3) is the Rejector section. Paragraphs 5.1.1 and 5.1.2 use drawing D11995 (1).

5.1.1 RESTORER

The buffer amplifier (Q1-Q6) accepts a linear input signal (AMP IN), delayed by L1 for 2 microseconds and provides a low impedance drive to the restorer capacitors and voltage controlled resistor (VCR, Q7). DC restoration is accomplished by clamping the input to ground for a brief period following the linear input signal.

After DC restoration, a buffer amplifier (Q10 through Q16) drives the linear gate (Q17 through Q20), followed by the output driver (Q21 through Q28). Output signals are obtained only when the linear gate is open. The gate is opened during a linear input signal. This will be true if there is a strobe signal or if the rejector is off, and if the external gate is enabled and the restorer is not clamped. The amplifier discriminator (A1) fires when the input signal exceeds the discriminator threshold causing the VCR impedance to go high (through the VCR driver, Q8 and transistor Q9), and enabling the linear gate by opening the gate time flip-flop (Q31 and A2C).

At the end of the input signal period, the clamp monostable (Q32 through Q34) generates a clamp signal which causes the VCR (through A2B) to go to a low impedance. The clamp signal also closes the gate time flip-flop. The gate time flip-flop cannot be reopened while a clamp signal is present, therefore, any input signal occurring during the clamp time cannot enable the linear gate.

5.1.2 REJECTOR

The preamplifier signal (PREAMP IN) is amplified and shaped through a 0.2 microsecond delay line and amplifiers Q35 through Q37, Q38 through Q41, and Q42 through Q44. The resulting 0.2 microsecond wide unipolar signal causes the tunnel diode discriminator to produce a negative-going pulse, 0.2 microseconds wide.

The tunnel diode (TD) pulses are applied to the width discriminator (A3 and A4A) which produces an output only if the TD pulses are wider than 60 nanoseconds. Noise pulses in the tunnel diode discriminator have a width of less than 50 nanoseconds. Therefore, noise pulses are rejected but signal pulses are accepted. The output of the width discriminator generates TIMING OUT signals (through Q48-Q49) and triggers the trim monostable (Q50-A5A).

The trim monostable fires the dead time (Q51-A8) and strobe delay (Q54-A5B) monostables. The output of the strobe delay monostable is OR'd with the restorer discriminator (A2A) and provides early opening of the VCR.

The outputs of the deadtime monostable, trim monostable, and tunnel diode discriminator are AND'd at A4B. A REJECT OUT signal is generated (at the rear panel) if a preamplifier signal is received during the deadtime or if the input has a rise time longer than that determined by the TRIM control.

The strobe delay monostable sets the strobe flip-flop (A6A). If the flip-flop is still in its set condition at the end of the strobe delay, the strobe signal (from Q57-A7B) is enabled through A5C. Thus, the linear gate in the Restorer section is opened (through D43) and the strobe flip-flop is reset. If a REJECT OUTPUT occurs during the strobe delay time, the strobe flip-flop is reset, inhibiting the strobe signal.

5.2 CIRCUIT DESCRIPTIONS, RESTORER SECTION

The Model 1464 Restorer is described in detail by the following subsections:

5.2.1 Signal Amplifiers
5.2.2 Restorer and Voltage Controlled Resistor
5.2.3 Linear Signal Discriminator and Restorer Control Signals
5.2.4 Linear Gate and Gate Driving circuits

Refer to schematic drawing D11995 (2) for the Restorer circuitry.

5.2.1 SIGNAL AMPLIFIERS

There are three buffer amplifiers which are built around the basic amplifier loop shown in Figure 5-1. The input differential dual transistor (Q1) has equal collector currents and voltages for maximum temperature stability. Q2 is a voltage level translator and an impedance load for signal currents driving the complementary output transistors (Q3 and Q4).

The delay buffer amplifier (Q1 through Q6) compensates for the voltage loss in the 2 microsecond delay line (DL1) at the input. Temperature compensation of the delay line is provided by means of resistor R6. Q2 and Q4 are the constant current sources for the input differential transistor pair (Q1) and level translator (Q3). C6 is a high frequency stabilizing capacitor. Diodes D1 and D5 provide output voltage limiting before saturation of any transistor in the loop.

The Restorer buffer amplifier (Q10 through Q16) adds an FET dual transistor pair (Q10) to provide high input impedance. Since the DC stability of this and the output loops is critical, the constant current sources (Q14 and Q15) are temperature compensated by D16 and D17.

The output driver amplifier (Q21 through Q28) adds two transistors (Q25 and Q28) to provide high current driving of a 100 ohm load and still maintain the high impedance at the collector of Q26. Diodes D22-D25 compensate for the output transistor base emitter voltage drops.

5.2.2 RESTORER AND VOLTAGE CONTROLLED RESISTOR (VCR)

Q7 (FET) is a voltage controlled resistor. With no signal input the FET is adjusted by RV-5 to provide an impedance from drain to ground of 7K to 9K ohms. C11 through C15 in conjunction with the impedance of the FET provide a time constant of 10 to 15 times the amplifier input shaping time constant (when the SHAPING switch, S1a, is selected to match the signal time constant).

Q9 provides the current which controls the gate of Q7. With no amplifier input signal the voltage at A2A-3 is zero. A2B-6 is +3V. R31 and R36 in the emitter circuit of Q9 provide an impedance of 1.75K ohms from a voltage of +3V. With R32 returned to zero volts, the base of Q9 is at 1.7 volts, providing a collector current in Q9 of 0.6 milliamps. The current through R34 is adjusted by RV-5 to produce approximately -3 volts at the gate of Q7.

When a signal is received, A2A-3 goes positive, causing the base of Q9 to go to +3 volts and cutting off Q9. With no voltage drop across R34, the gate of Q7 goes to -6 volts cutting off Q7 and providing a high impedance to coupling capacitors C11 through C15. When a signal is present the coupling capacitors are charged only by the parallel input impedance of Q10 and R40 which is greater than 50 megohms.

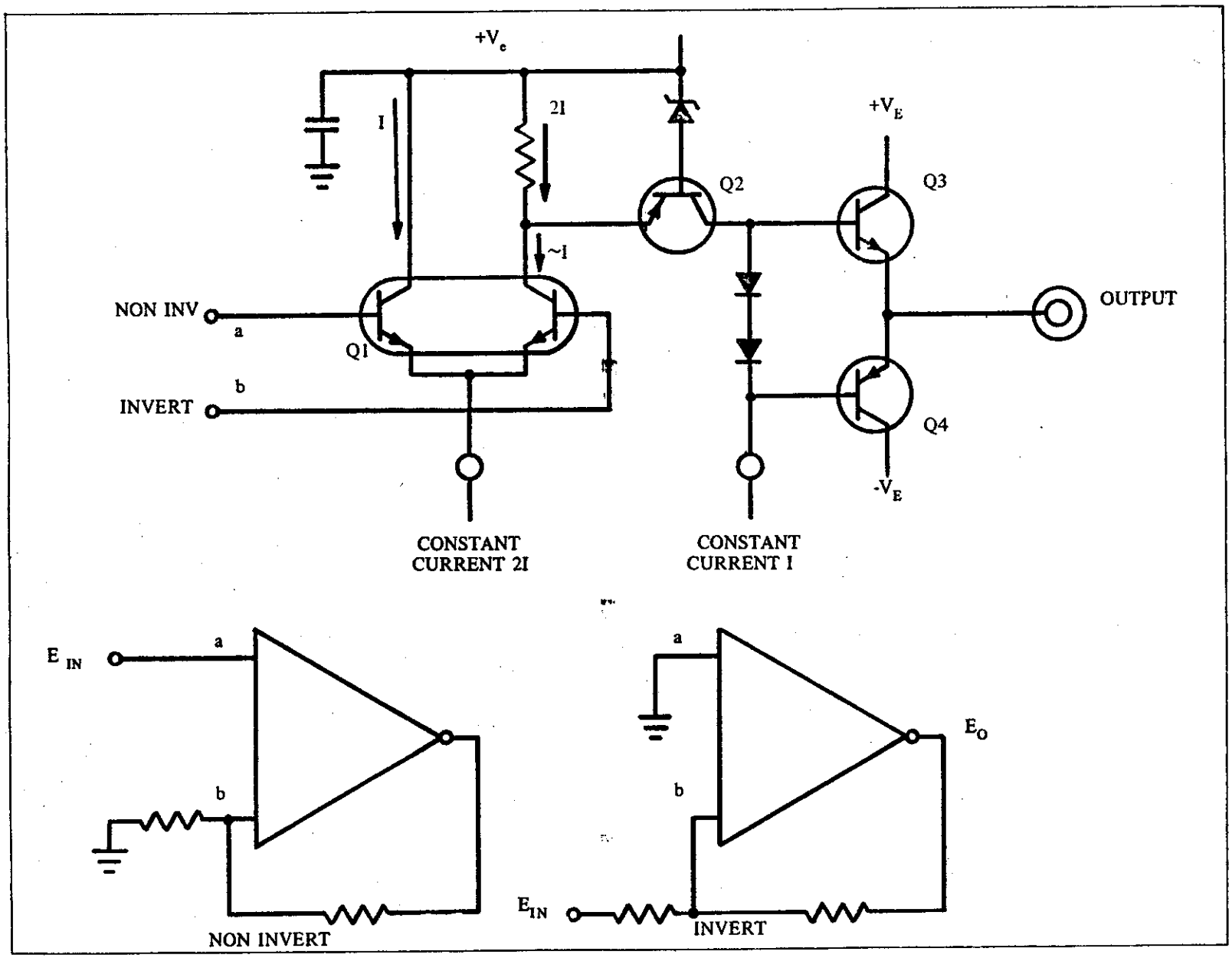


FIGURE 5-1. BASIC AMPLIFIER LOOP

At the end of the input signal duration, A2A-3 goes to zero. The clamp signal (see Section 5.2.3) causes A2B-6 to go to zero, grounding the base of Q9 through D9. This results in a collector current of 1.5 milliamps, turning Q7 ON. The coupling capacitor is then discharged through the ON resistance (approximately 80 ohms) of Q7 and R33. This restores the DC level at Q10 and discharges the coupling capacitor. At the end of the clamp time, A2B-6 goes high, and the circuit returns to its normal operating condition.

The voltage at Q7 gate is also applied to the base of inverter Q8. The inverter couples the gate voltage to the drain of the FET through C16. This compensates the gate/drain capacity of the FET and prevents switching spikes from appearing on the signal. RV-4 provides adjustment for exact compensation.

5.2.3 LINEAR SIGNAL DISCRIMINATOR AND RESTORER CONTROL SIGNALS

The signal discriminator (A1) produces a positive output whenever the input exceeds the bias level set by RV-9 (AMP DISC). The input is derived from the sum of the restored and non-restored signals. This ensures that a new input occurring during the clamp time of the restored signal will fire the discriminator to prevent clamping during a signal. R97 provides feedback hysteresis for preventing multiple noise triggering. Q29 and C44 stretch the output by 0.3 microseconds to allow time for the input signal to go to zero. A2D provides signal inversion.

The negative discriminator signal from A2D is applied to NAND gate A2A-2. With the Rejector OFF, A2A-1 is positive; the signal applied to the VCR circuit lasts for the duration of the input signal. If the Rejector is ON, A2A-1 goes negative 2 microseconds before the signal is seen at the Discriminator. Thus, the VCR is switched to its high impedance state before the signal occurs and nonlinearity at low signal amplitudes is avoided.

The clamp signal for the VCR circuit comes from the monostable made up of Q32-Q34. The positive-going trailing edge of the inverted discriminator signal is differentiated by C47 and R114, inverted by Q34, and applied as a trigger to the base of Q32. The output of Q32 is a positive pulse which clamps Q33 ON. Q33 stays ON until Q32 begins to conduct. Q32 conducts after C46 has discharged through the resistors (R102-R106) selected by the SHAPING switch. At this time, the circuit resets awaiting a new trigger signal.

The time duration of the clamp signal determined by the SHAPING switch setting is automatically set for approximately 75% of the normal width of the input signal. The positive clamp signal (at the collector Q32) is applied to NAND gate A2B-5; the other input, A2B-4, is the output of the discriminator (through A2D). Since the discriminator output has ended, A2B-4 is positive, and A2B-6 output goes negative providing the clamp signal to the VCR. If another linear input signal appears during the clamp time, A2B-4 goes negative, generating a positive output and removing the clamp signal from the VCR. At the same time the clamp monostable is reset by diode D34.

5.2.4 LINEAR GATE AND GATE DRIVING CIRCUITS

The linear gate is made up of transistors Q17 through Q20 (shown simplified in Figure 5-2). When the gate control signal is positive all transistors are saturated. The input signal to the operational amplifier is attenuated by 1000:1, or greater, by resistors Rc and Rb and the ON resistance of the transistors. Resistors Ra and Ri/Rf ensure common mode balance.

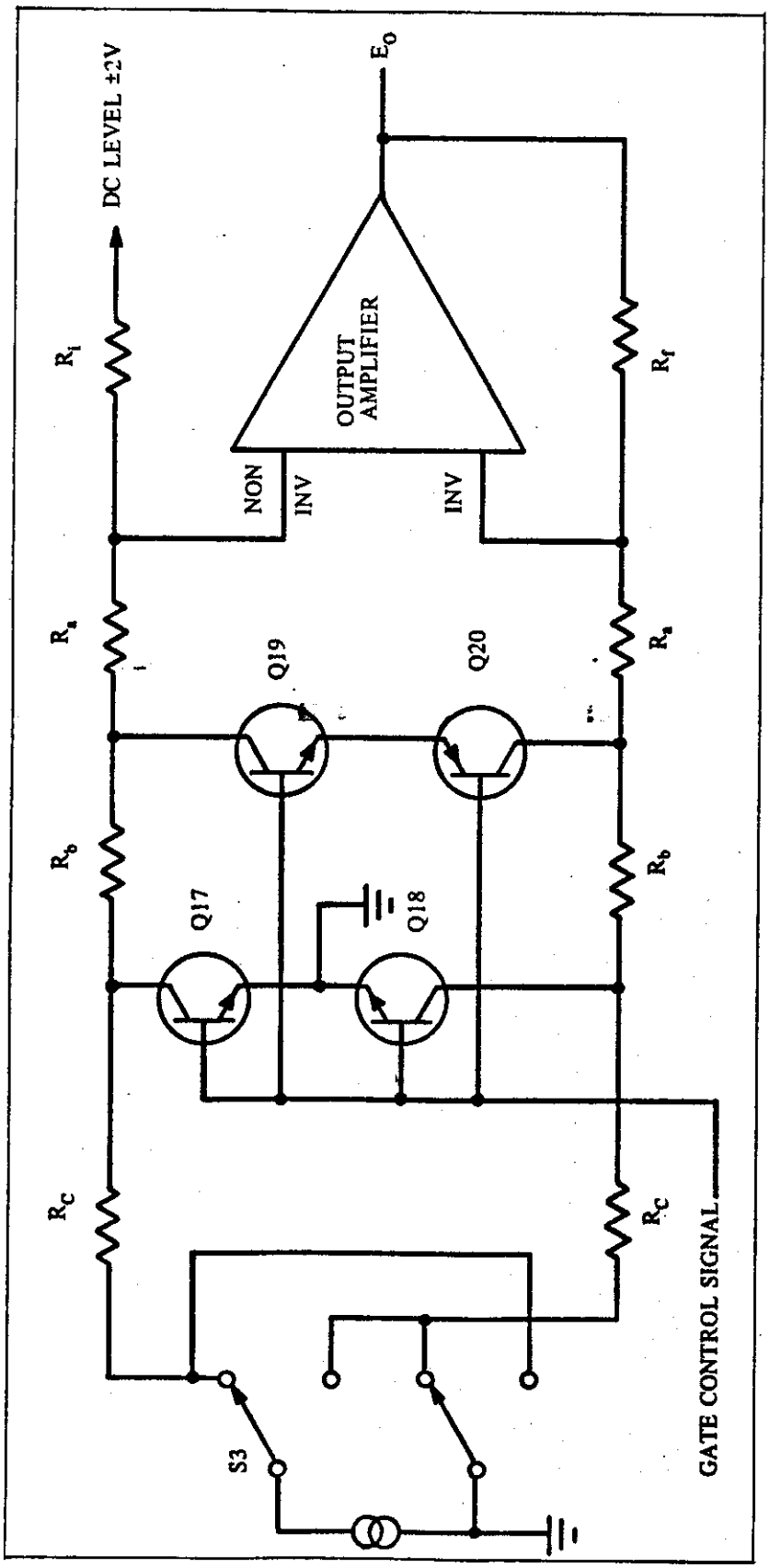


FIGURE 5-2. LINEAR GATE, SIMPLIFIED

If the gate control signal goes to ground, the transistors are turned OFF: with positive inputs. the output signal can be made positive or negative by the OUTPUT POLARITY switch (S3). The input to the amplifier is still balanced by Rc and Rb, therefore there is no gate pedestal and the gain remains the same for both positive and negative outputs.

In the actual gate the transistors are driven through equalizing resistors R60-R63 (see schematic D11995 (2)). RV-7 provides adjustment to equalize the saturation voltage of Q19 and Q20. R55 through R58 change the overall gain of the circuit to limit the output voltage range. The DC level of the output, controlled by RV-8, has only a second order effect on the common mode balance.

The linear gate drive is from the diode AND circuit consisting of D43, D41, and D39. With the Rejector OFF, D41 is grounded through D40. With no EXT GATE IN signal, Q30 is ON thus grounding D43. When all inputs to diodes D43, D41, and D39 are at ground the bases of Q17-Q20 go to -0.5 volts (by R123) and the gate is opened. The gate is closed until a signal is received because D39 is positive due to the state of the gate time flip-flop.

The current from R118 through D39 is sufficient to supply base current to all gate transistors (Q17 through Q20) through the equalizing resistors. Gate switching transients are very low (under 20 millivolts) because of the balanced nature of the gate. CV-1 provides adjustment for variations in stray capacity.

Q31 in the gate time flip-flop (Q31 and A2C) is normally OFF due to the emitter diode D38 (A2C-8 is low). The negative discriminator signal, differentiated by C48, R120, sets A2C to the 1 state. R121 couples to the base of Q31, switching it ON. The potential at D39 is brought close to ground, opening the linear gate, and holding A2C in the 1 state. At the end of the discriminator signal period, the clamp signal from A2B-6 grounds the base of Q31. This turns Q31 OFF and returns the flip-flop to its normal state, thus closing the linear gate.

If a second input signal should occur during the clamp time, the flip-flop is prevented from retriggering since Q31 is still held OFF until C49 recharges through R115. A signal input must occur 1 microsecond later than the end of the clamp time for the gate to open. This prevents the clamping time constant from modifying the output signal pulses.

5.3 CIRCUIT DESCRIPTIONS, REJECTOR SECTION

The Model 1464 Rejector circuits are covered in detail by the following descriptions:

5.3.1 Preamplifier Signal Shaping
5.3.2 Tunnel Diode Discriminator
5.3.3 Width Discriminator and Timing Output
5.3.4 Reject Selection Circuits
5.3.5 Strobe and Strobe Delay

Refer to schematic D11995 (3) for the Rejector circuits.

5.3.1 PREAMPLIFIER SIGNAL SHAPING

The preamplifier input signal passes through a three-stage inverting/non-inverting buffer amplifier (Q35-Q37). This provides a standardized positive-going signal at its output. The internal INPUT RANGE switch (S5) provides for unity gain or a gain of 2. The setting selected is determined by the noise level of the preamplifier. Normally, a gain of 2 is used, unless the preamplifier noise level is high enough to prevent correct setting of the PREAMP DISC control.

The operational amplifier (Q38 through Q41) has a gain of 5. The non-inverting input (Q38 base) is fed directly from the buffer amplifier; the inverting input (Q38 emitter) through a 0.2 microsecond delay line. The resulting output (TP6) is a 0.2 microsecond wide pulse which contains the rise time information of the original signal.

RV-1 adjusts for monotonic return to the baseline. It is preset for a 50 microsecond decay time and normally need not be adjusted as long as the preamplifier decay time is within a range of 40 to 100 microseconds.

After unipolar shaping, differentiation occurs and is accomplished by C62, R157, and D50 equalizing the return to zero time for large input signals. D51 clamps the undershoot to 0.1 volt with a very fast recovery.

5.3.2 TUNNEL DIODE DISCRIMINATOR

Q43 and Q44 form an emitter coupled pair which provides a current pulse to the tunnel diode (D52). The load line of the tunnel diode is set by RV-2 and the trigger point by RV-10 (PREAMP DISC). As soon as the current of the tunnel diode passes the peak point it switches to its high voltage state. L2 provides the current to charge the circuit capacities. When D52 goes high Q45 conducts, producing a negative 2.5 volt pulse at its collector to drive the pulse width discriminator.

At the end of the input signal duration, D52 returns to its low voltage state. If a noise signal turns D52 ON, the time constant of L2 and the circuit capacities provide an output pulse less than 50 nanoseconds wide.

5.3.3 PULSE WIDTH DISCRIMINATOR AND TIMING OUTPUT

The pulse width discriminator (A3 and A4) is made of MECL II logic units. These are negative input NAND gates with logic 0 at -1.5 volts and logic 1 at -0.75 volts. All inputs to the gates must be at logic 0 for a logic 1 output. (The A4 gates have complementary outputs.)

The output from the tunnel diode discriminator is level shifted by R171 and delayed 55 nanoseconds by DL3. Both the delayed and undelayed pulses are used in the pulse width discriminator. These pulses combine in A3A and A3C and provide a 50 nanosecond wide pulse, regardless of the input width, to set A3B to logic 0.

The delayed and undelayed discriminator signals are combined in A4A. These inputs are all at logic 0 only when the discriminator output is greater than 60 nanoseconds. The delayed input is the last to go to logic 0 at which time the outputs of A4 change state. The logic 1 output reverses the state of flip-flop A3C and A3B after a delay of 20 microseconds due to C75. As soon as A3B goes to logic 1, the outputs of A4 revert to normal. This results in a 25 nanosecond wide pulse coupled to the differential pair Q48 and Q49. The output of Q48 produces the NIM standard negative logic pulse TIMING OUTPUT.

If the discriminator pulse is due to noise, it is only 50 nanoseconds wide. A4A thus never sees all inputs at logic 0, therefore there is no TIMING OUT pulse.

5.3.4 REJECT SELECTION CIRCUITS

Any timing pulse triggers the trim monostable (Q50 and A5A). The positive pulse at Q50 collector is adjusted in width by the front panel TRIM control so it is just wider than a normal discriminator pulse. When Q50 goes positive, the Busy Time circuit (Q51-A8) is activated and the output of A8 goes

to zero volts. The outputs of Q50 and A8 are level shifted by R190 through R193 to provide inputs (with the discriminator pulses) to A4B.

Assuming a preamplifier input signal pulse is present, the two discriminator pulses go to logic 0, the trim pulse goes to logic 1 and the busy time pulse goes to logic 0. There are no logic 0's occurring at the same time, therefore, A4B does not change state.

If the preamplifier pulse has a long rise time the discriminator pulse widens and remains at logic 0 when the Trim pulse returns to logic 0. All inputs to A4B are now logic 0; an output occurs at A4B. If a second preamplifier pulse occurs before the end of the busy time, the discriminator pulses go to logic 0 before the Trim goes to logic 1, resulting in the change of state of A4B.

When A4B changes state, the differential transistor pair (Q55-Q56) provides a negative output from Q56. This negative output triggers the rejector monostable (Q58-A7C) and resets the A6 (A-C) flip-flop. The REJECT OUT pulse is buffered by the emitter follower Q60.

The BUSY OUT circuit uses comparator A8. Q51 is normally OFF and the non-inverting input A8-2 is higher than the inverting input A8-3. A8 output is +2.5 volts. A trim signal switches Q51 on, discharging C80 to ground. A8-3 is kept positive by R203, R204. The output of A8 goes to zero. When the input signal ends, Q51 goes off; C80 charges through R201 and RV-12 (DEADTIME width) toward 24 volts.

As soon as the voltage across C80 exceeds A8-3, the output of A8 reverts to +2.5 volts. If a new input is received during the time C80 is charging (DEADTIME), C80 is immediately discharged by Q51 thereby continuously updating the deadtime.

At minimum deadtime A8-3 is at 0.5 volts. C80 charges rapidly through R201. At maximum deadtime, A8-3 is at 5.5 volts and C80 charges slowly through R201 and RV-12 providing a wide range of deadtime adjustment. D59 prevents the input to A8-2 from exceeding 6.5 volts.

Q51 base is driven by the trim pulse (through D58) and by the linear signal discriminator (Restorer Section) through R196, D33 and D32. BUSY OUT is the sum of the signal widths and deadtime buffered by Q52 and Q53.

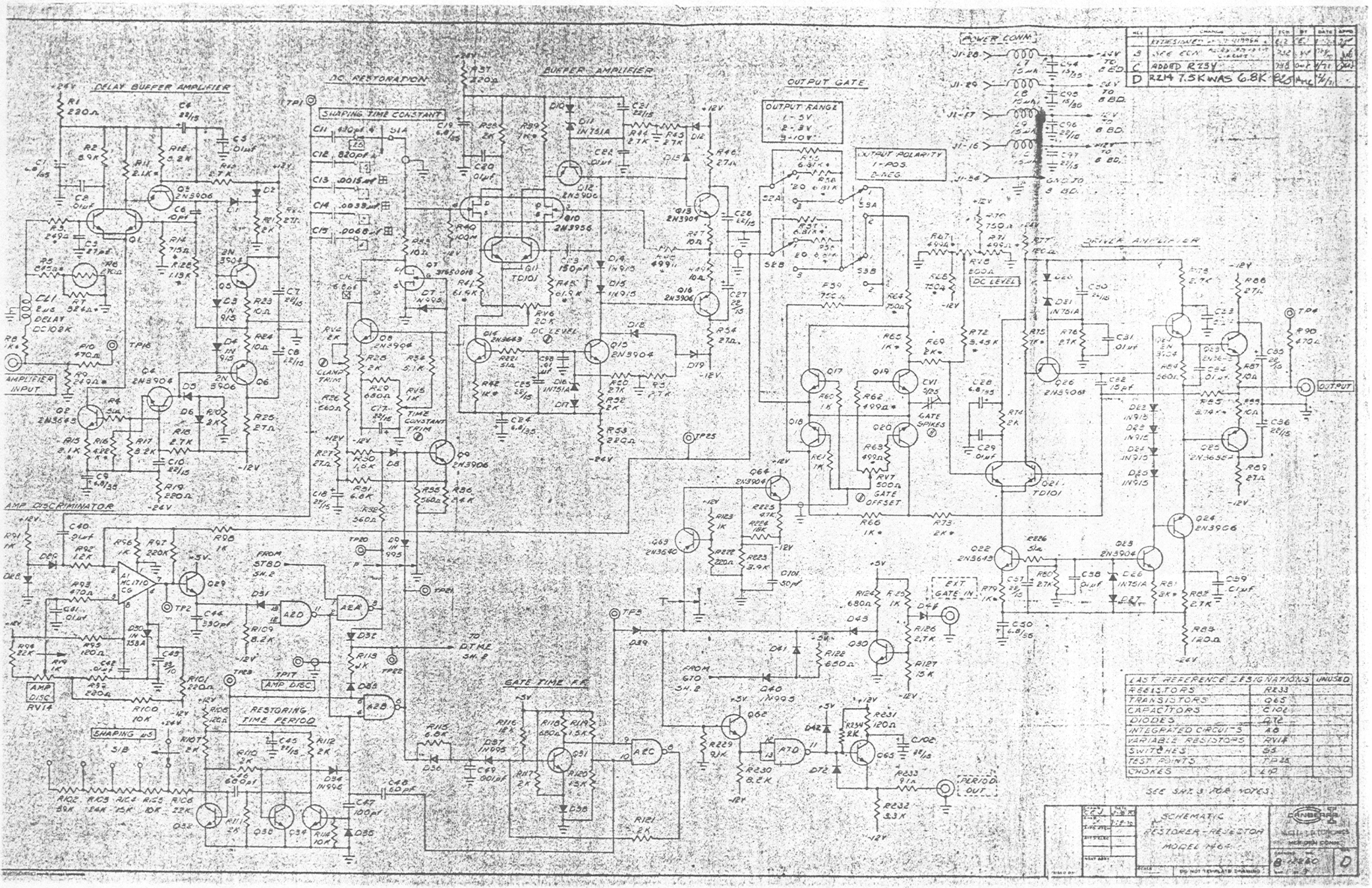
5.3.5 STROBE DELAY AND STROBE OUTPUT

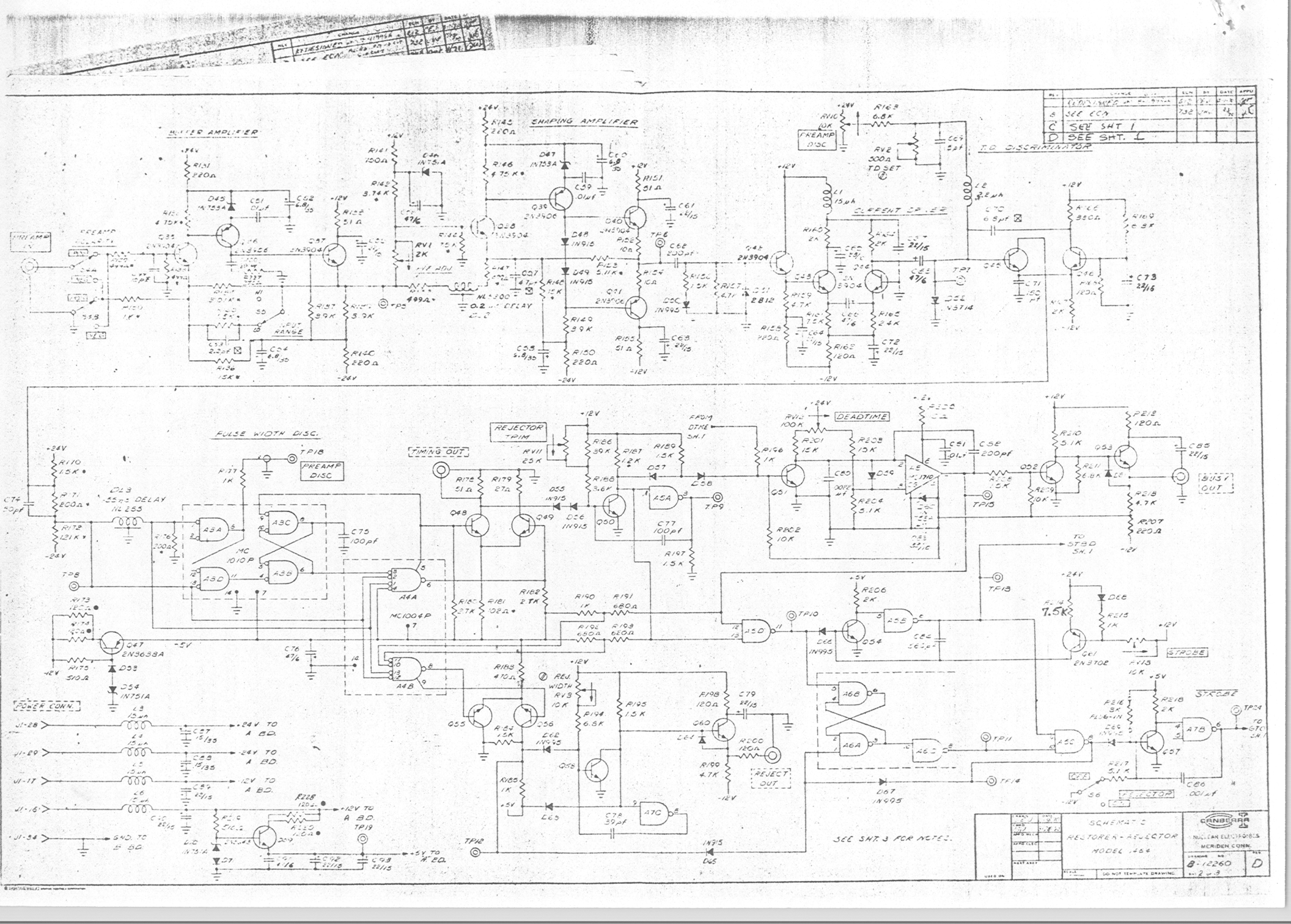
Assuming the preamplifier input pulse does not occur during the busy time, the positive trim signal (at the collector of Q50) produces a negative going output at A5D. The busy signal that follows the trim pulse resets and holds A5D positive, preventing any further outputs during the Busy time.

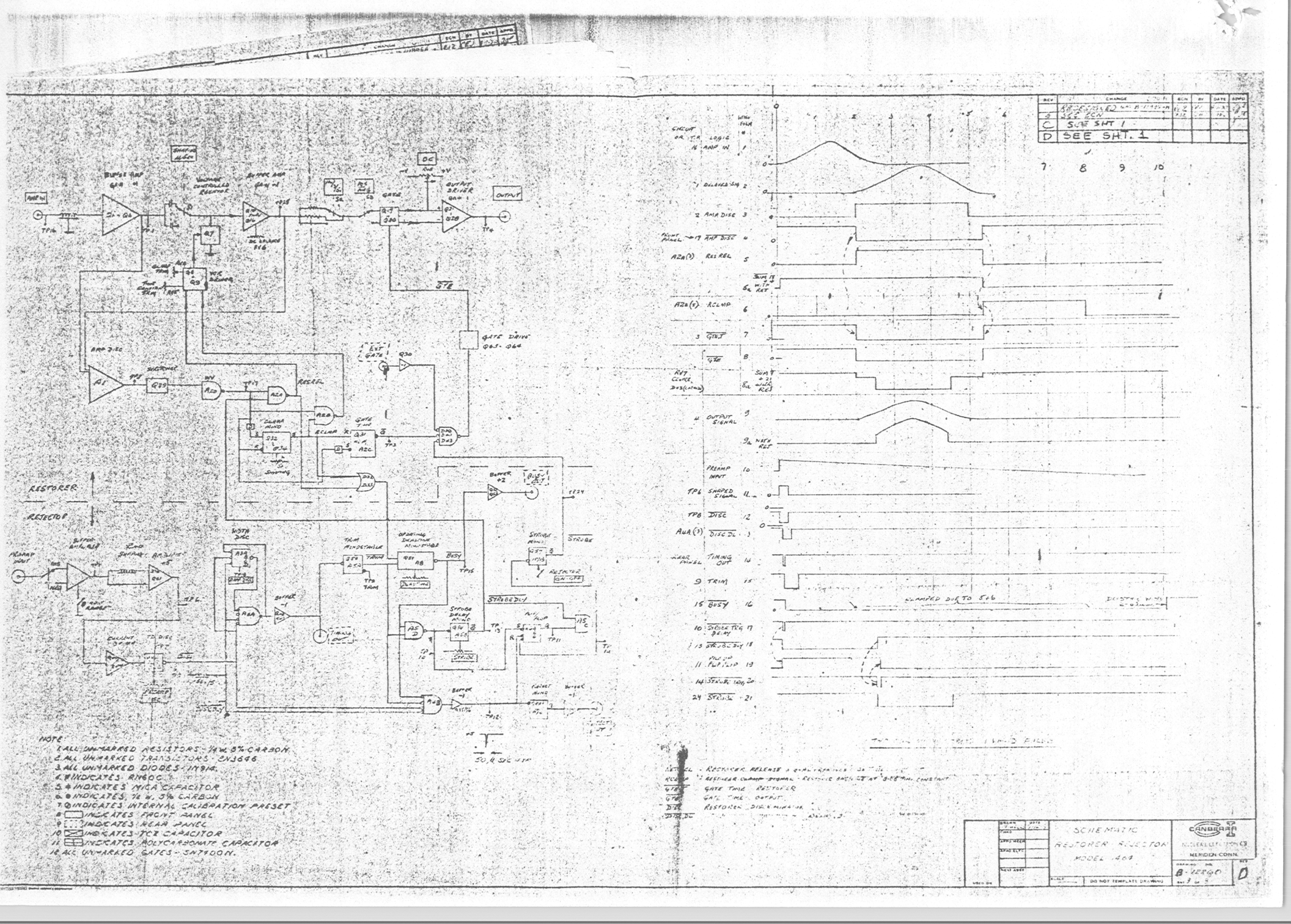
A5D triggers the strobe delay (Q54-A5B-Q61) and sets flip-flop A6 so that the output at TP11 goes to logic 1. The strobe delay width is determined by C84 and the current source Q61. RV-13 (STROBE) provides linear delay control.

At the end of the strobe delay, TP13 goes positive. If A6 is still positive the negative pulse at A5C fires the Strobe monostable (Q57-A7B). The negative 2 microsecond wide strobe pulse from A7B opens the linear gate in the Restorer section. If the REJECTOR switch (S6) is in the OFF position, Q57 is biased OFF through R217 holding A7B negative. Thus the reject circuits are inhibited from control of the linear gate in the Restorer.

A trigger pulse from A5C also resets flip-flop A6 to logic 0 through diode D67. The strobe cycle is ended. If another preamplifier pulse is received during the strobe delay period, indicating pileup, the REJECT output pulse (at the collector of Q56) resets A6 to logic 0 through D65. This is done before the end of the delay, preventing the negative pulse from A5C at the end of the delay time, and inhibiting the strobe pulse. Thus the contaminated pulse is rejected from the Restorer output.


DELAY BUFFER AMPLIFIER
DC RESTORATION
BUFFER AMPLIFIER
OUTPUT GATE
POWER CONN.
DRIVER AMPLIFIER
AMP DISCRIMINATOR
RESTORING TIME PERIOD
GATE TIME F.F.
SHAPING TIME CONSTANT
OUTPUT RANGE
1 - 3V
2 - 3V
3 - 10V
OUTPUT POLARITY
1 - POS.
2 - NEG.
DC LEVEL
GATE SPIKES
GATE OFFSET
EXT. GATE IN
PERIOD OUT
AMPLIFIER INPUT
OUTPUT
DELAY DC102K
CLAMP TRIM
TIME CONSTANT TRIM
AMP DISC
SHAPING µS
FROM ST8D SH. 2
TO D.T.M.E. SH. 2
FROM G10 SH. 2
SEE SH. 3 FOR NOTES
LAST REFERENCE DESIGNATIONS
RESISTORS R233
TRANSISTORS Q65
CAPACITORS C102
DIODES D72
INTEGRATED CIRCUITS A8
VARIABLE RESISTORS RV18
SWITCHES S6
TEST POINTS TP25
CHOKES L10
SCHEMATIC
RESTORER-REJECTOR
MODEL 1464
B-1464
D


MIXER AMPLIFIER
SHAPING AMPLIFIER
PREAMP DISC
T.D. DISCRIMINATOR
CURRENT DRIVER
PULSE WIDTH DISC.
REJECTOR TRIM
TIMING OUT
DEADTIME
BUSY OUT
STROBE
REJECT OUT
POWER CONN.
SEE SHT. 3 FOR NOTES.
SCHEMATIC
RESTORER - REJECTOR
MODEL 1464
CANBERRA
NUCLEAR ELECTRONICS
MERIDEN CONN.
B-12260
SHT 2 OF 3
D



REV	CHANGE	ECN	BY	DATE	APPD
B	ADDED SHT 2				
C	SEE ECN				
C	SEE SHT 1				
D	SEE SHT. 1				

RSTCL - RESTORER RELEASE & QUALIFIER
RCLMP - RESTORER CLAMP SIGNAL - RESTORE RATE SET AT 3.8 E-6 SEC TIME CONSTANT
GTEJ - GATE TIME RESTORER
GTE - GATE TIME OUTPUT
DISC - RESTORER DISCRIMINATOR
DISC DL - [illegible]

DRAWN	DATE	SCHEMATIC RESTORER REJECTOR MODEL 460	CANBERRA INDUSTRIES INC MERIDEN CONN.
TRACED			
APPD MECH			
APPD ELEC			
NEXT ASSY			
USED ON		DRAWING NO. A-1460 REV D	
SCALE	DO NOT TEMPLATE DRAWING	SHT 2 OF 2	