INSTRUCTION MANUAL

430

SCALER

Serial No. ______________________________

Purchaser ______________________________

Date Issued ______________________________

ORTEC

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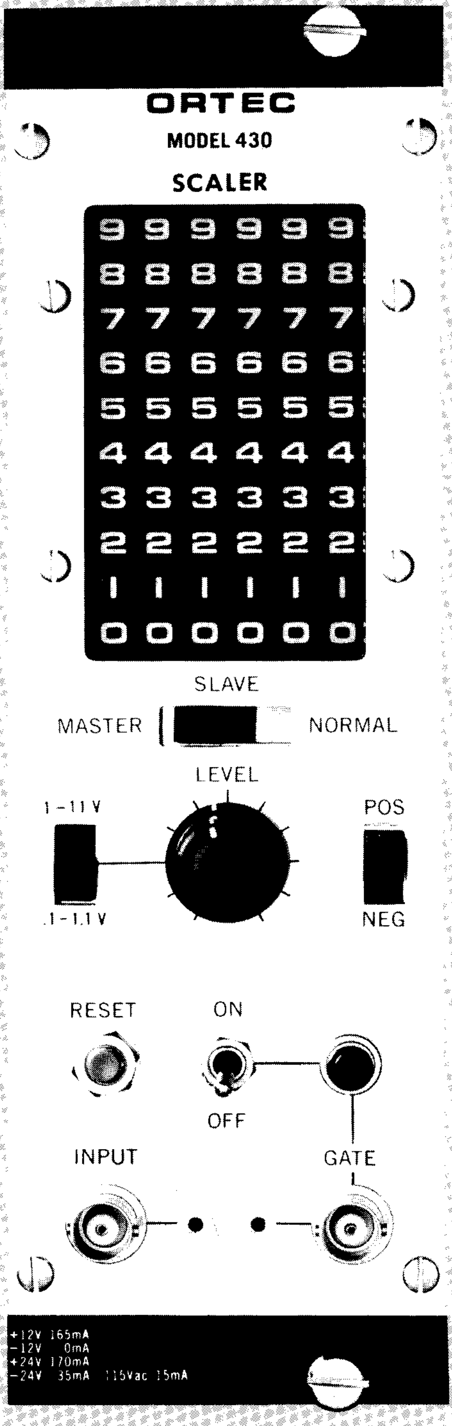

ORTEC
MODEL 430
SCALER
SLAVE
MASTER
NORMAL
LEVEL
1 - 11 V
POS
.1 - 1.1 V
NEG
RESET
ON
OFF
INPUT
GATE
+12V 165mA
-12V 0mA
+24V 170mA
-24V 35mA 115Vac 15mA

ORTEC 430 SCALER

1. DESCRIPTION

1.1 General Description

The ORTEC 430 Scaler is a high speed, integrated-circuit, six decade scaler with a self-contained discriminator and printing output. The scaler is packaged in a two-unit wide module compatible with the AEC recommended Nuclear Standard Module Series.

1.2 Basic Feature Description

The ORTEC 430 features:

SMALL SIZE – Standard double-width module (2.7 inches wide).

HIGH SPEED - Typically, 16 MHz continuous counting rate capability with pulse resolution of about 60 nanoseconds. Guaranteed performance at 10 MHz continuous rates or 100 nanosecond pulse resolution.

LOW POWER – Standard bin power supply will accommodate six units.

INTERNAL DISCRIMINATOR – A direct-coupled internal discriminator will accept signals from 0.1V to 11V. There are almost no restrictions on rise time, and pulses as narrow as 20 nanoseconds can be counted.

POSITIVE OR NEGATIVE INPUTS – Internal discriminator will accept inputs of either polarity as selected by a front panel switch.

ELECTRONIC GATE – Counting can be controlled by dc levels on GATE input, or coincident-anticoincident counting can be performed by pulse control of gate. Gate signals as narrow as 100 nanoseconds can be used.

SYSTEM GATING FLEXIBILITY – When several 430 Scalers (or 431 Timer-Scalers) are connected together as a counting system: any unit can be selected (MASTER) to control the system count gate line, either manually or electronically, and to reset all modules in the system; any unit can be selected (SLAVE) to be controlled by the system count gate line as well as by its own individual manual and electronic gate signals; and any unit can be selected (NORMAL) to be independent of the system count gate line.

SERIAL PRINTING CAPABILITY – By including one 432 Printout Control in the system, a flexible serial-output data acquisition system of up to 50 scalers is obtained. System expansion up to the maximum is possible at any time by merely adding more scalers without any modification to the existing system.

RELIABILITY – All decades are composed of integrated circuits, and all transistors are silicon. All indicators are high-intensity neon glow lamps for long life.

1.3 Related Equipment

The versatile input of the 430 Scaler accepts signals from essentially any logic signal source of either polarity with widths greater than 20 nanoseconds. Timing of counting interval can be obtained with the matching 431 Timer-Scaler. Control and connection to an external data acquisition system is through the 432 Printout Control. System gating and interconnection is obtained automatically through the rear panel control connection. A control cable is furnished with each scaler.

2. SPECIFICATIONS

2.1 Electrical Specifications

COUNT CAPACITY	$10^6 - 1$ (999999)
CONTINUOUS COUNTING RATE	Typically 16 MHz, guaranteed minimum 10 MHz
TRIPLE PULSE RESOLUTION	Measured with three equally spaced pulses. Typical pulse separation of 60 nsec, guaranteed operation at separation of 100 nsec.
COUNT INPUT SIGNAL	Width: Minimum typically 20 nsec, guaranteed to operate at 50 nsec pulse width. Maximum width - no limitation. Rise and Fall Time: Normally no restrictions; guaranteed to operate at rise and fall times of 1 millisecond per volt or less. Polarity: Positive or negative as selected by front panel switch. Amplitude: Adjustable in two ranges from 0.1V to 1.1V and 1.0V to 11V by a front panel selector switch and a one-turn potentiometer. For 50 nsec wide input signals or greater, the threshold span of adjustment will be from 100mV or less to 1.1V or greater on the low range and from 1.0V or less to 11V or greater on the high range. Absolute Maximum Input Signals: Low Range 0.1V to 1.1V — ±100V peak and ±25V average High Range 1.0V to 11V — ±500V peak and ±25V average
DUTY CYCLE	50 nsec minimum interval between trailing edge of first signal and leading edge of second signal.
INPUT IMPEDANCE	1000 ohms, approximately; dc-coupled.
GATE INPUT SIGNAL	To allow counting: +3V or greater To stop counting: +1.5V or less Absolute Maximum Input: +25V, -5V Minimum Width at +3V: 100 nsec Duty Cycle Limitations: none, dc-coupled

Rise and Fall Time Limitations: none

Input Impedance: greater than 1000 ohms. Driving source must be capable of sinking 1 mA of current from positive source.

RESET INPUT SIGNAL

To Reset: +3V or greater

To Not Reset: +1.5V or less

Absolute Maximum Input: ±25V

Minimum Width at +3V: 12μsec

Input Impedance: ~3000 ohms, dc-coupled in series with diode junction.

OVERFLOW OUTPUT SIGNAL

Signal Amplitude: +4V or greater into 100 ohms

Signal Absent Level: +1.0V or less through 1000 ohms to ground

Signal Width: greater than 2μsec

Following signals are located in rear panel 14 pin connectors. See Section 3.4.5 for complete listing and description of these signals:

PRINT COMMAND INPUT

"1" level (for printout), +1.5V or less, -5V maximum
"0" level (not printing), +3V or greater, +12V maximum
Maximum Risetime "0" to "1", 10μsec

PREVIOUS MODULE FINISHED INPUT

"1" level (start data transfer), +3V or greater, +12V maximum
"0" level, +1.5V or less, -5V maximum
Maximum Risetime "0" to "1", 10μsec

DATA OUTPUTS (1-2-4-8)

"1" level, +6V nominal (±1) through isolating diodes
"0" level, +1V or less clamped to ground through isolating diode

THIS MODULE FINISHED OUTPUT

"1" level, +6V nominal (±1)
"0" level, +1V or less

SYSTEM GATE (In and Out Common)

"1" level (to allow counting) nominal +6V level
"0" level (to prevent counting) +1V or less
Note: This line can be grounded from any scaler. Any external connection should be limited to an NPN transistor collector for safe operation.

SYSTEM PRESET (In and Out)

"0" level (to allow counting) nominally +6V
"1" level (to prevent counting) +1V or less
Note: This line can be grounded from any scaler. Any external connection should be limited to an NPN transistor collector for safe operation.

SYSTEM RESET (In and Out)	"1" level (to cause reset) +1V or less "0" level (non reset), nominally +6V Note: This line can be grounded from any scaler. Any external connection should be limited to an NPN transistor collector for safe operation.
PRINT ADVANCE (In and Out)	Negative pulse input from +3V or greater to +1.5V or less with advance occurring when signal returns positive. Maximum risetime of positive transition not to exceed 10μsec.
POWER CONSUMPTION	+24V 170 mA -24V 35 mA +12V 165 mA 115V ac 15 mA
OPERATING TEMPERATURE	0 - 50° C

2.2 Mechanical Specifications

SIZE	Standard double-width module (2.70 x 8.71 inches)
NET WEIGHT	4.1 pounds (1.9 kg)
INDICATORS	High brightness neon glow lamps behind glass mask
READOUT	Six columns of numbers 0 through 9 vertically with 0 at the bottom.

3. INSTALLATION

3.1 General Installation Considerations

The 430, used in conjunction with a 401A/402A Bin and Power Supply is intended for rack mounting; therefore, it is necessary to ensure that vacuum tube equipment operating in the same rack with the 430 has sufficient cooling air circulating to prevent any localized heating of the all-transistor circuitry used throughout the 430. The temperature of equipment mounted in racks can easily exceed 120^0 F (50^0 C) unless precautions are taken.

3.2 Connection to Power - Nuclear Standard Bin, ORTEC 401A/402A

The 430 contains no internal power supply; therefore, it must obtain power from a Nuclear Standard Bin and Power Supply such as the 401A/402A. It is recommended that the bin power supply be turned off when inserting or removing modules. The ORTEC 400 Series is designed so that it is not possible to overload the bin power supply with a full complement of modules in the Bin; however, this may not be true when the Bin contains modules other than those of ORTEC design, and in this case, the power supply voltages should be checked after insertion of the modules. The 401A/402A has test points on the power supply control panel to monitor the dc voltages.

The 430 requires 115V ac to operate the indicators. Some bins and power supplies, as well as jumper cables, may not be wired to provide this power. In the event that the indicators fail to operate in a new installation, the bin and/or cable should be checked to determine if it is properly wired.

3.3 Scaler Interconnection

When a counting system contains more than one 430 Scaler or 431 Timer, the units are connected together as shown in Figure 3.1. The connectors for this hookup are located on the rear panel of each 430 or 431. For nonprinting systems, the order of connection is not important, but for printing systems the order of printing is from 1 through n in sequence as shown in Figure 3.1.

3.4 Signal Connections

3.4.1 Count Input

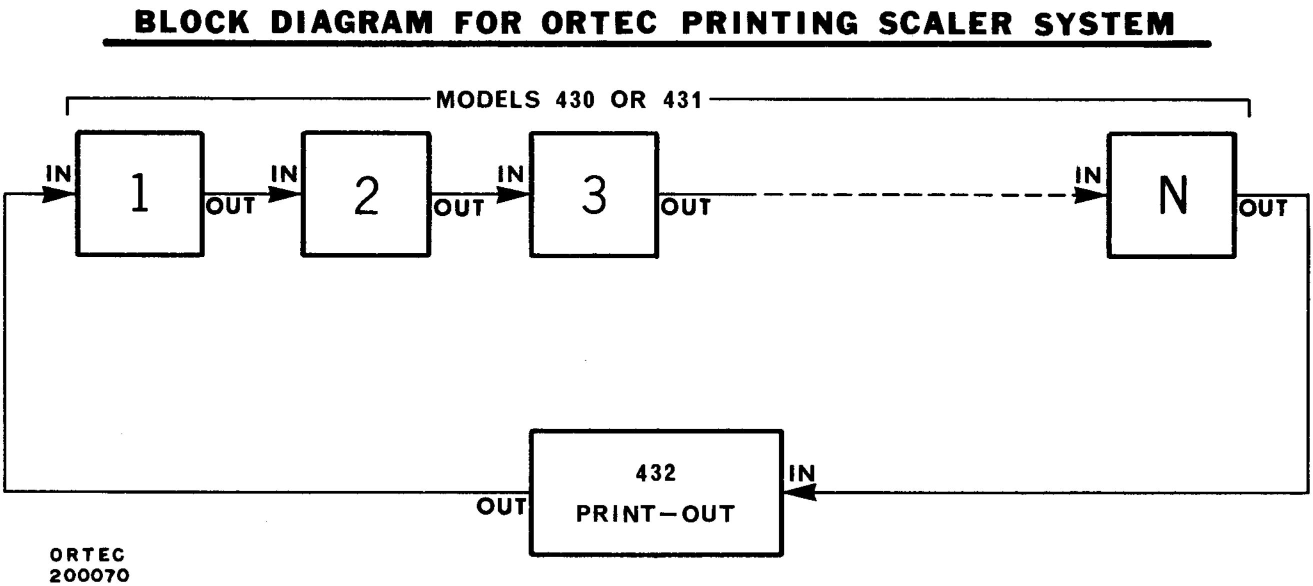
The signal to be counted by the 430 can be connected to either the front or rear panel BNC connector. These two connectors are not isolated from each other; signals from two sources should not be connected simultaneously to the two input connectors.

The input circuit of the 430 is dc-coupled to eliminate baseline shifts associated with changing counting rates. For signals whose average dc level is greater than ±25V, external capacitive coupling must be provided by the user. For dc levels below ±25V, connection to the input can be made safely without damage to the 430. However, for the scaler to count these signals there must be transitions of the signals within the range of ±11V, since this is the input level over which the discriminator will operate.

The flexibility of the 430 makes it possible to count almost any signal wider than 20 nanoseconds and greater than 100 mV in amplitude. There are two important points to remember when supplying signals to the input:

a) The signal should not cross the threshold level more than one time. Signals with overshoot, ringing, etc., can easily be counted more than once if the discriminator level is raised to the level at which the perturbations occur.

b) Signals with slow rise and fall times should be as clean (noise free) as possible because of the high gain and bandwidth of the 430 discriminator. As a slow signal approaches the threshold, a small spurious noise pulse can traverse the threshold and return, causing an extra count to be added to the contents of the scaler.



432 NECESSARY ONLY FOR PRINTING SYSTEMS

Figure 3.1. Scaler Interconnection For System Operation

3.4.2 Gate Input

The Gate input signal can be connected to the 430 by either the front or rear panel mounted BNC connectors. As in the case of the count input connectors, no isolation is provided between the two inputs so that two signal sources are not to be connected simultaneously to the Gate input. With no connection made to the gate input, the input voltage level is about +6V, and the scaler gate will permit the unit to operate. To cut the gate off, the gate input must be pulled down to below ±1.5V but not below -5V. To do this, the driving circuit must be capable of absorbing 1 mA from the gate input circuit. The gate circuit will permit counting when the gate input is at +3V or greater.

3.4.3 Reset Input

The reset input signal can be connected to the 430 by means of the rear panel mounted BNC connector. To reset the scaler to zero, a positive signal of +3V or greater originating from zero potential with a minimum width of 3 microseconds should be used. The input impedance is approximately 3000 ohms in series with a diode junction. Negative signals will not perform any useful function at the reset input. The input circuitry will not be harmed as long as the input signal level does not exceed ±25V.

3.4.4 Overflow Output

The overflow signal is available on a rear panel mounted BNC connector. A positive signal appears at this output each time the contents of the scaler change from 999999 to 000000.

The output signal can provide an input to another scaler or counting register. The output signal is approximately +8V open circuited and +4V into a 100 ohm load. The output signal width is about 2 to 5 microseconds.

3.4.5 System Connector Signals

The following signals are in the two 14 pin rear panel connectors. Ten (10) of the eleven (11) signals are common to the two connectors, the only difference being on pin 7. On the "in" connector, the signal is Previous Module Finished; and the "out" connector, the signal is This Module Finished.

"In" Connector		"Out" Connector	
Pin	Description	Pin	Description
1	Data 1	1	Data 1
2	Data 2	2	Data 2
3	Data 4	3	Data 4
4	Data 8	4	Data 8
5	Print	5	Print
6	Print Advance	6	Print Advance
7	Previous Mod. Finished	7	This Mod. Finished
8	System Gate	8	System Gate
9	System Preset	9	System Preset
10	System Reset	10	System Reset
11	Ground	11	Ground
12	Spare	12	Spare
13	Spare	13	Spare
14	Spare	14	Spare

Below is a description of the signals listed above. For more complete information about these signals see sections 2, Electrical Specifications and 5, Circuit Description.

Pins 1 – 4 — Data Lines	Carry the contents of the individual scalers to the Printout Control. Individual isolation is provided in each scaler, and each scaler drives these lines only during its turn for printing.
Pin 5 — Print	Prepares the scaler for data transfer during printing.
Pin 6 — Print Advance	Advances the scanner in each scaler during printing.
Pin 7 — Previous Module Finished	Starts the actual data transfer for this scaler.
Pin 7 — This Module Finished	Is the signal to the next scaler to start its data transfer.
Pin 8 — System Gate	Carries a "Gate Off" signal to all scalers (Slaves) connected to it. The signal originates in a Master scaler.

4. OPERATING INSTRUCTIONS

4.1 Front Panel Controls

On – Off

Controls the counting of the 430. ON position permits counting. OFF position inhibits counting.

Positive–Negative

Normally set to the polarity of the input signal. For positive input signals, set to POS. For negative input signals, set to NEG. For bipolar input signals, either POS or NEG can be selected as desired. Care should be taken that the bipolar signal produces a minimum second overshoot if high sensitivity is being used in the presence of large input signals. Otherwise, this overshoot may also be counted if it exceeds the threshold.

Range 0.1-1.1V; 1-11V

Two-position switch to select the range of input signal amplitudes over which the LEVEL adjustment operates. This switch, along with the LEVEL adjustment, provides a 1100:1 dynamic range for the threshold adjustment.

Level

This one-turn potentiometer adjusts the input level within the selected range that will be counted. Normally, for counting signals whose amplitude is constant (logic signals) the LEVEL should be adjusted approximately half way between the expected lowest amplitude true signal and the largest amplitude false signal. For use with linear signals, assure that the signals have only one point of inflection, or some signals may cross the threshold more than one time, producing erroneous counts.

Reset

A pushbutton switch which resets the contents of all decades to zero when depressed. For proper operation of the RESET function, the ON-OFF switch should be set to OFF before pushing the RESET pushbutton.

Gate Indicator

This neon glow lamp indicates the condition of the scaler GATE circuit. The indicator ON means the scaler is in a counting condition. The indicator OFF means that the scaler will not count. When the scaler is being gated either ON or OFF at low duty cycles, the neon lamp will not provide a good indication of the gate condition because the change in light or the gating rate will not be perceptible to the observer.

Master-Slave-Normal

This three-position slide switch determines the role of the individual module when contained in a counting system as shown in Figure 3.1. The switch allows the user considerable flexibility for controlling the system either manually or electrically, or for doing complex gating without the use of auxiliary equipment. To appreciate the role of this control, consider the System Gate and System Reset line functions. Both are such that a particular scaler can either transmit a signal to other modules through the line or receive signals from other modules through the line; and in some cases both sending and receiving can be performed simultaneously. The System Gate signal can prevent any scaler or timer attached to it from counting when the line is in the OFF condition, and the System Reset line can reset any scaler attached to it.

Master

A unit selected as a MASTER:

1. Turns the System Gate line off when its own ON-OFF switch is set to OFF or when its own Gate signal is at ground potential.

2. Transmits a reset signal on the System Reset line when the Reset pushbutton is depressed or when the Reset input is at +3V.

3. Is not gated off by a signal on the System Gate line that has originated from another MASTER scaler or timer.

4. Is reset by a signal on the System Reset that has originated from another MASTER scaler or timer.

5. Is gated off by a signal on the System Preset line, originating in any MASTER or SLAVE unit in the system.

If more than one MASTER exists in a system, each MASTER will exercise control over the System Gate line. This means that all MASTERS cannot be started by the ON-OFF switch on any one unit. Instead, all MASTERS will have to be switched on individually.

Slave

A unit selected as a SLAVE:

1. Does not exercise any control over the System Gate line.

2. Does not exercise any control over the System Reset line.

3. Is gated off by a signal on the System Gate line.

4. Is reset to zero by a signal on the System Reset line.

5. Is gated off by a signal on the System Preset line.

Normal

A unit selected as NORMAL:

1. Does not control the System Gate line.

2. Does not control the System Reset line.

3. Is not gated off by the System Gate line.

4. Is <u>not</u> reset by the System Reset line.

5. Is gated off by a signal on the System Preset line.

4.2 Initial Operation of Scaler

1. Install the 430 into a 401A/402A Bin and Power Supply, or equivalent, and turn the power on. (It is recommended that the power always be off when inserting or removing modules from the bin.)

2. Push the reset pushbutton. The readout should now indicate that the contents of the scaler are zero (000000).

3. Turn the ON-OFF switch ON and the Gate Indicator should be lighted. Turn the switch to OFF and the indicator should be off.

4. Set the Level to full clockwise position and the selector switch to 1 to 11V.

5. Set the polarity switch to correspond to the same polarity as the signal to be counted.

6. Connect a signal to the Input Connector. The signal should not be greater than 11V in amplitude or narrower than 50 nanoseconds with a maximum duty cycle of 50%. Signals narrower than 200 nanoseconds or with a rise and fall time of less than 100 nanoseconds may need to be terminated at the scaler INPUT. A front panel test point is provided to monitor the input signal.

7. Turn the ON-OFF switch to ON.

8. Rotate the Level potentiometer counter-clockwise until the 430 starts counting. If the input signal is below 1.1V in peak amplitude, the LEVEL selector switch must be changed to 0.1 to 1.1V to make the unit operate.

9. With the scaler operating, ground the GATE input and observe that counting stops and the GATE indicator goes off. Remove the ground and restore the counting condition.

10. Turn the ON-OFF switch OFF and counting should stop and the indicator should be off.

4.3 Counting Setup with One Scaler

Proceed as outlined in the preceding section, but omitting those steps involved in "testing" the instrument. Take care that the input signal does not exceed ±100V or ±500V with the LEVEL selector switch in the low or high range respectively.

4.4 Counting with Multiple Scaler/Timer Setup

4.4.1 Preferred Setup

In a multiple scaler setup, each scaler should be inserted into the bin and power supply and connected together as shown in Figure 3.1. If the system data is to be printed automatically with the 432 Printout Control, the sequence for OUT and IN control cable connections determine the printing order in the system. For nonprinting system, the sequential arrangement of the control cables is unimportant.

With the scalers properly connected together, the individual count signal connections and gate signal connections are made to the respective scalers. When all units are installed, testing of individual scalers can be performed by operating each unit in either the MASTER or NORMAL mode of operation. This frees the unit under test from all other scalers in the system, except for Preset. If the gate indicator does not come on or if the scaler does not accumulate counts during this phase, check to see if a 431 Timer/Scaler in the system has reached a Preset condition. Any module reaching Preset will stop all modules from counting. This can be eliminated during the setup phase by resetting the 431 and turning it off.

After the individual scalers have been set up and tested for proper operation, the Master-Slave-Normal controls can be switched as desired. Normally in a counting system, one scaler (or timer) would be selected as a Master and all remaining scalers (or timers) would be selected as Slaves. With this arrangement, the entire counting system can be controlled from the Master. The ON-OFF control on the Master would start and stop accumulation in all of the scalers and timers and the Reset pushbutton on the Master would reset all of the system. In addition, a Gate signal to the Master could also exercise control over the entire system while individual Gate and/or Reset signals to any Slave would control only that Slave scaler. It is important to remember that a scaler selected to operate in the NORMAL mode cannot be started or stopped by a Master unit.

4.4.2 Alternate Connections for One or Two Scalers with a Timer

The module interconnection scheme shown in Figure 3.1 is the preferred manner of connecting more than one scaler or timer into a data system because of the flexibility available. There is, however, an alternate connection for a simple setup involving a 431 Timer/Scaler and one or two 430 (or 431) Scalers, without using the control cables.

A cable connected from the rear panel Interval Connector of the Timer to the Gate Connector of the Scaler(s) will allow the ON-OFF switch on the Timer to start and stop counting in the scalers provided the scaler controls are set to permit counting. When the Timer reaches Preset, the scalers will stop counting.

4.5 Printing Systems

The 430 Scaler is designed to operate as a part of an automatic data acquisition system. Some of the characteristics of the scaler (and a printing system) will be described here, although a more thorough description will be found in the literature describing the 432 Printout Control.

The 430, upon command, provides the data stored in its register to the 432 in a serial-by-character format. The data is fed to the 432 in six groups (characters), one following the other at a rate determined by the 432 or the printout device. Each group or character is composed of four bits of information in a 1-2-4-8 code with a logical one being about +6V and a logical zero about 0V. The transfer of data starts with the most significant decade and proceeds sequentially to the least significant decade. Figure 4.1 shows the sequence of events for a single scaler containing the number 705849. As a note of explanation, the Print Command signal originates in the 432. It can be initiated manually, by a 431 reaching a Preset condition, or triggered externally. The Start Data Transfer is supplied by the 432 in the case of Scaler 1 in Figure 3.1, by Scaler 1 in the case of Scaler 2, by Scaler 2 in the case of Scaler 3, etc. In other words, as each scaler finishes transferring its data to the 432 it sends a signal to the following scaler allowing data transfer. (In reality, the signal Start Data Transfer in Figure 4.1 is called Previous Module Finished on the 430 schematic diagram.)

The following sequence of events illustrates how a multiple scaler printing system operates.

a. A Print Command is generated manually, by Preset, or triggered.

b. All scalers and timers stop accumulating and remain static for one or two seconds.

c. All indicators go off except the most significant digit in Scaler 1, which is on until the digit is printed by the output device.

d. Each of the remaining five digits in Scaler 1 is printed in succession, and as each digit is printed the indicator for that digit is illuminated.

e. A space is generated in the printed format after the six digits representing the first scaler.

f. The six digits of scaler 2 are printed in succession.

g. A space is formed as in e.

h. This sequence repeats until the last scaler has finished printing. Carriage return and line feed replace the space function at appropriate times in the program.

i. After the last scaler has been printed, one of two basic modes can be selected:

1. The system will remain in a static or noncounting mode until a new cycle is started. The scaler indicators will be on.

2. A System Reset will be generated and data accumulation will restart.

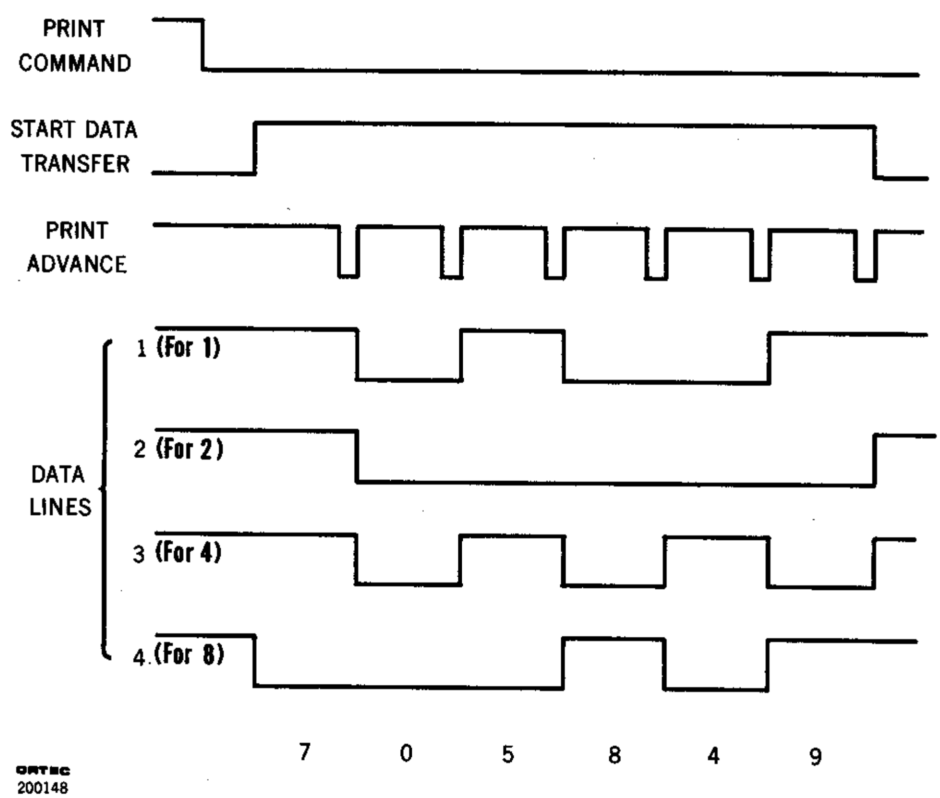


Figure 4.1. Signal Sequence for Transferring Data for 705849
From a Printing Scaler to the 432 Printout Control

5. CIRCUIT DESCRIPTION

5.1 General Description

The 430 is a six-decade ripple scaler preceded by a fast discriminator. It includes logic for gating and for printing and it employs a six-stage ring scanner with a single BCD-to-decimal decoder to provide the illuminated readout. These respective "parts" of the 430 are described below. Refer to the block diagram and the schematic diagrams for the following discussions.

5.2 Discriminator

Basically the input discriminator to the 430 is a dc-coupled, high gain differential amplifier driving a tunnel diode. The threshold level is one input to the differential amplifier and the signal is the other input. Only those signals greater than the reference will be amplified to trigger the tunnel diode and produce an output signal.

If we assume that a positive signal is applied to the input, we can trace the signal through the circuit to see the basic manner in which the circuit operates. The signal is applied to an attenuator composed of R4 and R5. For signals below about 1.1V the attentuator is not used. For signals between 1 and 11V, the input is attenuated by a factor of 10. After the attenuator is the input protection circuit composed of D11, D12, D13, and the associated resistors. Suppose that the signal is large (25V or so). As the input rises, the current from R114 is diverted into R116 replacing current formerly supplied by R115, with the result that the base of Q82 rises linearly with the input. However, when the signal increases beyond about 1.5V, the current from R115 is routed through D12 and R119 to ground. As the input keeps increasing, the base of Q82 will finally clamp at about +3V when all of the current through R115 flows through D12. At this point the right half of D11 will cut off to protect the input transistor Q82. For negative signals, the operation is analogous with D13 clamping and the left half of D11 cutting off.

When the input level at the base of Q82 exceeds the reference level at the base of Q77, amplified signals appear at the bases of Q79 and Q80 which provide further amplification. The current which normally flows through Q79 is diverted to Q80, through the polarity switch and into the tunnel diode D16. When the tunnel diode switches to its high voltage state, Q74 is cut off and a negative signal of nominally 1V is produced at the collector of Q74 to provide an input to the first stage of the first decade.

Negative input signals are processed by changing the reference voltage from positive to negative, and by switching the tunnel diode drive to Q79.

5.3 Fast Decade

The first decade of the 430 is composed of five integrated circuits. Four of the circuits (926) are 20 MHz JK Flip Flops and the other (914) is a dual two input positive Nor circuit.

The JK Flip Flop has the following inputs and performance characteristics:

a. The Clock Input - pin 3: A negative going signal on this input may cause an output change, but a positive going signal does nothing.

b. The Gate Inputs - pins 2 and 4: A negative level on the gate inputs permits output changes and positive levels prevent changes. If at the time the clock goes negative, there is a positive signal on pin 2 and a negative signal on pin 4, the output at pin 7 will go negative and pin 9 will go positive. If pin 7 was already negative, no change will occur. If the reverse is true, pin 2 negative and pin 4 positive, the output on pin 9 will go negative and pin 7 will go positive. If both gate signals are positive, there will be no change in the output state; or if both gate inputs are negative, the device will change states like an ordinary binary.

A truth table for the 926 JK Flip Flop as used in the 430 is shown in Figure 5.1. The contents of the table are applicable when the negative transition of the clock input has been restored.

The 914 Dual Nor gate has the following inputs and performance characteristics:

Inputs - pins 1 and 2 are one gate and 3 and 5 are the second gate. Either or both of the 2 inputs at a high level will force the output to low level, or both inputs at a low level will force the output to a high level.

Outputs - pin 7 for the gate controlled by inputs 1 and 2; pin 6 for the gate controlled by inputs 3 and 5.

For the following description of the fast decade refer to Figure 5.2 and the Scaler schematic.

The negative signals from the discriminator go directly to the clock input of the first stage of the scaler. Normally the Scaler Gate signal is at 0V so that the first stage acts like an ordinary binary, changing states at each input. The output of the first stage (pin 9) is the clock input to the remaining stages. Note that in Figure 5.2, pin 7 of the first stage is shown which is of the opposite polarity of the signal on pin 9.

In the reset condition, the pin 7 outputs are high and the pin 9 outputs are at low. The low output from pin 9 of the 8-stage feeds back to control the gate inputs of the 2-stage. This means that the 2-stage will act like a binary as long as this condition exists but will not change at all when the gate input goes to the high state.

Gate Signals at Time of Clock Transition		Outputs after Clock Transition	
Pin 2	Pin 4	Pin 7	Pin 9
H	H	No Change	No Change
H	L	L	H
L	H	H	L
L	L	Change State	Change State

H = High Level, L = Low Level

Figure 5.1. Truth Table for 926 JK Flip Flop as used in ORTEC 430 Scaler

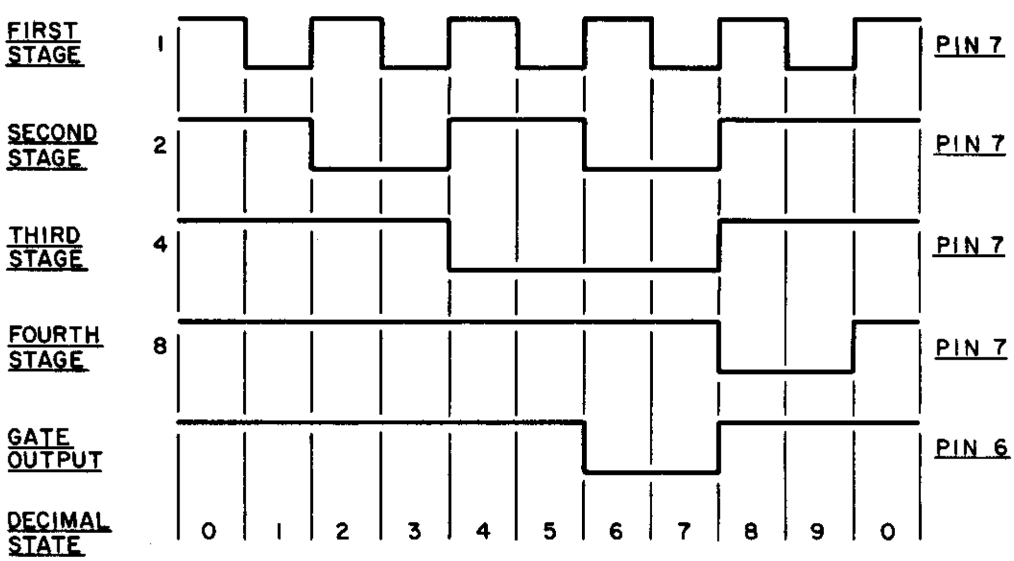


Figure 5.2. Timing Diagram Of Fast Decade

Counting proceeds in the decade as in an ordinary binary up to the count of 9. The scheme used in the 430 is like a synchronous counter in that the last three stages all change states at the same time because they all have the same input clock, the output of the 1-stage. This minimizes delays which are important in a feedback scaler. The 914 gate provides for synchronous counting of the 8-stage by setting pin 4 to the low state at the count of 6. Then when the count changes from 7 to 8 and pin 9 of the 1-stage goes negative, pin 7 of the 8-stage goes negative. Note that prior to this pin 2 of the 8-stage was negative so that each negative transition of the clock attempted to change pin 9 to the negative stage, but since it was already in that state, no change occurred. After the eighth input, the feedback from the 8-stage to the 2-stage is positive so that the next clock to that stage will not change its state; the 8-stage feeds back on itself from pin 7 to pin 2 so that the next clock will set pin 9 back to its original low level, and both the 2-stage and 4-stage are back to their original condition. The ninth input signal changes only the 1-stage, but it does not change any of the other stages because the transition of pin 9 is in the positive direction.

On the tenth input signal, the first stage changes and the clock input to the 2-, 4-, and 8-stages goes negative. The 2-stage cannot change because the gate inputs are held positive by the 8-stage, and the state of the 2-stage inhibits any change in the 4-stage. The 8-stage gating is such that pin 2 is negative. Therefore, the 8-stage changes state and the entire circuit is back to its original reset condition.

5.4 Slow Decades

Following the fast decade in the 430 Scaler are five identical integrated circuit decades. Each decade is contained in a single 8 lead TO-5 size case. These decades are designated on the schematics as 958. These decades are guaranteed by the manufacturer[1] to operate at 2 MHz, which is well within the range of their use in the 430.

These devices count in a 1-2-4-8 BCD format with the true "1" state being a low potential (about 0V) and the false or "0" state at about 1.5V. Counting takes place as the input signal goes positive.

5.5 Display Scanner

5.5.1 Ring Scaler

The contents of the six decade scalers are sequentially scanned in the 430 for readout. The following discussion refers to the Block Diagram and the lower half of the scaler schematic.

A normally free-running multivibrator composed of transistors Q63 and Q64 provides signals at approximately 1 Khz to a six-stage ring scaler. The signals from the multivibrator are shaped by Q61 and Q60 to drive the ring scaler input.

The ring scaler is made up of six identical stages with each stage composed of one PNP transistor and one NPN transistor. For example, Q45 and Q51 make one stage, Q46 and Q52 make another stage, etc. The main feature of this type of arrangement is that it is a very low power configuration because only the two transistors in the "on" stage are drawing power.

With each input signal to Q58, the common emitter line of the NPN transistors is raised positive by Q58 which cuts off the "on" NPN transistor. The positive signal at the collector of the NPN unit is capacitively coupled to the base of the next NPN transistor with a time constant

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[1] Fairchild Semiconductor. The devices are commercially available as the 958 Decade Counter.

sufficiently long that when the input signal goes away, the second NPN base is still positive. Thus, the second NPN turns on, causing its mating PNP to also turn on. Now the ring scaler is again in a stable condition with the "on" stage shifted one position.

Each stage of the ring scaler provides two outputs. One output gates the data from a scaler decade onto the common data lines while the second output gates the high voltage to the column of neon indicators representing that same decade. Therefore, as the ring scaler advances, it sequentially gates the contents of the decades onto the common data lines and supplies power to the indicators appropriate to each decade.

5.5.2 Data Gates

An output from each stage of the scanner ring scaler goes to the input of one of six sets of transistors called Data Gates. These inputs go to Q39-Q44 shown in the center of the scaler schematic. When for example Q44 is on, the other five transistors driven by the ring scaler are off. This means that Q32, Q20, Q26, and Q38 <u>can</u> conduct if the signals driving their bases are positive. These base signals from the four stages of the first decade are positive when the respective "bit" is "0". Therefore, since Q32, Q20, Q26, and Q38 invert the signals, the common output lines are at a low potential (about 0.5V) for a logical "0" and at about +6V for a logical "1". Note that the contents of the other five decades do not influence the common data lines because Q39-Q43 are not turned on. Thus, at any particular time, the data line signals are a function of a decade's contents and the position of the ring scaler.

5.5.3 Neon Gates

The second output of the ring scaler stage goes to one of the Neon Decade Gate transistors (Q1-Q6) on the Control Board Schematic. When a stage in the ring scaler is "on" the output signal to the Neon Gate is held below the +6V emitter supply and the Gate transistor is held off. This allows the voltage at the junction of the two series collector resistors to move upwards toward the level of the high voltage supply (~165V dc). However, when the level reaches about 135V one of 10 neons tied to that point will turn on after which the voltage falls to about +65V, the maintaining potential of the NE2H used in the 430. The particular neon which comes on will depend upon the contents of the decade and may change during the off time of the Gate transistor if the scaler is accumulating counts.

The signals from the "off" stages of the ring scaler turn on the Neon Decade Gate transistors. With the transistors on, the potential to the neons is about 60-70 volts which is far below the ionizing potential of about 135V. This means that at any one time there is only one decade illuminated. The scanning rate at 1 KHz is high enough to prevent flicker and this mode of operation greatly lengthens the already long life of the neon indicators.

5.6 <u>Display Decoder</u>

The circuit for the single BCD-to-decimal decoder used in the 430 is shown on the Control Board Schematic. The four data line signals, 1-2-4-8, are inverted by Q19-Q22 to provide the complementary signals $\bar{1}$-$\bar{2}$-$\bar{4}$-$\bar{8}$. These eight signals are then decoded in the diode "and" gates (D5-D14) in groups of two. That is, the outputs of the gates are valid for 0-1, 2-3, 4-5, 6-7, and 8-9 for each of the five gates respectively. The diode gates each drive two transistors with one transistor of each gate controlled by the "1" signal for the odd numbers (1, 3, 5, 7, 9) and the second transistor controlled by the "$\bar{1}$" signal for the even numbers. For example, suppose that the decade being "looked at" contained a 7, so that 1-2-4 were positive and 8 was at 0V. Then out of the inverts $\bar{1}$-$\bar{2}$-$\bar{4}$ would be 0V and $\bar{8}$ would be positive. Looking at the diode gate inputs, we find that the second gate from the top is the only one that has all of its inputs positive. Then Q11 for the 7 indicator would be on because Q11 can conduct through Q7 which is turned on by "1" while Q12 for 6 cannot conduct because $\bar{1}$ holds Q8 off. One of the six indicators for the number 7 will conduct through Q11. The particular "on" indicator will depend upon which decade the data came from.

5.7 Gate Circuits

The input gating circuit for the 430 is shown on the Control Board Schematic. Note from the schematic that the ON-OFF switch and the Gate input are the two inputs to a diode gate composed of D17 and D18. If either input is at zero, the output from Q23 will also be at zero because of the two cascaded inverters.

The output of Q23 through D20 along with the inputs to Q26 and Q28 are the three inputs to a positive "and" gate (D20, Q26, Q28) that is followed by an inverter Q27. Thus, if any of the three inputs is at zero volts, the output of Q27 will be positive. This positive signal (Scaler Gate) goes to the gate inputs of the first JK Flip Flop of the fast decade and will prevent the decade from counting.

The Scaler Gate is positive and inhibits counting if any one of the following conditions is met:

1. On-Off switch is Off.

2. Gate input is on zero volts.

3. System Gate signal is at zero and in Slave mode (Q26).

4. System Preset signal is at zero (Q28).

The output of Q25 is connected to the System Gate line when the Master mode is used. Thus, in Master, if either the On-Off switch is Off or if the Gate input is zero, the output of Q25 will hold the System Gate line to zero, stopping the counting of all Slave scalers that are connected into the system.

5.8 Reset Circuit

The Reset circuit of the 430 is shown in the lower left of the Control Board Schematic. There are two ways that Reset can be performed at an individual scaler. A positive Reset signal is inverted by Q32 producing a zero voltage level at the collector, or the Reset pushbutton can be depressed to ground the collector of Q32. This negative signal is one input of the two-input negative "or" gate composed of D22 and D23. The other input is provided by the System Reset when operating in the Slave mode. If either the input to D22 or the input to D23 goes negative from about +6V to about zero potential, a positive reset signal will be generated by Q34 and be fed to all of the decades by the emitter follower, Q35.

Note that in the Master mode, the collector of Q32 is connected to the System Reset line and can reset all other scalers in the system that are in either the Master or the Slave mode of operation. The local Master scaler will also respond to a signal on the System Reset line, if this signal is furnished from another Master unit in the system.

5.9 Printout Control Circuitry

The Printout Control circuitry is shown in the lower left portion of the Scaler Schematic. Normally when the scaler is operating, the internal scanning circuitry, composed of the Display Oscillator, the ring scaler, and the Data Gates, is operating at a fast rate totally independent of any other part of the counting system. When operating during printout, the Display Oscillator is disabled and this same scanner is utilized with external control.

When a negative Print command is received at the base of Q65, Q66 cuts off and its collector goes positive. This accomplishes two things. First, it stops the Display Oscillator because Q64 cannot conduct current, due to its back biased emitter to base junction. Secondly, the positive signal from Q66 is inverted by Q69 to produce a fast negative going signal which sets the bistable mode of Q70 and Q71 so that Q71 is on. With Q71 conducting, the output from Q68, This Module Finished, is at ground potential.

Since this same sequence of events takes place simultaneously in all scalers in the system, the input, Previous Module Finished, is also at ground potential. (Note that the output, This Module Finished, is the input, Previous Module Finished, to the next scaler in the system.) Therefore, Q67 is off and D6 is back biased so that the base of Q57 is raised positive by R73.

With the base of Q57 positive all six stage of the ring scaler are off with the result that all Data Gates are off and all indicators are off. The scaler then does not influence the system data lines at all because D1-D4 will be back biased if another scaler pulls one of the lines to ground potential.

When the Previous Module Finished signal goes positive, indicating that it is time to begin scanning, Q67 turns on. This turns Q57 off producing a positive transient at the base of Q59 and turning Q59 on momentarily. When Q59 turns on, Q51 also turns on which in turn turns on Q45. Then after the transient is over, Q51 and Q45 remain on and the most significant decade of the scaler is gated onto the common data lines for both display and printout.

After the most significant digit has printed, the back edge of the negative Print Advance signal from the Printout Control (ORTEC 432) advances the ring scaler one state to the second most significant decade. This process repeats until the least significant decade has been printed. Then the Print Advance causes the ring scaler to leave the last position (Q50 and Q56 on). This produces a positive transient at the base of Q73, then resets the bistable (Q70 and Q71) so that Q70 is on.

With Q70 on and Q71 off, a positive signal at the collector of Q71 turns Q67 off which turns Q57 on and makes the ring scaler again inoperative with all six stages off. At the same time, a positive This Module Finished signal is produced by Q68 to turn on the most significant decade of the next scaler in the system.

There are two points that were not considered in the preceding discussion. First, unless the Print signal is near ground potential, the ring scaler will always be in one of its six states because D6 will not let Q57 turn on. Secondly, if Q57 is on, as in the case during printing except when this particular scaler is printing, the Print Advance does not affect the ring scaler.

6. MAINTENANCE INSTRUCTIONS

6.1 Testing Performance

The basic performance of the 430 Scaler can be tested by following the procedure outlined in Section 4.2 of this manual. This section is entitled Initial Operation. It should be noted that this will not check the unit to its published specification.

6.2 Calibration Adjustments

There is only one calibration adjustment in the 430. This potentiometer, located on the Scaler board and shown on the Scaler Schematic near the signal input, is for the purpose of setting dc input voltage at ground potential.

Adjustment should only be necessary when Q77, Q78, Q81, or Q82 are replaced. The procedure for adjustment is as follows (use a nonconducting or insulated screwdriver):

1. With a digital voltmeter or vtvm, measure the input voltage at the front panel BNC. Use the range 0.1 to 1.1V and the level fully counterclockwise.
2. Adjust the potentiometer until the reading is less than ±10mV.
3. Change the polarity switch and re-measure the voltage.
4. Normally, adjustment can be made so that the change in voltage will not be more than about 5mV as the polarity switch is changed. A difference of as much as 10mV would not be detrimental.

6.3 Suggestions for Troubleshooting

When a 430 does not function properly, it should first be isolated from all other units except the one providing the signal to be counted. The problem may be in the system interconnections and this is a quick way to check for this. Below are listed a few of the more common problems that might be encountered. Suggestions are made for each.

6.3.1 Unit will not count at all

a. Check to see if discriminator is set too high.

b. Check to see if polarity switch is set properly.

c. Check to see if On-Off switch is On.

d. Check to see if Gate Indicator is On.

1. If gate indicator is off and cannot be turned on, the problem is most likely in the gate circuits described in Section 5.7.
2. If gate indicator is on, the problem is most likely in the input discriminator as described in Section 5.2.
3. If discriminator output at Q74 is negative signal of 1.0 to 1.5V from a dc level of approximately +1.0 volt, the first binary (926 JK - IC I4) is probably faulty.

6.3.2 Unit will not count at low level settings

This probably means that the input signal is riding on a dc level equal to or greater than the threshold setting. This can be check at the front panel test point. If this is not the case, the four input transistors are poorly matched.

6.3.3 Unit multiple counts each input signal

a. Check input signal at front panel test point for:

1. overshoot on front edge of pulse due to poorly terminated line. This can be cured by terminating signal at input to scaler.

2. ringing or irregular top that could be passing through threshold more than once.

b. If a bipolar input signal is being used, the second overshoot can sometimes be significant if a low threshold is being used.

c. If the input signal quality is good, check the discriminator all the way through looking for oscillations, etc.

6.3.4 All indicators are off

a. Check Gate Indicator and if it will not turn on, the high voltage supply is probably out.

b. Remove rear panel IN and OUT cables. This will eliminate print associated signals.

c. Measure voltage at base of Q57; it should not exceed +0.7V. If above this level, ground base and see if indicators come on. If this solves problem, check circuit through Q66 and D6.

6.3.5 All six indicators of one numeral will not turn on. Check the decoding circuit for that numeral, particularly the transistors Q9-Q18.

6.3.6 Odd or even numerals will not turn on. Check Q7 for odd numerals off and Q8 for even numerals off.

6.3.7 One decade not indicated or indicated with all other decades. Check the Neon Decade Driver transistors Q1-Q6.

6.3.8 One decade on - all others off

a. Remove rear panel In and Out cables to eliminate print associated signals.

b. Check base of Q58 for +4V, 0.5 to 1μsec signals at about 1 kHz. If not present, oscillator (Q63, Q64) is likely bad.

c. Make detailed check of ring scaler.

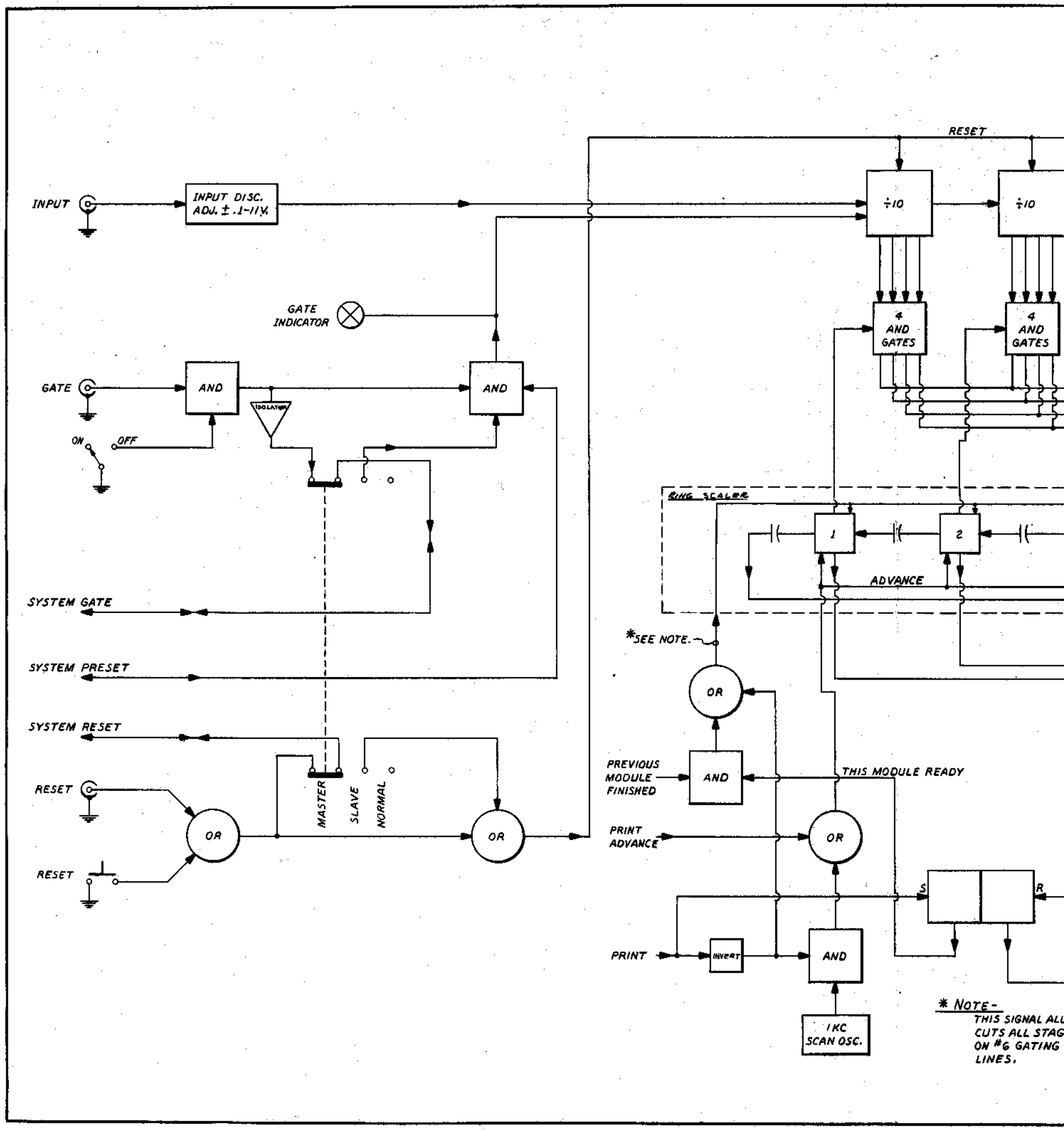
6.3.9 Reset Pushbutton will not stop counting.

This is not the intention of the reset feature. Proper reset action is obtained by first stopping the counting, then resetting scaler to zero.

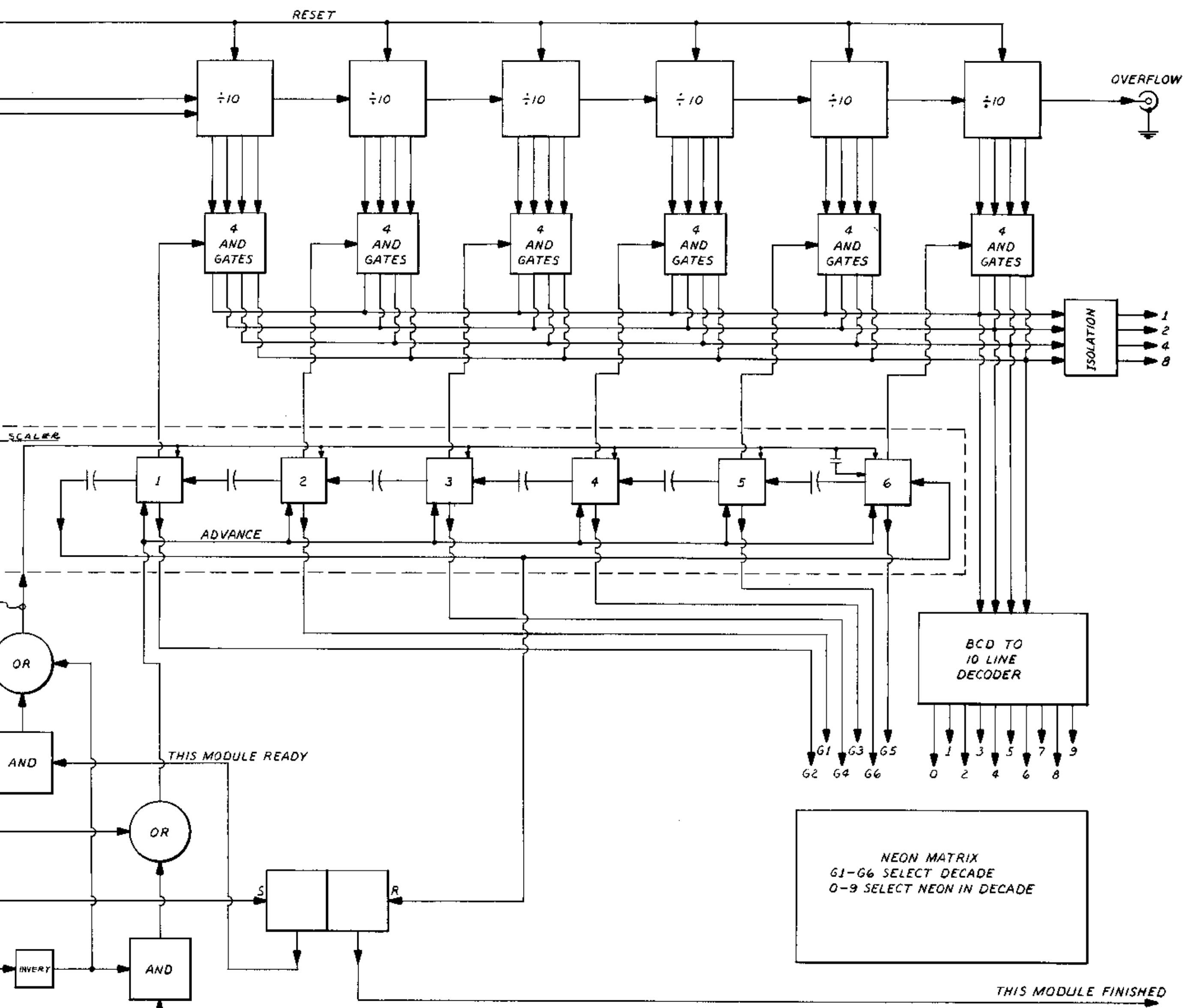
BIN/MODULE CONNECTOR PIN ASSIGNMENTS FOR AEC STANDARD NUCLEAR INSTRUMENT MODULES PER TID-20893

Pin	Function	Pin	Function
1	+3 volts	23	Reserved
2	- 3 volts	24	Reserved
3	Spare Bus	25	Reserved
4	Reserved Bus	26	Spare
5	Coaxial	27	Spare
6	Coaxial	*28	+24 volts
7	Coaxial	*29	- 24 volts
8	200 volts dc	30	Spare Bus
9	Spare	31	Carry No. 2
*10	+6 volts	32	Spare
*11	- 6 volts	*33	115 volts ac (Hot)
12	Reserved Bus	*34	Power Return Ground
13	Carry No. 1	35	Reset
14	Spare	36	Gate
15	Reserved	37	Spare
*16	+12 volts	38	Coaxial
*17	- 12 volts	39	Coaxial
18	Spare Bus	40	Coaxial
19	Reserved Bus	*41	115 volts ac (Neut.)
20	Spare	*42	High Quality Ground
21	Spare	G	Ground Guide Pin
22	Reserved		

**These pins are installed and wired in parallel in the ORTEC 401A Modular System Bin.*



RESET
INPUT
INPUT DISC. ADJ. ± .1-11V.
÷10
÷10
4 AND GATES
4 AND GATES
GATE INDICATOR
GATE
AND
AND
ISOLATION
ON
OFF
RING SCALER
1
2
ADVANCE
SYSTEM GATE
*SEE NOTE.
SYSTEM PRESET
OR
SYSTEM RESET
PREVIOUS MODULE FINISHED
AND
THIS MODULE READY
RESET
MASTER
SLAVE
NORMAL
OR
OR
PRINT ADVANCE
OR
RESET
S
R
PRINT
INVERT
AND
1KC SCAN OSC.
* NOTE-



* NOTE-
THIS SIGNAL ALLOWS SCANNER TO COUNT. WHEN FALSE CUTS ALL STAGES OFF. WHEN GOING TRUE, TURNS ON #6 GATING MOST SIG. DECADE ONTO OUTPUT LINES.

UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES
TOLERANCES
FRACTION ±
DECIMALS ±
ANGLES ±
SURFACE FINISH √ RMS
APPLIED PRACTICES.

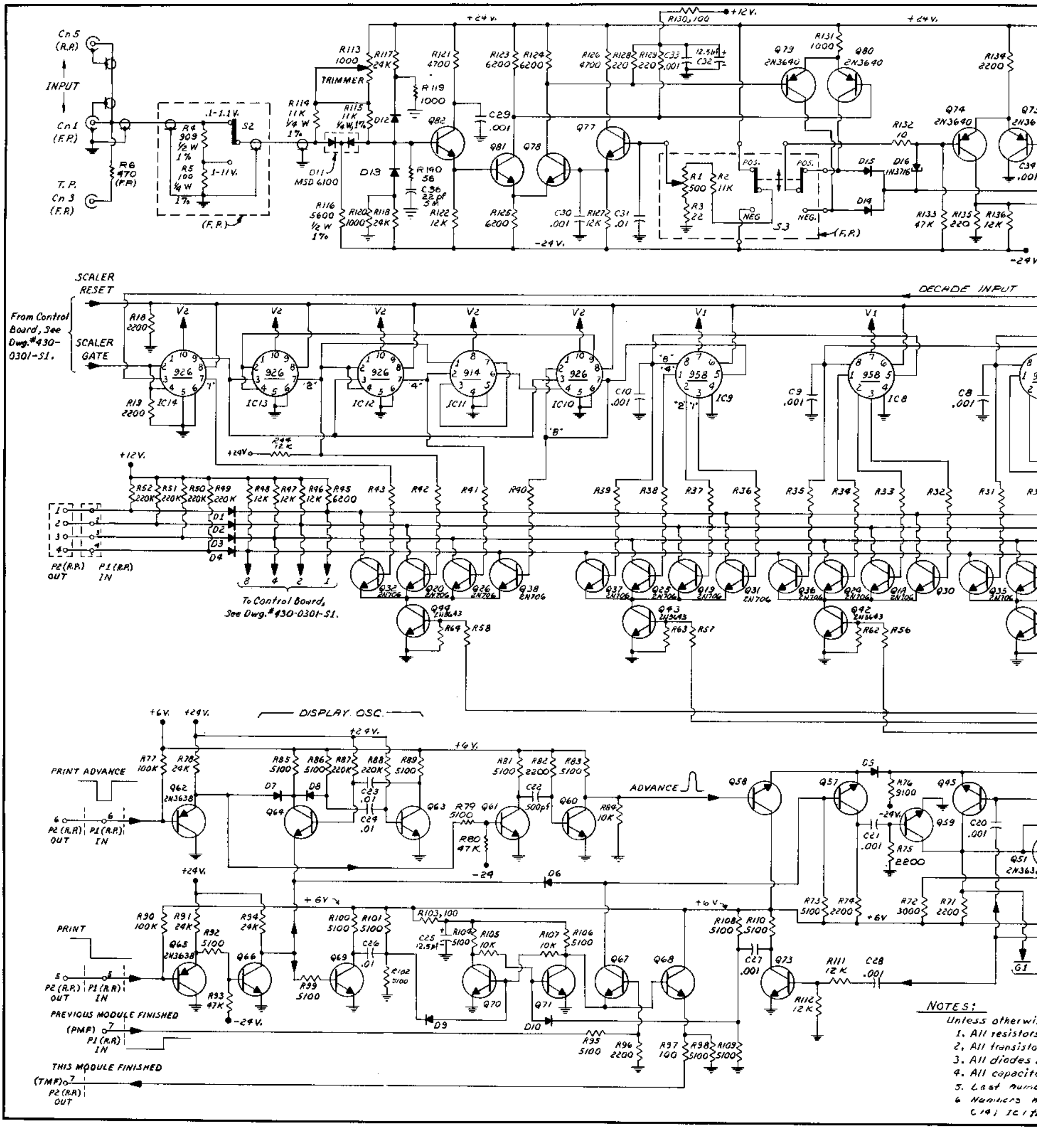
REVISIONS

ORTEC
OAK RIDGE TECHNICAL ENTERPRISES CORPORATION
OAK RIDGE TENNESSEE

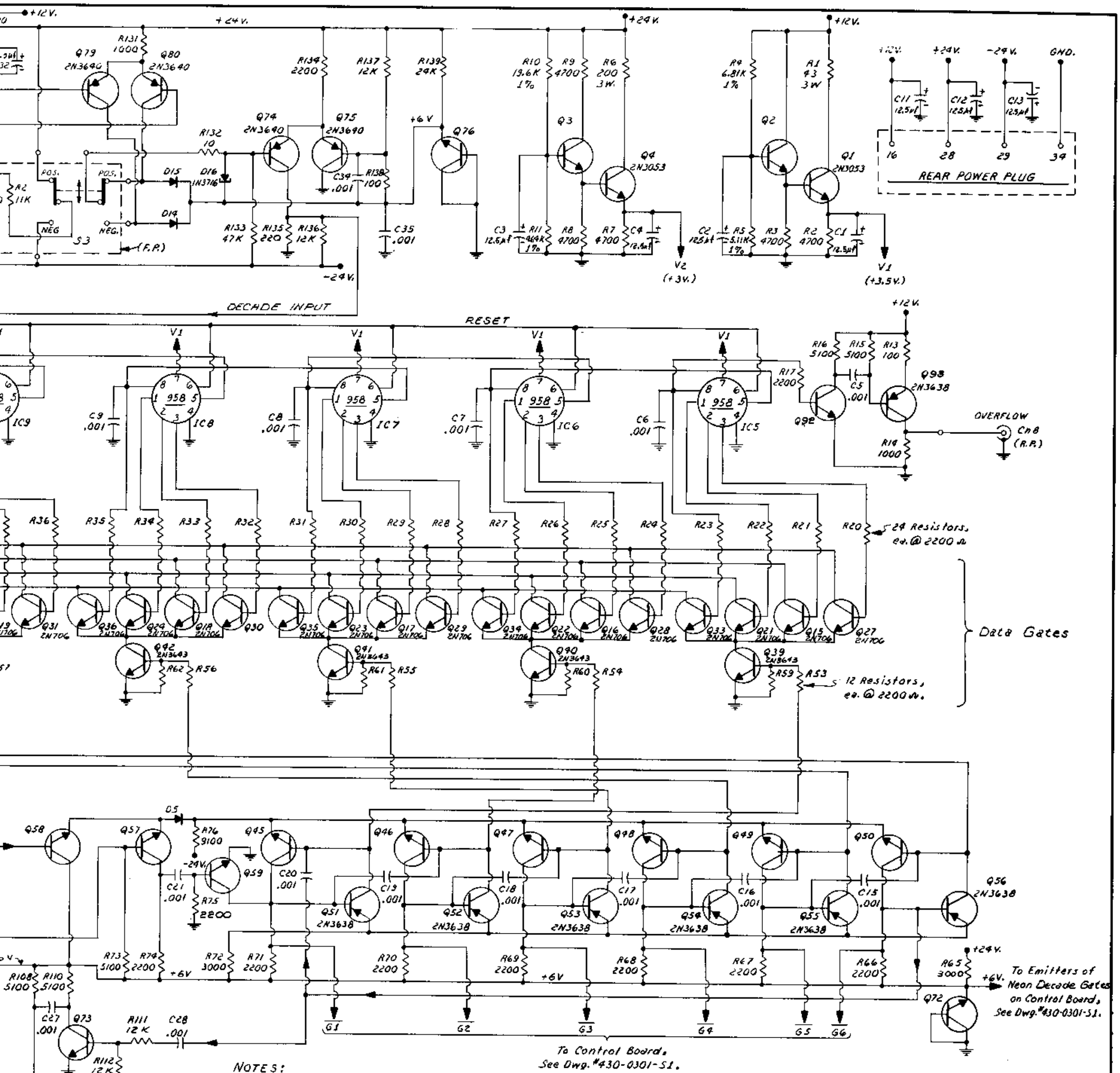
TITLE: SCALER BLOCK DIAGRAM

DRAFTSMAN: L. C. Keith 5-28-68 | ENG APPROVAL: B. J. Moore | ENG: Bill Moore
DRAWING NO: 430-0100-B1

The transistor types installed in your instrument may differ from those shown in the schematic diagram. In such cases, necessary replacements can be made with either the type shown in the diagram or the type actually used in the instrument.



INPUT
Cn 5 (R.P.)
Cn 1 (F.P.)
T.P. Cn 3 (F.P.)
R6 470 (F.P.)
S2
(F.P.)
TRIMMER
D11 MSD 6100
+24 V.
-24 V.
+12 V.
R130, 100
S3
POS.
NEG.
(F.P.)
SCALER RESET
SCALER GATE
From Control Board, See Dwg. #430-0301-S1.
DECADE INPUT
IC14
IC13
IC12
IC11
IC10
IC9
IC8
P2 (R.P.) OUT
P1 (R.P.) IN
To Control Board, See Dwg. #430-0301-S1.
DISPLAY OSC.
PRINT ADVANCE
ADVANCE
PRINT
PREVIOUS MODULE FINISHED
(PMF)
THIS MODULE FINISHED
(TMF)
NOTES:
Unless otherwi
1. All resistors
2. All transisto
3. All diodes
4. All capacit
5. Last num
6. Numbers



NOTES:

Unless otherwise specified:

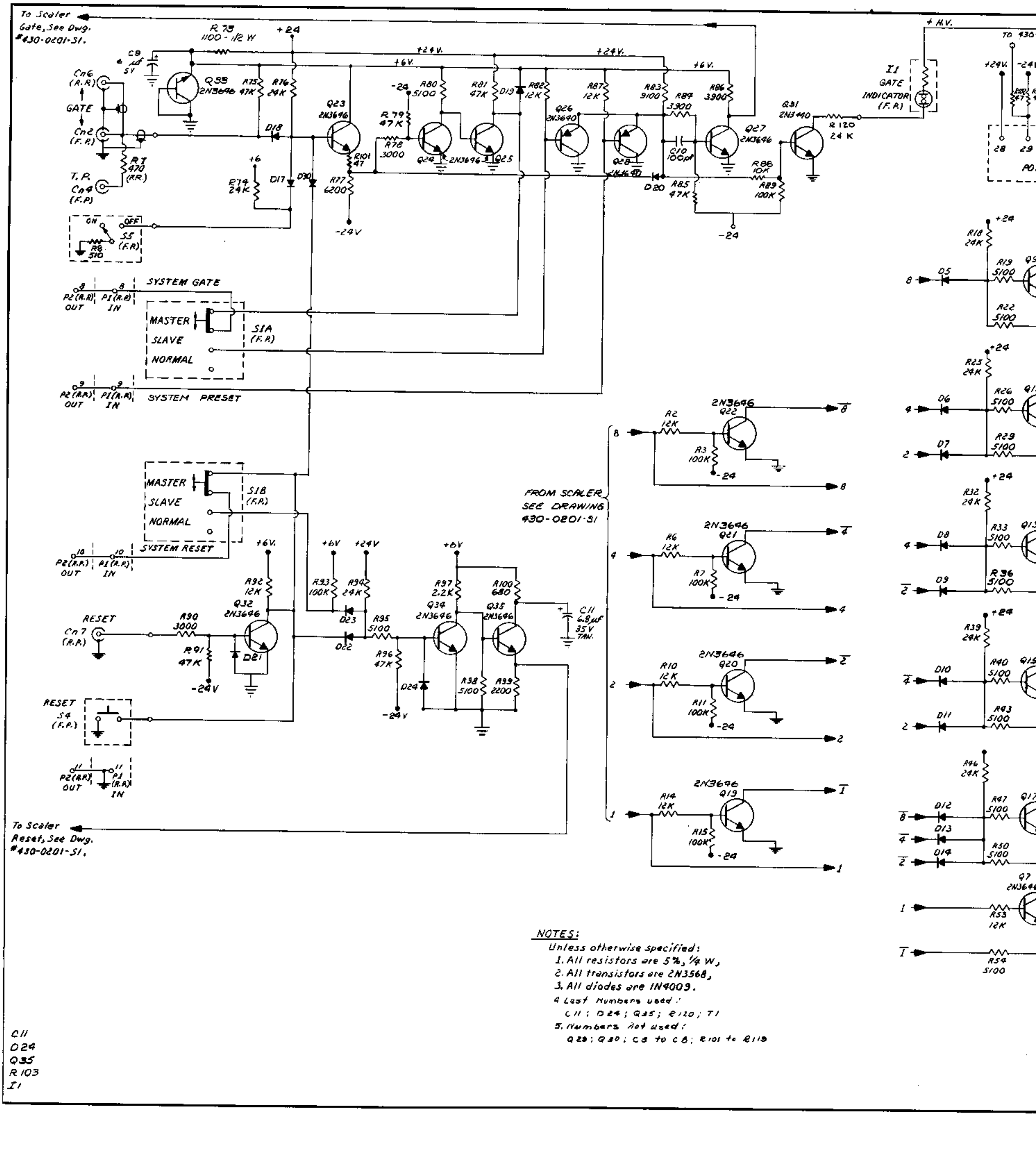
1. All resistors are 5%, ¼W,
2. All transistors are 2N3646,
3. All diodes are IN4009
4. All capacitors are 6.8 μf, 35 V. TAN.
5. Last numbers used: C36; IC14; Q93; R140; D16
6. Numbers not used: C14; IC1 to IC4; Q5 to Q14; R14, Q83 to Q91

UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES
TOLERANCES
FRACTION ±
DECIMALS ±
ANGLES ±
SURFACE FINISH √ RMS
APPLIED PRACTICES

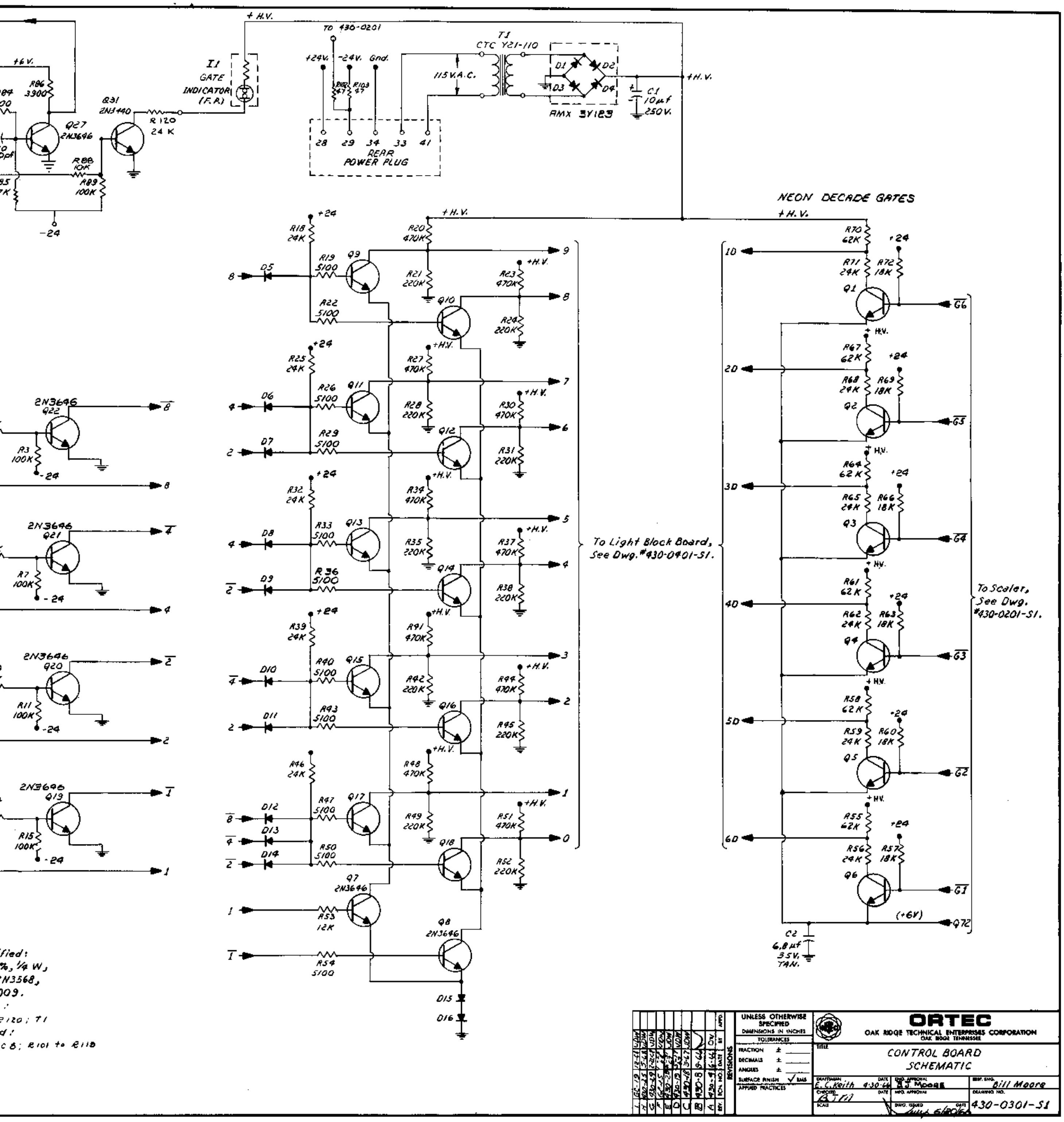
ORTEC
OAK RIDGE TECHNICAL ENTERPRISES CORPORATION
OAK RIDGE TENNESSEE

TITLE: SCALER - SCHEMATIC

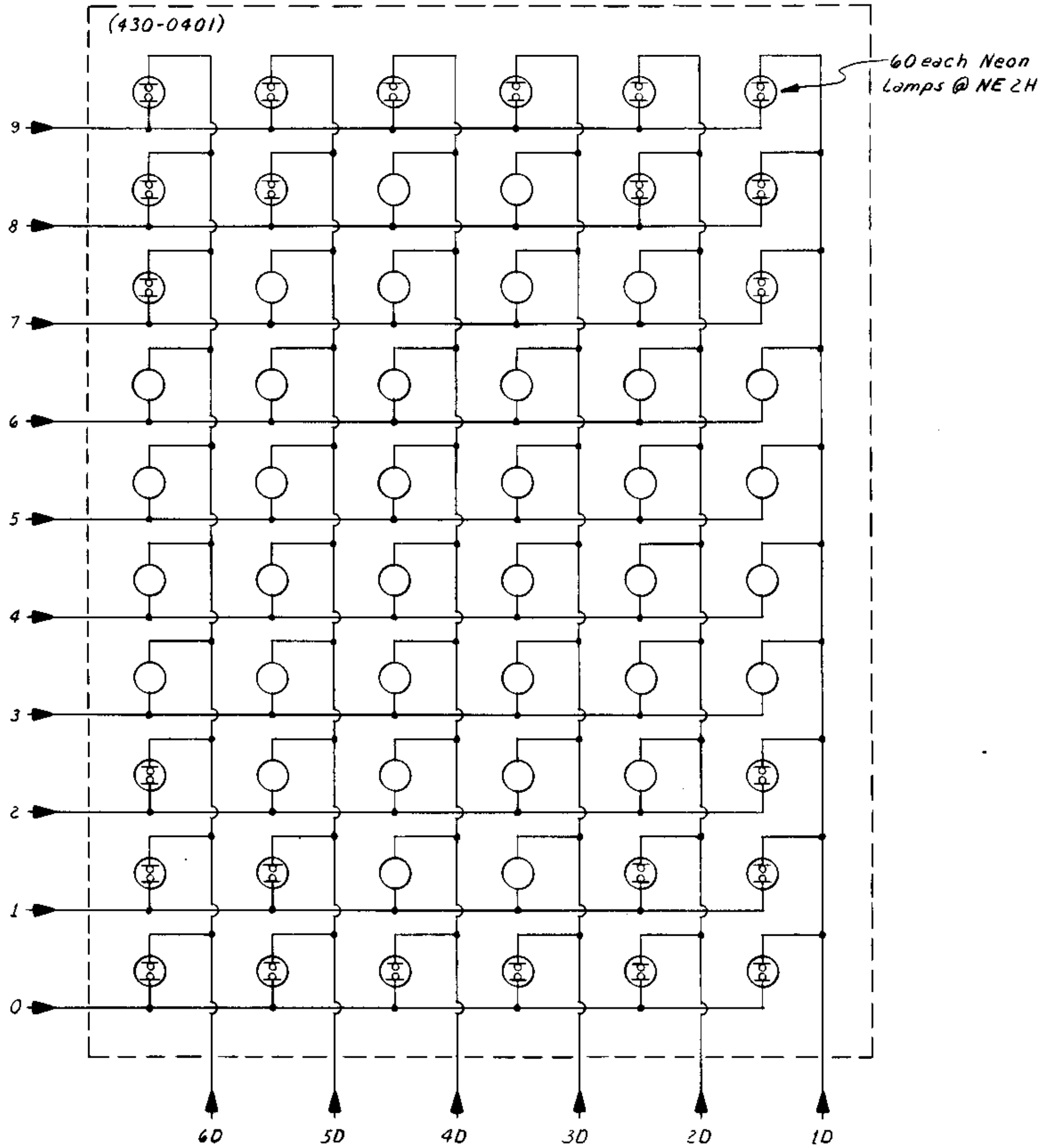
DRAFTSMAN: E.L. Keith — DATE: 4-23-66 — ENG. APPROVAL: B.J. Moore
ENG.: Bill Moore
DRAWING NO.: 430-0201-S1



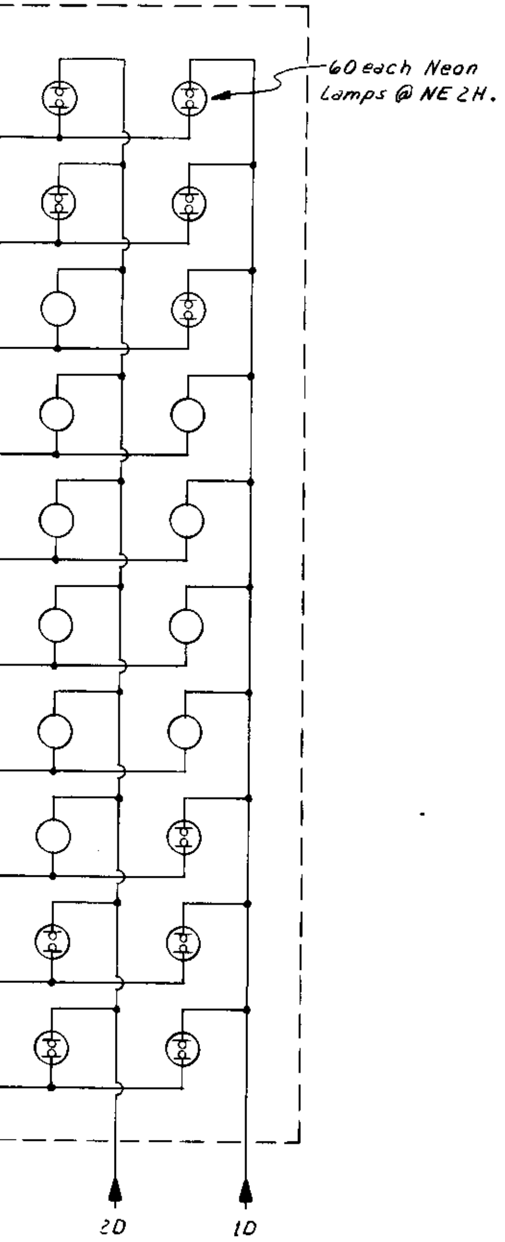
To Scaler Gate, See Dwg. #430-0201-S1.
To Scaler Reset, See Dwg. #430-0201-S1.
GATE
RESET
SYSTEM GATE
SYSTEM PRESET
SYSTEM RESET
MASTER
SLAVE
NORMAL
S1A (F.P.)
S1B (F.P.)
S4 (F.P.)
S5 (F.P.)
I1 GATE INDICATOR (F.P.)
FROM SCALER SEE DRAWING 430-0201-S1
NOTES:
Unless otherwise specified:
1. All resistors are 5%, 1/4 W,
2. All transistors are 2N3568,
3. All diodes are 1N4009.
4. Last Numbers used: C11; D24; Q35; R120; I1
5. Numbers not used: Q29; Q30; C3 to C8; R101 to R119
C11
D24
Q35
R103
I1



+H.V.
TO 430-0201
T1
CTC Y21-110
+24V. -24V. Gnd.
115 V.A.C.
D1 D2 D3 D4
C1 10µf 250V.
AMX 3Y183
I1 GATE INDICATOR (F.P.)
Q31 2N3440
R120 24 K
Q27 2N3646
R86 3900
R88 10K
R89 100K
-24
28 29 34 33 41
REAR POWER PLUG
NEON DECADE GATES
To Light Block Board, See Dwg. #430-0401-S1.
To Scaler, See Dwg. #430-0201-S1.
2N3646 Q22
2N3646 Q21
2N3646 Q20
2N3696 Q19
Q7 2N3646
Q8 2N3646
D15
D16
C2 6.8µf 35V. TAN.
UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES
TOLERANCES
FRACTION ±
DECIMALS ±
ANGLES ±
SURFACE FINISH
APPLIED PRACTICES
REVISIONS
ORTEC
OAK RIDGE TECHNICAL ENTERPRISES CORPORATION
OAK RIDGE TENNESSEE
CONTROL BOARD SCHEMATIC
E. C. Keith 4-30-66
Bill Moore
430-0301-S1



(430-0401)
60 each Neon Lamps @ NE 2H.
9
8
7
6
5
4
3
2
1
0
6D
5D
4D
3D
2D
1D



NOTE - This Light Bd. Schematic mates with the Schematic of either 1 of 2 Control Bd's. as shown on Dwg's. 430-0301-S1 and 431-0301-S1.

REVISIONS		
REV. ECN. NO.	DATE	BY APPD.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES
TOLERANCES
FRACTION ±
DECIMALS ±
ANGLES ±
SURFACE FINISH √ RMS
APPLIED PRACTICES

ORTEC
OAK RIDGE TECHNICAL ENTERPRISES CORPORATION
OAK RIDGE TENNESSEE

TITLE: LIGHT BLOCK BOARD SCHEMATIC

DRAFTSMAN: E.C. Keith	ENG. APPROVAL: R.J. Moore	RESP. ENG.: Bill Moore
CHECKED: WLP DATE: 5-24-66	MFG. APPROVAL	DRAWING NO.
SCALE: NONE	DWG. ISSUED DATE: 6-10-66	430-0401-S1