INSTRUCTION MANUAL
442
LINEAR GATE STRETCHER

Serial No. _____

Purchaser _____

Date Issued _____

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TABLE OF CONTENTS

LIST OF FIGURES AND ILLUSTRATIONS

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ORTEC warrants its nuclear instrument products to be free from defects in workmanship and materials, other than vacuum tubes and semiconductors, for a period of twenty-four months from date of shipment, provided that the equipment has been used in a proper manner and not subjected to abuse. Repairs or replacement, at ORTEC option, will be made without charge at the ORTEC factory. Shipping expense will be to the account of the customer except in cases of defects discovered upon initial operation. Warranties of vacuum tubes and semiconductors, as made by their manufacturers, will be extended to our customers only to the extent of the manufacturers' liability to ORTEC. Specially selected vacuum tubes or semiconductors cannot be warranted. ORTEC reserves the right to modify the design of its products without incurring responsibility for modification of previously manufactured units. Since installation conditions are beyond our control, ORTEC does not assume any risks or liabilities associated with methods of installation other than specified in the instructions, or installation results.

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ORTEC instruments not in warranty may be returned to the factory for repairs or checkout at modest expense to the customer. Standard procedure requires that returned instruments pass the same quality control tests as those used for new production instruments. Please contact the factory for instructions before shipping equipment.

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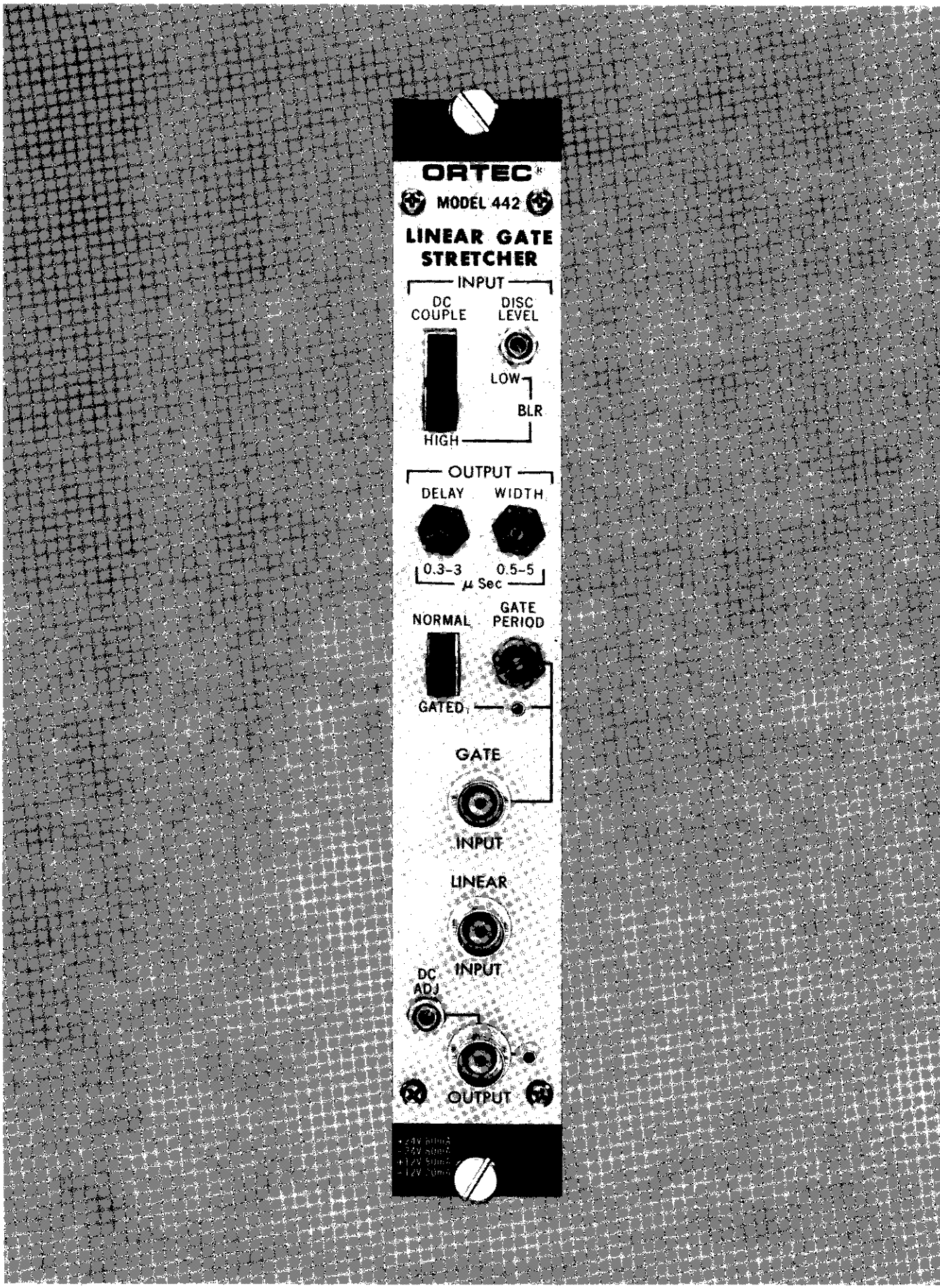
Shipments should be examined immediately upon receipt for evidence of external or concealed damage. The carrier making delivery should be notified immediately of any such damage, since the carrier is normally liable for damage in shipment. Packing materials, waybills, and other such documentation should be preserved in order to establish claims. After such notification to the carrier, please notify ORTEC of the circumstances so that we may assist in damage claims and in providing replacement equipment if necessary.


ORTEC
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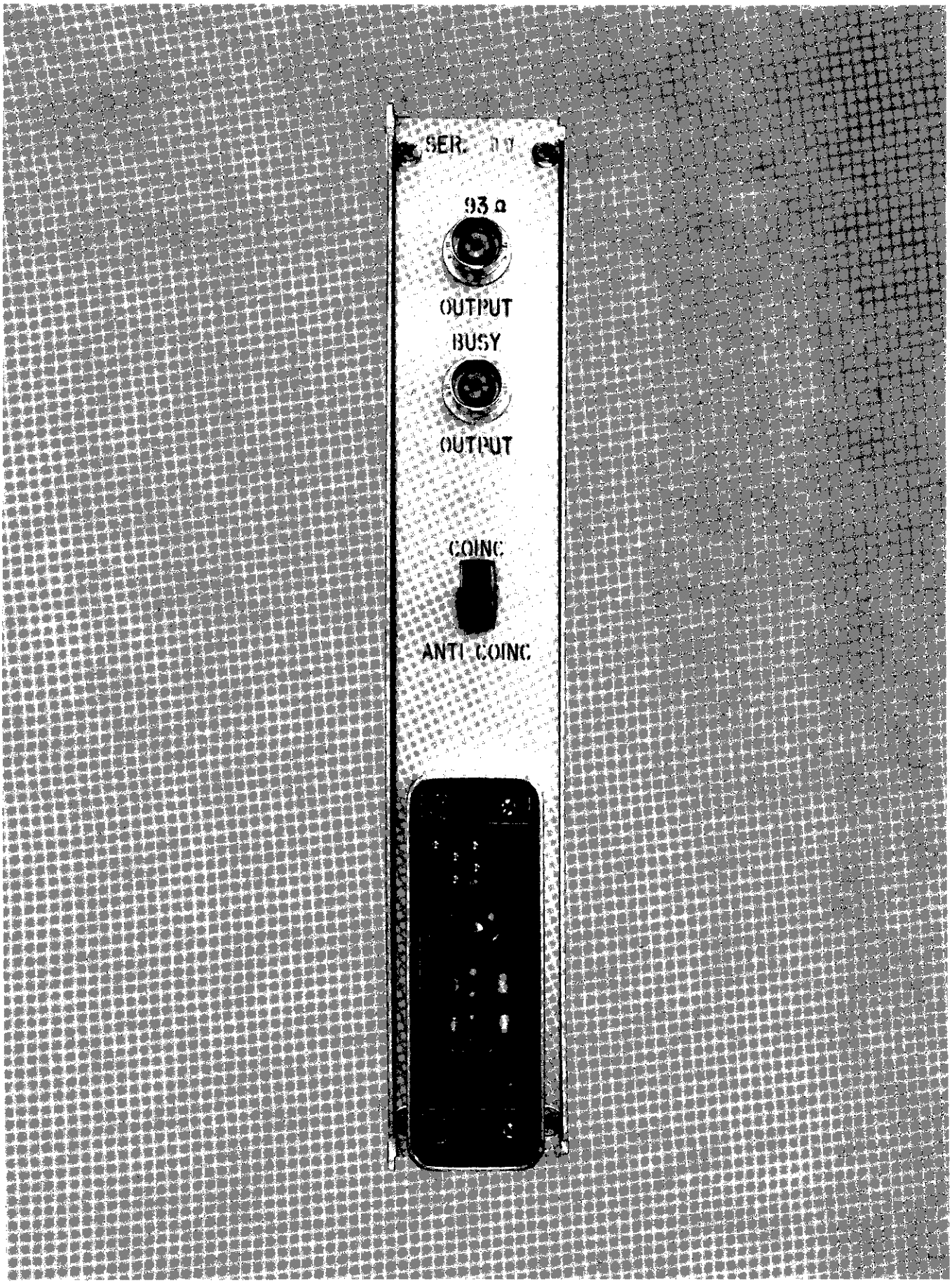
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ORTEC 442 LINEAR GATE AND STRETCHER

1. DESCRIPTION

1.1 General

The ORTEC 442 Linear Gate and Stretcher is designed to increase the duration of short input pulses by stretching their peak amplitudes for a required minimum pulse width. This effectively reduces the bandwidth requirements of analog-to-digital converters in multichannel pulse height analyzers, and improves the resulting linearity. The linear gate included in the 442 permits selective control of the acceptance of input pulses, and is also used to prevent positive-on-positive pulse pile-up.

1.2 Basic Functions

The purpose of the 442 is to accept linear signals, during its permissive gating periods, from any linear source, and to reshape the input signal as required to provide a suitable waveform into a circuit which measures the peak amplitude. Any reshaping of the input pulse must retain the linear parameter of the input signal, which is its relative peak amplitude. The pulse width of the input is unimportant except from the practical viewpoint of having the peak amplitude exist long enough to permit accurate response and measurement.

The input gate can be controlled from an external source, and operated in either a coincidence or an anticoincidence mode. The gate period generator will be triggered on the leading edge of a gate input pulse, and continue for the effective period set by the front panel adjustment. The Gate Period must overlap the linear input pulse peak for coincidence mode operation, or must overlap the discriminator response for anticoincidence mode.

A linear input pulse must exceed the adjusted discriminator level to initiate a response in the 442. When the discriminator fires, it initiates the stretch action unless the gate control is in the external coincidence mode and a gate pulse is not present. The input gate remains open only until the peak of the linear pulse has been detected, and is again closed to prevent pileup. An output pulse will be generated if a peak is detected, and occurs at an adjusted delay following the input peak for an adjusted width. Both the delay and width adjustments are front panel controls on the 442. The input gate cannot be opened again until the output pulse has been completed *and* the linear input pulse has permitted the discriminator to reset. This internal logic prevents pulse pileup and false amplitude outputs for the system.

Short duration linear pulses are associated normally with biased amplifiers. The 442 can be used in this, or any other, system to assure an adequate duration of the peak amplitude where a pulse width might be too short, or where the width variations would otherwise produce a non-linear response or measurement. It may be used at any point in the linear system after a basic linear amplifier, and its gating function permits logical placement directly after the linear amplifier. For best system performance the 442 should precede the biased amplifier.

2. SPECIFICATIONS

LINEAR INPUT

POLARITY: Positive unipolar, or bipolar with positive portion leading

AMPLITUDE: +0.1 to +10 volts, linear range; ±12 volts maximum

RISE TIME: 100 nsec to 10μsec

INPUT IMPEDANCE: ~1000 ohms

INPUT CIRCUIT: Switch selectable, DC-Coupled, or DC-Restored for either High or Low count rate

GATE INPUT

FUNCTION: Optional external control for switch selectable coincidence or anticoincidence mode triggering

INPUT PUSLES: Standard NIM[1] Slow Logic pulse, triggers selected gate function at +3 volts (100 nsec min width); protected to ±25 volts

INPUT DISCRIMINATOR

FUNCTION: Adjustable to eliminate response to small input (noise) pulse amplitudes. Initiates stretcher response when triggered

RANGE: +0.1 to 1 volt, front panel adjusted

DURATION: Remains triggered while input level exceeds adjusted sensitivity

LINEAR OUTPUT

POLARITY: Positive

AMPLITUDE: +0.1 to +10 volts, equal to peak of the accepted linear input pulse

RISE TIME: 300 nsec

WIDTH: Adjusted by front panel control; range 0.5 to 5μsec

DELAY: Adjusted by front panel control; range 0.3 to 3μsec after input pulse peak

OUTPUT IMPEDANCE: <1 ohm on front panel, 93 ohms on rear panel

NON-LINEARITY: <0.1% with pulse amplitude droop <0.5 millivolts/μsec

BASELINE ADJUST: ±1.5V DC Adjust on front panel

BUSY OUTPUT

FUNCTION: Produces a pulse equal in width to the internally created dead time

BUSY: +5 volts nominal, when linear pulse cannot be accepted

NOT BUSY: 0 volts nominal, when linear pulse can be accepted

OUTPUT IMPEDANCE: <10 ohms

FRONT PANEL CONTROLS

DC-COUPLE, BLR HIGH, BLR LOW: Three position slide switch, selects input circuit desired

DISCRIMINATOR LEVEL: Screwdriver potentiometer, adjusts sensitivity level for input discriminator; range +0.1 to 1V

OUTPUT DELAY: Screwdriver potentiometer, adjusts delay period from input pulse peak to start of output pulse; range 0.3 to 3μsec

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[1] NIM Standard Logic Pulses in accordance with preferred practices of AEC Report TID-20893 (Revised).

OUTPUT WIDTH: Screwdriver potentiometer, adjusts width of the output pulse; range 0.5 to 5μsec

NORMAL/GATED: Switch, selects exclusion (NORMAL) or inclusion (GATED) of optional external gating function

GATE PERIOD: Screwdriver potentiometer, adjusts duration of gating control from leading edge of Gate Input pulse; range 0.5 to 5μsec. Includes test point for monitoring adjusted gate period.

OUTPUT DC ADJUST: Screwdriver potentiometer, permits adjustment of output dc level between ±1.5V.

REAR PANEL CONTROL

COINCIDENCE/ANTICOINCIDENCE: Slide switch, selects effective mode for Gate Input function

FRONT PANEL CONNECTORS (All type BNC)

LINEAR INPUT: Accepts positive unipolar or bipolar pulses; linear range +0.1 to +10 volts

OUTPUT: Furnishes linear positive output pulses through $Z_o < 1\Omega$. Includes test point

GATE INPUT: Accepts optional NIM[1] Slow Logic pulses for Gated control, with selected coincidence or anticoincidence mode and adjusted effective period. Includes test point

REAR PANEL CONNECTORS (Type BNC)

OUTPUT: Furnishes linear positive output pulses through $Z_o = 93\Omega$

BUSY: Furnishes +5 volt nominal signal through $Z_o < 10\Omega$ through all periods when input pulses cannot be accepted. May be used for external control or for monitoring internally created dead time.

GAIN: Unity

INTEGRAL NONLINEARITY: <0.1%, for pulse rise time >100 nsec and pulse width >400 nsec

COUNTING RATE: DC-Coupled throughout when DC-Coupled Input is selected. The centroid of a pulser spectrum at 85% of full scale will shift less than 0.1% when modulated by 5×10^4 counts/sec of random signals from ^{137}Cs source-detector combination with photopeak at 70% of full scale (DC-Coupled Mode, $\tau \doteq 1\mu$sec). When DC restorer modes are used, count rate is dependent on shaping amplifier time constants and pulse undershoot.

OPERATING TEMPERATURE RANGE: 0 to 50°C

TEMPERATURE STABILITY: Gain shift less than 0.01%/°C, 0 to 50°C

POWER REQUIREMENTS:

+24V	69mA	+12V	75mA
-24V	76mA	-12V	14mA

RELATED EQUIPMENT

The ORTEC 442 can be used effectively in any linear pulse system where it is advantageous to reshape a linear signal to a constant width. The output can be connected into a biased amplifier, the ADC input of a multichannel anlayzer, a single channel analyzer, or any of the ORTEC 400 Series linear circuit modules. The input should have been amplified into the linear range of 0.1 to 10 volts (maximum) prior to the 442.

ORDERING INFORMATION

WEIGHT (Shipping): 4 pounds (1.9 kg)

WEIGHT (Net): 2 pounds (0.9 kg)

DIMENSIONS: Standard single width module (1.35 by 8.714 inches) per TID-20893 (Rev.)

3. INSTALLATION

3.1 General Installation Considerations

The 442 is designed for installation in a standard Bin and Power Supply, such as the ORTEC 401A/402A. Since this enclosure is intended for rack mounting, it is necessary to ensure that any vacuum tube equipment operated in the same rack will have adequate cooling air circulation to prevent any localized heating of the 442 transistorized circuits. The temperature of equipment mounted in racks can easily exceed the recommended maximum unless precautions are observed. The ORTEC 442 should not be subjected to temperatures in excess of 120°F (50°C).

3.2 Connection to Power

The ORTEC 442 contains no internal power supply, and obtains its dc operating power from the standard Bin and Power Supply in which it is installed. Always turn power off for the Bin and Power Supply before inserting or removing any modules. The ORTEC 400 Series of modular instruments are designed such that it is not possible to overload the power supply with a full complement of modules in the bin. However, this may not be true when the bin contains modules other than those of ORTEC design; check the power supply for any overload conditions by testing the dc power levels after insertion of all modules.

The ORTEC 442 may be operated outside the 401A/402A Bin and Power Supply, using a power extension cable. Be sure that the cable used accounts properly for the grounding circuits recommended in AEC standards of TID-20893 (Rev.). Both clean and dirty ground connections are included to ensure proper reference voltage feedback into the power supply, and these must be preserved by the remote cable. Be careful to avoid ground loops when the module is not physically installed in the bin during operation.

3.3 Linear Input Connection

Linear input pulses can be furnished from any ORTEC linear module of the 400 Series. These include amplifiers, delay circuits, biased amplifiers, gates, and other pulse handling equipment. It is recommended that the 442 be used prior to the biased amplifier when both modules are used in a system. The effective input range will be from the adjusted discriminator level (+0.1 to 1V) up through +10 volts.

When the linear input signals are furnished through a cable more than four feet long (approximately), the input should be terminated with the characteristic impedance of the cable. This can usually be avoided when shorter cables are used.

3.4 Linear Output Connections

The shaped linear output pulses can be furnished into any other ORTEC Series 400 linear module, or directly into the ADC input of a multichannel analyzer. It is important to preserve the pulse shape and linear amplitude relationship of the output, as it appears when accepted into subsequent instrument modules. Either of two standard output impedances may be selected, according to the type and length of interconnecting cable and the input impedance of the instrument to which it is connected. The output is available through a front panel connector, with an output impedance of less than 1 ohm, or through a rear panel connector, with Z_O = 93 ohms. For most applications, the 1 ohm front panel output connector can be used, with a short cable length, to transfer the output signal into the (normally) high input impedance of the next module. When the output signals must be furnished through cable lengths greater than approximately four feet, proper resistive termination of the cable is required in order to preserve the linear output pulses and prevent oscillations. Either of two convenient methods can be selected for the 442 outputs, when termination is required.

One method is a series type termination, using the rear panel 93Ω Output connector and an appropriate length of 93 ohm coaxial cable to transfer the signal into the next module or instrument. The input impedance of the next equipment will probably be on the order of 1000 ohms or more. The total amplitude of each output pulse will be divided between the 93 ohm output impedance of the 442 and the input impedance of the next module, so a high input impedance is desirable when this series termination method is used.

An alternate method depends upon shunt termination at the remote end of the cable. For this, use the front panel 1Ω Output connector, and whatever type coaxial cable is desired. Then use a BNC Tee at the input to the next module, to accept both the cable and a BNC Terminator, selected to match the characteristic impedance of the cable when connected in parallel with the instrument's input impedance. For convenience, ORTEC stocks a limited quantity of BNC Tee connectors, and both 50 and 100 ohm BNC Terminators.

3.5 Gate Input

When Gate Input signals are required, they will be furnished through the BNC connector on the front panel of the 442. The function of an input pulse will be to trigger the 442 Linear Input gate for an adjusted Gate Period. The function must be selected as either Coincidence or Anticoincidence by a rear panel slide switch.

Gate Input pusles are effective when they rise through +3 volts for a period of at least 100 nsec. A standard NIM Slow Logic positive pulse source may be used. The Gate Input circuit is protected to ±25 volts, so a wide variety of alternate sources can also be used to initiate this control. When operating in the Coincidence mode, the Gate Period must be triggered before the peak of the linear input pulse and must be continued until after the peak. When operating in the Anticoincidence mode, the Gate Period must be triggered prior to a discriminator response to the linear input and must be continued until the discriminator has been reset.

No Gate Input is required if the front panel NORMAL/GATED switch is set at NORMAL. Likewise, if the front panel switch is set at GATED, and the rear panel mode selector is set at ANTI-COINC, a Gate Input pulse is not required except when a linear input signal is to be rejected. When these switches are set for GATED and COINCIDENCE, respectively, a linear input pulse will be accepted only if it is accompanied by a time coincident Gate Input pulse.

3.6 Connection for Busy Output

The duration of each Busy Output signal is from the time an input pulse peak is detected until the resulting output pulse has been furnished and the input discriminator has been reset. This identifies each period during which a new input pulse cannot be accepted in the 442. This output can be integrated externally to indicate the average dead time.

4. OPERATION

4.1 Selection of Input Circuit

Any of three circuit connections can be selected with the slide switch at the top of the front panel. They are DC-Couple, BLR Low, or BLR High. The proper selection will depend on the type of output circuit in the module from which the linear input pulses are furnished to the 442, and the relative counting rate.

The DC-Coupled switch position provides an optimum signal transfer circuit with 1000 ohms input impedance if the pulses are furnished from an amplifier with a dc-coupled output and a properly adjusted zero baseline. If the source does not include baseline restoration, use a capacitive coupling into the 442 and select either Low or High Baseline Restorer in the 442.

For any ac-coupled signal input, select one of the DC-Restorer input circuits in the 442. There is no precise dividing line, because of the various shaping time constants which may be affecting the pulse shape furnished to the 442. For 1μsec pulses, the division is approximately 15,000 counts per second. If bipolar pulses are applied to the input the DC-Coupled or BLR Low configurations must be selected. The most practical method of selecting between High and Low is observation of the Output, using the circuit which provides the better results.

4.2 Discriminator Level Adjustment

The purpose for the adjustment of the discriminator sensitivity level is to prevent response to all noise pulses. Therefore, it should be adjusted high enough in its +0.1 to 1 volt range to ensure discrimination against the maximum noise amplitude which may exist at the input to the 442 in the system. Since the logic in the 442 prevents response to a new input pulse until the discriminator is reset, but permits acceptance at that time unless an output pulse has not been completed, too high a setting of the discriminator level can permit a small amount of pileup to occur if the input pulse has a very long time constant decay. Although this interference is possible, it is unlikely in most applications. Still, an unnecessarily high adjustment is not recommended.

4.3 Output Delay Adjustment

The adjustment of the delay permits a control for normalizing timing in the system in which the 442 is included. The delay period is measured from the time the internal stretch amplifier senses a peak amplitude in the accepted linear input pulse, and is adjustable through the range of 0.3 to 3μsec. At the end of the delay period, the output gate is opened and an output pulse is furnished to the next instrument in the system.

4.4 Output Width Adjustment

The purpose of the stretch circuit is to provide an output pulse with a fixed and known width. The range of the control is 0.5 to 5μsec, and its proper setting will be determined by the input requirements of subsequent instruments in the system. Each output pulse will have the adjusted width, regardless of the width(s) of linear pulses furnished to the 442 input.

4.5 Output DC Adjustment

In normal usage the quiescent level for the output, through both the front and rear panel connectors, should be at ground potential. Use the test point for the front panel Output, and adjust the screwdriver control as necessary to set the level at ground potential when there are no output signals. When using the DC input on some analyzers it is necessary that the signal source have a quiescent dc level other than zero, when the 442 is used in such applications adjust the output dc level as required.

4.6 Gated Operation

No Gate Input pulse is required if the front panel slide switch is set at Normal. Likewise, if the slide switch is set at Gated and the mode selector on the rear panel is set for Anti-Coincidence, linear input pulses will be accepted when there is no signal through the Gate Input connector. Whenever a signal is furnished through the Gate Input with Gated Anti-Coincidence effective, all linear input signals are inhibited throughout the Gate Period. To be effective, the Gate Period must be adjusted to overlap the period of discriminator response to any pulse which is to be inhibited by the Anti-Coincidence signal; if the linear input triggers the discriminator before the Gate Input, or if the Gate Period

terminates prior to discriminator recovery, there will be an output, but the amplitude will not usually duplicate a peak input amplitude.

When the 442 is set for Gated Coincidence operation, a linear input signal is accepted for stretching if and only if there is a time coincident Gate Input. The Gate Input signal must occur before the peak amplitude of the linear input pulse, and the Gate Period must be long enough to continue the control beyond the internal detection of the peak amplitude.

Refer to Section 6.2.1 for linear gate pedestal adjustment procedures.

4.7 Overall Logic

When an input pulse arrives at the Linear Input, it is applied directly to the discriminator. As its amplitude rises through the discriminator threshold, the discriminator may be fired or it may still be set because of not having recovered from a previous input pulse. The linear input pulse will not be accepted unless the discriminator has recovered prior to the new pulse; it will also be rejected if (1) an output pulse has not been completed for a previously accepted input; (2) the operating mode is Gated Coincidence and no Gate Input has been furnished; or (3) the operating mode is Gated Anti-Coincidence, a Gate Input signal has been furnished, and the Gate Period is in effect. When the discriminator recovers, it will permit the input to be gated on unless (1) the output pulse has not been completed;or (2) external Gate Input logic has closed the linear input circuit. When the output pulse has been completed, the linear input is permissive unless (1) the discriminator is not reset; or (2) external Gate Input logic has closed the linear input circuit.

When the discriminator is triggered prior to a Coincidence Gate Input, but the linear input is otherwise permissive, the linear input signal is not applied to the stretch circuit until the Gate Input signal is furnished. Under these conditions, the linear input signal is applied to the stretch circuit at the Gate Input time; an output signal will result, which has an amplitude equal to (1) the peak input amplitude, or (2) the input amplitude at the end of the adjusted Gate Period (whichever occurs first). Thus, it is important that the gate be triggered during the rise time of the linear input pulse, and that it remain effective until after the peak amplitude has been sensed.

5. CIRCUIT DESCRIPTION

This section provides a brief description of the basic functions of the 442 and the circuit diagram. The block diagram and circuit diagram will be referred to frequently in this section so they should be readily available for reference.

5.1 DC Restorer

The input section of the 442 is a dc restorer which can be by-passed by selecting DC-Coupled with switch S1. If dc restoration is desired, restoration can be selected for either a low or high count rate by S1. The low restoration rate is approximately 5mv/μsec while the high rate is approximately 150mv/μsec. The restoration currents for the low and high modes are approximately 100μamp and 3 milliamp respectively. The restoration rate can be readily changed by changing the value of C1. The restoration circuit is composed of Q1, Q2, Q58, and Q59.

5.2 Buffer Amplifier

The restoration circuit is followed by a non-inverting buffer amplifier (Q3-Q6) with a gain of approximately one. The gain of this stage is given by the ratio of $\frac{R10 + R117}{R10}$. The 442 is dc-coupled from this stage to the output, so an adjustment is provided in each stage to adjust its dc level to zero. Potentiometer R7 should be adjusted so that the output dc level of the buffer amplifier (TP1) is zero volts. The buffer amplifier drives the input gate and the discriminator.

5.3 Input Gate

The 442 input gate (Q7) is a shunt type gate. When the NORM/GATED switch is in the NORM position, Q7 remains off until the peak of the pulse occurs; at this time Q7 saturates, clamping the gate of Q8 to ground. Q7 continues in saturation until the completion of the 442 output pulse and until the linear input pulse falls below the discriminator level. This prevents the 442 from accepting a second pulse until it has completed processing the first pulse, thereby eliminating positive on positive pile-up. Refer to timing diagrams in Figures 5-1 and 5-2.

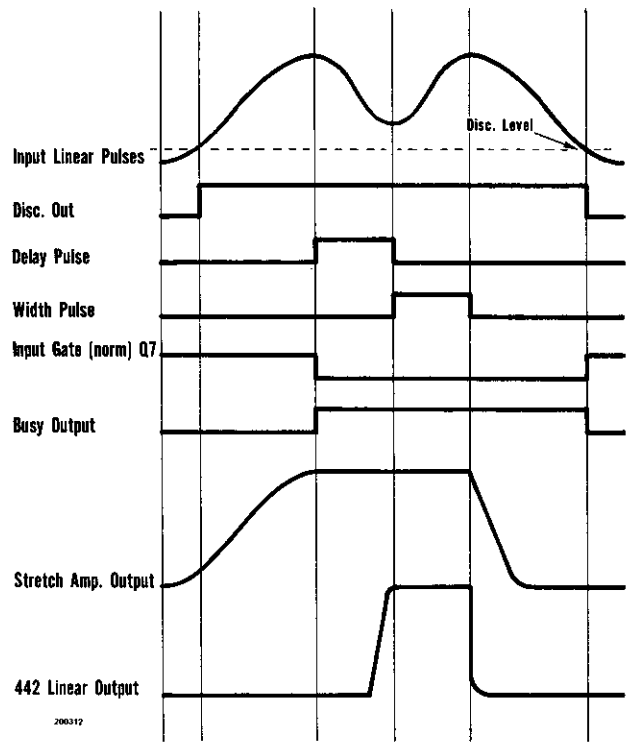


Figure 5-1

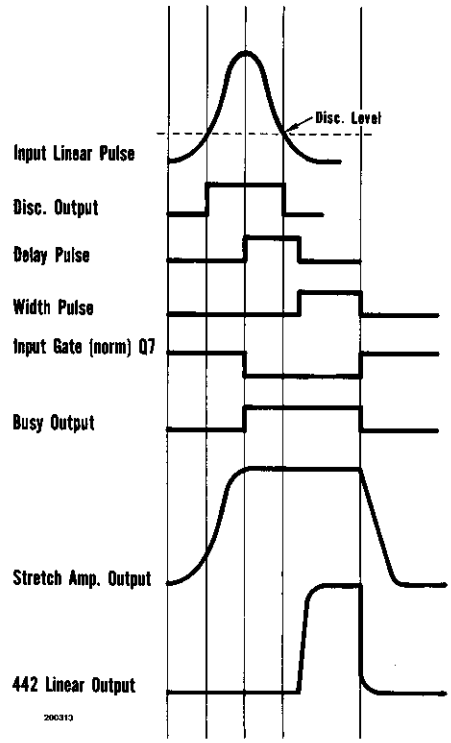


Figure 5-2

When the NORM/GATED switch is in the GATED position and the Coincidence-Anti-Coincidence switch is in the Coincidence position, Q7 will normally be turned on and saturated, clamping the gate of Q8 to ground. In order to open the gate by turning off Q7, a logic pulse must be applied to the Gate Input BNC. This pulse is reshaped to a desired Gate Period by IC5, Q56, and Q57 and applied to the input gate drive circuitry (Q41-Q43) to open the gate (Q7) for the time of the gate period. The gate period must overlap the peak of the linear pulse in order for the 442 to function properly.

If the Anti-Coincidence position is selected, Q7 will act in an inverse manner from what it does in the Coincidence mode; Q7 will normally be off (gate open) except during the gate period, at which time it will be saturated (gate closed). In order for the 442 to operate properly in the Anti-Coincidence mode the Gate Period pulse must totally overlap the time that the linear input is above the discrimination level for the pulse to be blocked. The range of the Gate Period circuit can be changed by changing the value of C45.

5.4 Busy Output

The Busy Output is a measure of the internally created dead time of the 442. This signal begins at the peak of the linear pulse and ends at the completion of the 442 output pulse if the input is below the discriminator level. Refer to timing diagrams in Figures 5-1 and 5-2.

5.5 Discriminator

The discriminator permits the 442 to reject all input pulses which fall below the discriminator level selected, vis. noise pulses. The discriminator level can be varied from 0.1V to 1V by a front panel potentiometer, R75. If the discriminator level is exceeded by an input pulse and the proper gating pulses are applied when operating in the gated mode, a signal is sent to the stretch amplifier switching the current in Q23 and Q24 causing the input pulse to be stretched.

5.6 Stretch Amplifier

The Stretch Amplifier is a non-inverting amplifier composed of transistors Q8-Q25. Q24 is normally conducting, causing current to flow in D5 and keeping the amplifier loop closed. When the input pulse exceeds the discriminator level the current in Q24 is switched to Q23. The stretch capacitor, C17, is

charged through D5 to the peak voltage of the input pulse. After the peak voltage occurs, D5 is back biased and the peak voltage is stored on C17 until Q24 is switched on again at the end of the output pulse. A high input impedance non-inverting amplifier, Q13-Q18, acts as a buffer and driver for the voltage on capacitor C17. This amplifier is included inside the stretch amplifier loop to provide better linearity and stability. Q20-Q22 monitors the voltage across D5 and produces a peak detect signal when D5 transistions to the back biased condition. The peak detect pulse is routed to the control logic to initiate the delay and output width signals.

Potentiometer R18 is provided to adjust the voltage at TP2 to zero volts when the input voltage to Q8 is zero.

5.7 Output Pulse Delay Control

The delay circuit consists of Q48, Q49, and two gates in IC3. The leading edge of the peak detect signal initiates the delay circuit, causing it to produce a pulse of width determined by the setting of R94. The width of the delay pulse can be varied from 300 nsec to 3μsec by varying the setting of R94. The delay range can be increased by increasing the value of C32.

5.8 Output Pulse Width Control

The delay pulse is routed to the output pulse width control circuit (Q46, Q47, and two gates in IC4). The trailing edge of the delay pulse energizes the width circuit, which produces an output pulse from 0.5 to 5 microseconds width depending on the setting of R91. The pulse width can be increased by increasing the value of C30.

5.9 Output Gate

The stretch amplifier is followed by an output gate composed of two shunt elements (Q26, Q27) and their drive circuitry (Q50-Q53). Q26 and Q27 are normally saturated, shorting the gate of Q28 to ground. The pulse from the output pulse width control is routed to the base of Q50 which opens the output gate for a period equal to the width pulse. This in effect strobes the stretched pulse for a time equal to the width pulse.

5.10 Output Driver Amplifier

The Output Amplifier is a high input impedance, non-inverting, short circuit-proof amplifier (Q28-Q40, Q61, Q62) with positive and negative output current limited by Q39 and Q40 respectively. The front panel output has an impedance of less than one ohm and the impedance of the rear panel output is approximately 93 ohms. Potentiometer R52 permits the output dc level to be adjusted from -1.5 volts to +1.5 volts.

6. MAINTENANCE

6.1 Testing Performance of Pulse Stretcher

6.1.1 Introduction

The following paragraphs are intended as a aid in the installation and checkout of the 442. These instructions present information on waveforms at test points and output connectors.

6.1.2 Test Equipment

The following, or equivalent, test equipment is needed:

(1) ORTEC 419 Pulse Generator
(2) Tektronix Model 580 Series Oscilloscope
(3) 100-ohm BNC terminators
(4) Vacuum tube voltmeter
(5) ORTEC Pulse Shaping Amplifier
(6) Schematic and block diagrams for 442 Pulse Stretcher

6.1.3 Preliminary Procedures

(1) Visually check module for possible damage due to shipment.
(2) Connect ac power to Nuclear Standard Bin, ORTEC 401A/402A.
(3) Plug module into Bin and check for proper mechanical alignment.
(4) Switch ac power on and check the dc power supply voltages at the test points on the 401A Power Supply control panel.

6.1.4 Pulse Stretcher

(1) Feed the output of the 419 Pulse Generator into the input of the Amplifier.
(2) Set the Amplifier controls for a gain of approximately 200 with equal integration and differentiation time constants.
(3) Set the 442 Input switch to DC-Coupled and the Gate switch to NORMAL.
(4) Adjust the 419 Pulse Generator for a 100-millivolt pulse from the unipolar output of the Amplifier.
(5) Feed the 100-millivolt unipolar output of the Amplifier into the input of the 442. Load the 442 output with a 100-ohm terminator.
(6) Adjust the discriminator trimpot on the front panel until triggering of the stretcher circuit just occurs, as evidenced by an output pulse from the 442.
(7) Increase the input signal to the 442 (by adjusting the 419 Pulse Generator) to 500 millivolts.
(8) The output of the 442 should have a peak amplitude of 500 ±25 millivolts (see Pedestal Adjustment procedure in Section 6.2 if these limits are exceeded); the top of the pulse should exhibit a smooth slope of less than 0.5 millivolt/μsec.
(9) Increase the input signal to the 442 to 10 volts; the output should be essentially 10 volts.
(10) The time at which the output occurs should be adjustable from 0.3 to 3 microseconds after the peak of the input pulse. The duration of the top of the waveform should be adjustable over the range of 0.5 to 5 microseconds.
(11) Select the Gated position on the front panel switch and the Coinc position on the rear panel switch. The 442 output should disappear.
(12) Select the Anti-Coinc position on the rear panel switch and the 442 output should reappear. (A more complete check of the 442 Gate can be made if a logic pulse in time coincidence with the linear input pulse is available.)
(13) Increase the input to the 442 to the saturation level of the amplifier, approximately 12 volts; the output of the 442 should be greater than 10.5 volts.
(14) Connect the amplifier output to the 442 Gate Input and Monitor the Gate Period pulse with a scope. The Gate Period should be adjustable from 0.5 to 5 microseconds.

6.1.5 Pulse Pile-Up Test

A dual or variable high frequency pulser is needed to check the operation of the 442 pile-up circuit.

(1) Connect a dual or variable high frequency pulser to the 442 input.
(2) Monitor the 442 input and output simultaneously with a scope.
(3) Adjust the output delay and width controls to full clockwise position.
(4) Gradually decrease the time interval between the input pulses.
(5) The second pulse should be blocked by the 442 when the time interval between the peaks of two consecutive pulses becomes 8-15 microseconds.

6.2 Calibration Procedures

6.2.1 Linear Gate Pedestal Adjustment

The input and output gates are shunt type gates which clamp the signal line to ground. If the signal line is not at ground potential in the quiescent condition then a pedestal is introduced by the gating action. This can be avoided by adjusting the output of the Buffer Amplifier (TP1) to zero volts and then adjusting the output of the Stretch Amplifier (TP2) to zero volts. The following procedure should be followed when making this adjustment.

(1) Set the input gate switch to NORMAL.
(2) Set the INPUT switch to the mode desired. If the DC-COUPLED position is used, insure that the dc level of the Amplifier driving the 442 is set to zero volts.
(3) Monitor TP1 with a digital voltmeter and adjust R7, on the front of the printed circuit board, to obtain zero volts at TP1.
(4) When the INPUT switch is moved to either of the other two positions, the voltage at TP1 should remain at zero volts ±20 millivolts.
(5) Monitor TP2 with the voltmeter and adjust R18 to obtain zero volts at TP2.
(6) The 442 is now adjusted for a zero pedestal. These adjustments must be made regardless of whether or not the linear gating function of the 442 is being used.

CAUTION: If the INPUT switch is set to DC-COUPLED and the output dc level of the Amplifier driving the 442 is not set at zero volts, the 442 will appear to have a pedestal since the 442 gate circuit will be chopping a dc voltage.

6.2.2 Discriminator Adjustment

The 442 discriminator level should be set well above the system noise because each pulse that exceeds the discriminator level will be stretched, whether it be noise or a legitimate signal. If the discriminator level is set far below the system's noise, the 442 pile-up rejection circuit may completely block the input and prevent any outputs from occuring. Normally a discriminator level of 100 millivolts is adequate. A precise discriminator setting can be made by the following procedure.

(1) Apply a 0.5 microsecond shaped signal to the 442 input with amplitude equal to the desired discriminator level setting.
(2) Monitor the 442 input and output signals with a scope.
(3) Adjust the 442 discriminator control (front panel) until the number of output pulses is approximately equal to one-half the number of input pulses.
(4) The discriminator is now properly adjusted.

6.3 Suggestions for Troubleshooting

6.3.1 General

In situations where the 442 is suspected of malfunction, it is essential to verify such malfunction in terms of simple pulse generator impulses at the input. In consideration of this, the 442 must be disconnected from its position in any system, and routine diagnostic analysis performed with a test pulse generator and oscilloscope. It is imperative that testing not be performed with a source and detector until the amplifier-pulse stretcher system performs satisfactorily with the test pulse detector.

The testing instructions in Section 6.1 of this manual and the circuit descriptions in Section 5 should provide assistance in locating the region of trouble and repairing the malfunction. The two side plates can be completely removed from the module to enable oscilloscope and voltmeter observations with a minimal chance of accidentally short-circuiting portions of the etched board.

The 442 may be returned to ORTEC for repair service at nominal cost. The standardized procedure requires that each repaired instrument receive the same extensive quality control tests that a new instrument receives.

6.3.2 Possible Problem Solutions

Problem: Unable to get an output pulse.

Solution:
(a) If INPUT switch is in the DC-COUPLE position, switch to ACTIVE. If output appears, a dc level is probably being applied to the 442 input and locking up the pulse pile-up circuit. Adjust the output dc level of the amplifier feeding the 442 to zero volts.
(b) Adjust the DISC LEVEL full clockwise. If an output occurs, the discriminator was probably set below the system noise level, locking up the pile-up circuit.
(c) If operating in the GATED mode, switch to the NORMAL mode. If an output occurs the gating logic is probably not in time coincidence with the linear pulse.

6.4 Tabulated Test Point Voltages on Etched Board

The following voltages are intended to indicate the typical dc voltages measured on the etched circuit board. In some cases the circuit will perform satisfactorily even though, due to component variation, there may be some voltages that measure outside the given limits. Therefore, the voltages given should not be taken as absolute values, but rather are intended to serve as an aid in troubleshooting.

Table 6.1 Typical DC Voltages

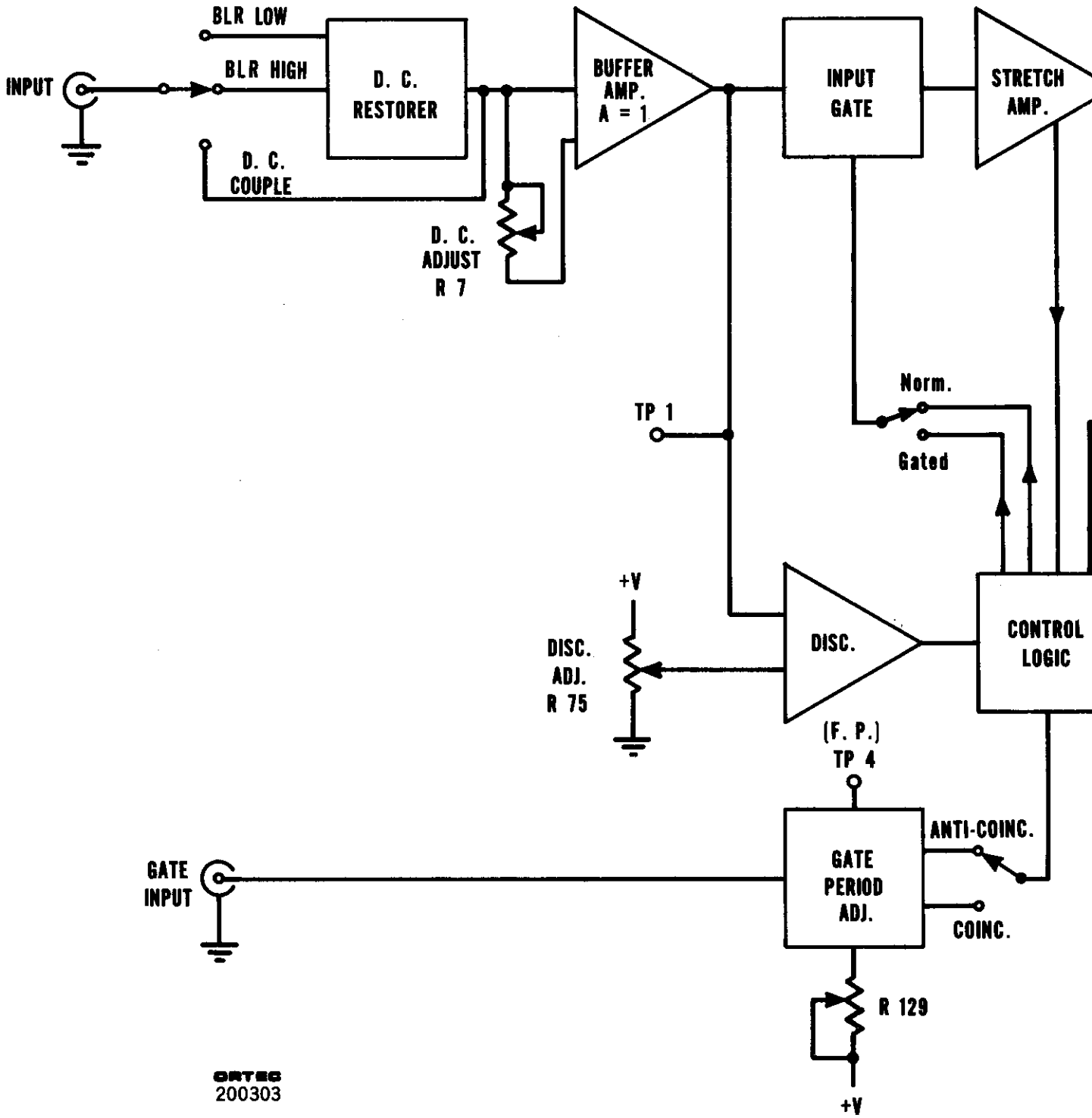
NOTE: All voltages measured with no input and input terminated in 100Ω. Input switch in DC-Coupled and all pots fully clockwise.

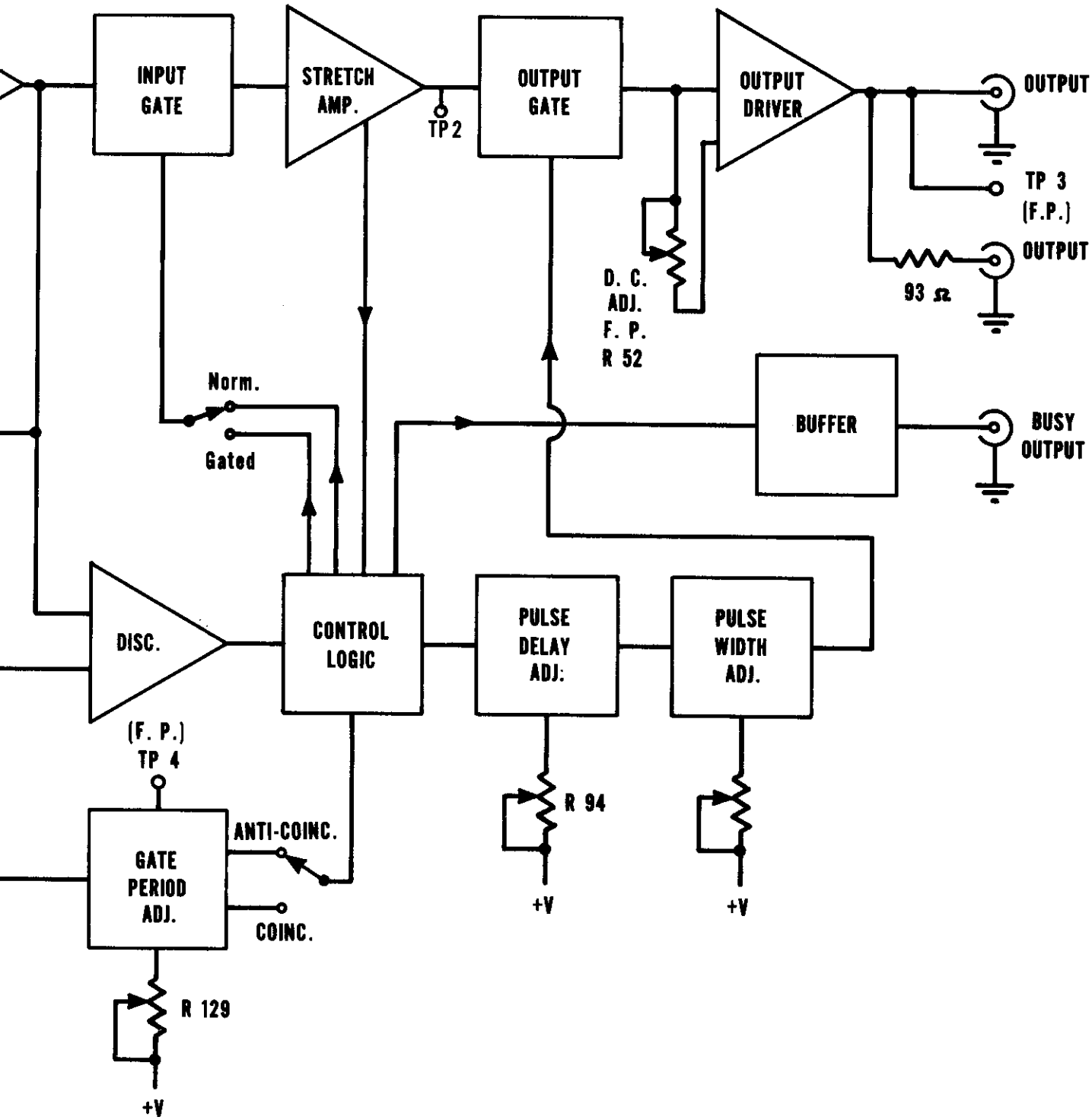
LOCATION	VOLTAGE	LOCATION	VOLTAGE
Q1B	+ 11.5	Q42C	- 11.9
Q1C	+ 0.012	Q42B	+ 1
Q2B	- 11.5	Q43B	+ 0.06
Q3B	0	Q44B	+ 0.7
Q4B	0	Q45B	+ 0.2
Q4C	+ 12.5	Q46B	+ 0.4
Q6B	+ 0.6	Q47B	+ 5.6
Q8G	0	Q48E	+ 0.78
Q8D	+ 18.9	Q49B	+ 5.6
Q9D	+ 20.2	Q50B	+ 0.15
Q11C	+ 0.5	Q50C	- 9
Q12B	- 2.6	Q51B	+ 1.1
Q12C	+ 1.6	Q51C	- 11
Q13D	+ 17.6	Q52C	- 2.7
Q16E	+ 18.2	Q53C	+ 2.1
Q17B	- 2.3	Q54E	+ 4.4
Q17C	+ 2.5	Q55E	+ 3.8
Q18E	0	Q56B	+ 5.6
Q20E	- 0.06	Q56C	+ 1
Q21C	+ 22.1	Q57B	+ 0.4
Q22C	0	Q58C	+ 11.2
Q23B	- 2.4	IC-1 Pin 2	0
Q25B	+ 3.8	IC-1 Pin 4	- 6
Q28G	0	IC-1 Pin 7	0
Q28D	+ 15.6	IC-1 Pin 8	+ 10.7
Q22D	+ 16.8	IC-2 Pin 3	+ 1.3
Q30B	- 2.5	IC-2 Pin 8	+ 0.05
Q30C	+ 0.4	IC-2 Pin 9	+ 1.3
Q32C	- 0.012	IC-2 Pin 13	+ 0.1
Q39B	+ 12.4	IC-5 Pin 8	+ 0.1
Q40B	- 12.4	IC-3 Pin 8	0

BIN/MODULE CONNECTOR PIN ASSIGNMENTS
FOR AEC STANDARD NUCLEAR INSTRUMENT MODULES
PER TID-20893

Pin	Function	Pin	Function
1	+3 volts	23	Reserved
2	- 3 volts	24	Reserved
3	Spare Bus	25	Reserved
4	Reserved Bus	26	Spare
5	Coaxial	27	Spare
6	Coaxial	*28	+24 volts
7	Coaxial	*29	- 24 volts
8	200 volts dc	30	Spare Bus
9	Spare	31	Carry No. 2
*10	+6 volts	32	Spare
*11	- 6 volts	*33	115 volts ac (Hot)
12	Reserved Bus	*34	Power Return Ground
13	Carry No. 1	35	Reset
14	Spare	36	Gate
15	Reserved	37	Spare
*16	+12 volts	38	Coaxial
*17	- 12 volts	39	Coaxial
18	Spare Bus	40	Coaxial
19	Reserved Bus	*41	115 volts ac (Neut.)
20	Spare	*42	High Quality Ground
21	Spare	G	Ground Guide Pin
22	Reserved		

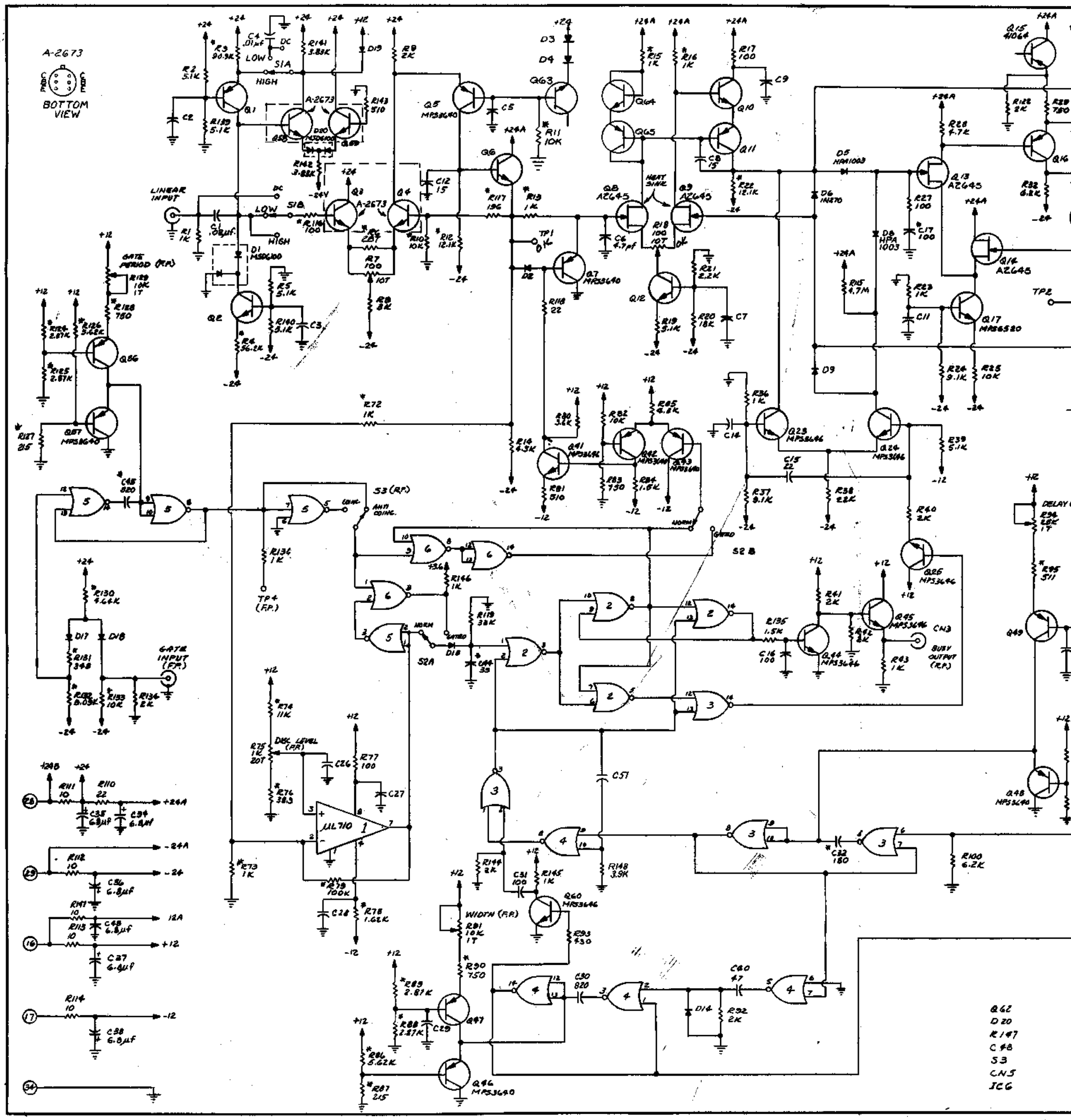
**These pins are installed and wired in parallel in the ORTEC 401A Modular System Bin.*


BLR LOW
BLR HIGH
INPUT
D. C.
RESTORER
D. C.
COUPLE
D. C.
ADJUST
R 7
BUFFER
AMP.
A = 1
INPUT
GATE
STRETCH
AMP.
Norm.
TP 1
Gated
+V
DISC.
ADJ.
R 75
DISC.
CONTROL
LOGIC
(F. P.)
TP 4
GATE
INPUT
GATE
PERIOD
ADJ.
ANTI-COINC.
COINC.
R 129
+V
ORTEC
200303

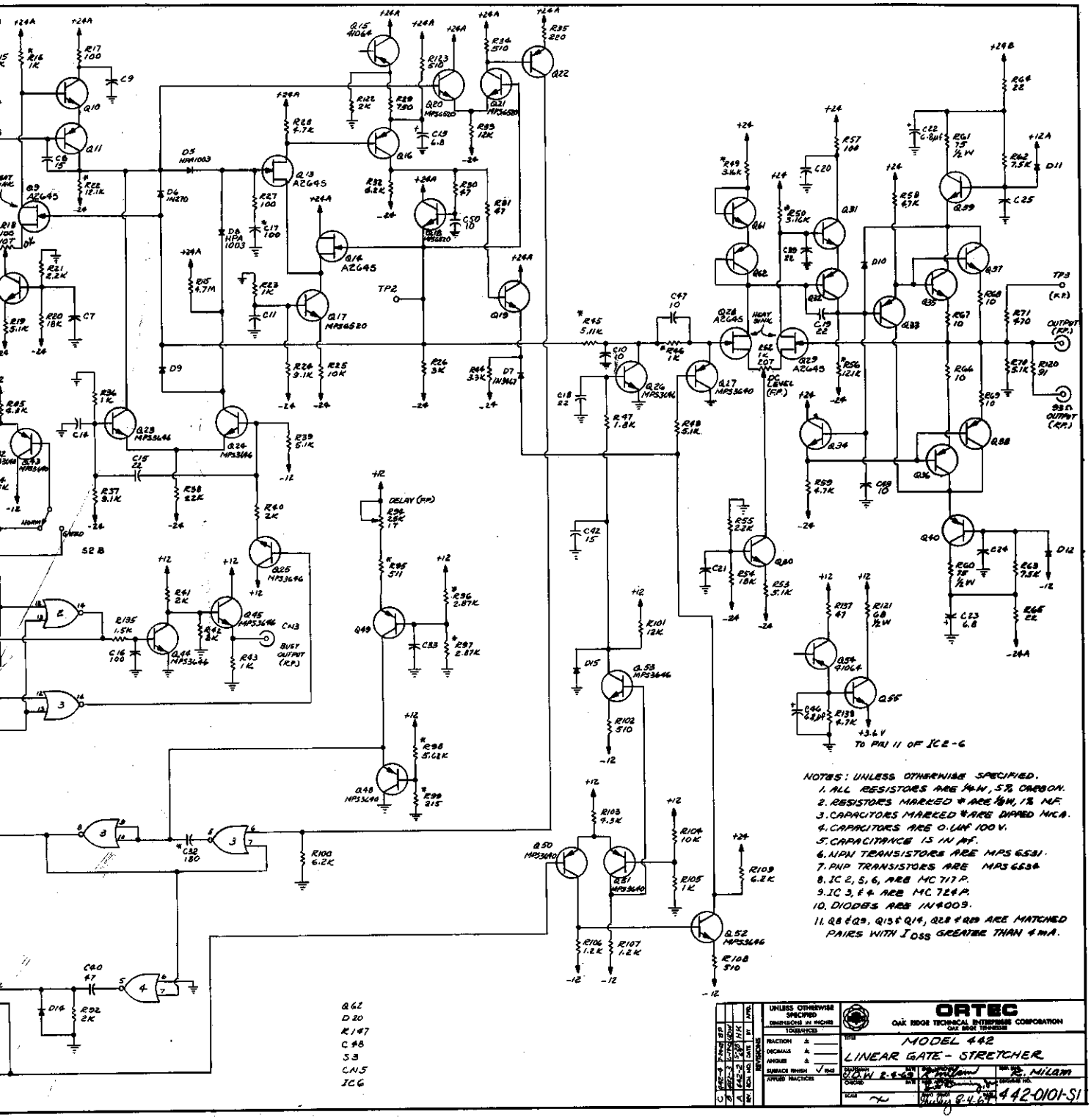


Model 442 Linear Gate-Stretcher Block Diagram

The transistor types installed in your instrument may differ from those shown in the schematic diagram. In such cases, necessary replacements can be made with either the type shown in the diagram or the type actually used in the instrument.



A-2673
BOTTOM VIEW
LINEAR INPUT
GATE PERIOD (F.P.)
GATE INPUT (F.P.)
DISC LEVEL (F.P.)
WIDTH (F.P.)
DELAY
BUSY OUTPUT (F.P.)
HEAT SINK
TP1
TP2
TP4 (F.P.)
S1A
S1B
S2A
S2B
S3 (F.P.)
ANTI COINC.
COINC.
NORM
GATED
HIGH
LOW
DC
CN3
Q62
D20
R147
C48
S3
CN5
IC6


NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTORS ARE ¼W, 5% CARBON.
2. RESISTORS MARKED * ARE ½W, 1% MF.
3. CAPACITORS MARKED * ARE DIPPED MICA.
4. CAPACITORS ARE 0.1MF 100 V.
5. CAPACITANCE IS IN MF.
6. NPN TRANSISTORS ARE MPS 6531.
7. PNP TRANSISTORS ARE MPS 6534.
8. IC 2, 5, 6, ARE MC 717 P.
9. IC 3, 4 ARE MC 724 P.
10. DIODES ARE IN4009.
11. Q8 & Q9, Q13 & Q14, Q28 & Q29 ARE MATCHED PAIRS WITH I_{DSS} GREATER THAN 4 mA.
+3.6 V TO PIN 11 OF IC2-6
Q62
D20
R147
C48
53
CN5
IC6
ORTEC
OAK RIDGE TECHNICAL ENTERPRISES CORPORATION
MODEL 442
LINEAR GATE - STRETCHER
442-0101-S1