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INSTRUCTION MANUAL 444 GATED BIASED AMPLIFIER

AN EG&G COMPANY

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A NEW STANDARD TWO-YEAR WARRANTY FOR ORTEC ELECTRONIC INSTRUMENTS

ORTEC warrants its nuclear instrument products to be free from defects in workmanship and materials, other than vacuum tubes and semiconductors, for a period of twenty-four months from date of shipment, provided that the equipment has been used in a proper manner and not subjected to abuse. Repairs or replacement, at ORTEC option, will be made without charge at the ORTEC factory. Shipping expense will be to the account of the customer except in cases of defects discovered upon initial operation. Warranties of vacuum tubes and semiconductors, as made by their manufacturers, will be extended to our customers only to the extent of the manufacturers' liability to ORTEC. Specially selected vacuum tubes or semiconductors cannot be warranted. ORTEC reserves the right to modify the design of its products without incurring responsibility for modification of previously manufactured units. Since installation conditions are beyond our control, ORTEC does not assume any risks or liabilities associated with methods of installation other than specified in the instructions, or installation results.

QUALITY CONTROL

Before being approved for shipment, each ORTEC instrument must pass a stringent set of quality control tests designed to expose any flaws in materials or workmanship. Permanent records of these tests are maintained for use in warranty repair and as a source of statistical information for design improvements.

REPAIR SERVICE

ORTEC instruments not in warranty may be returned to the factory for repairs or checkout at modest expense to the customer. Standard procedure requires that returned instruments pass the same quality control tests as those used for new production instruments. Please contact the factory for instructions before shipping equipment.

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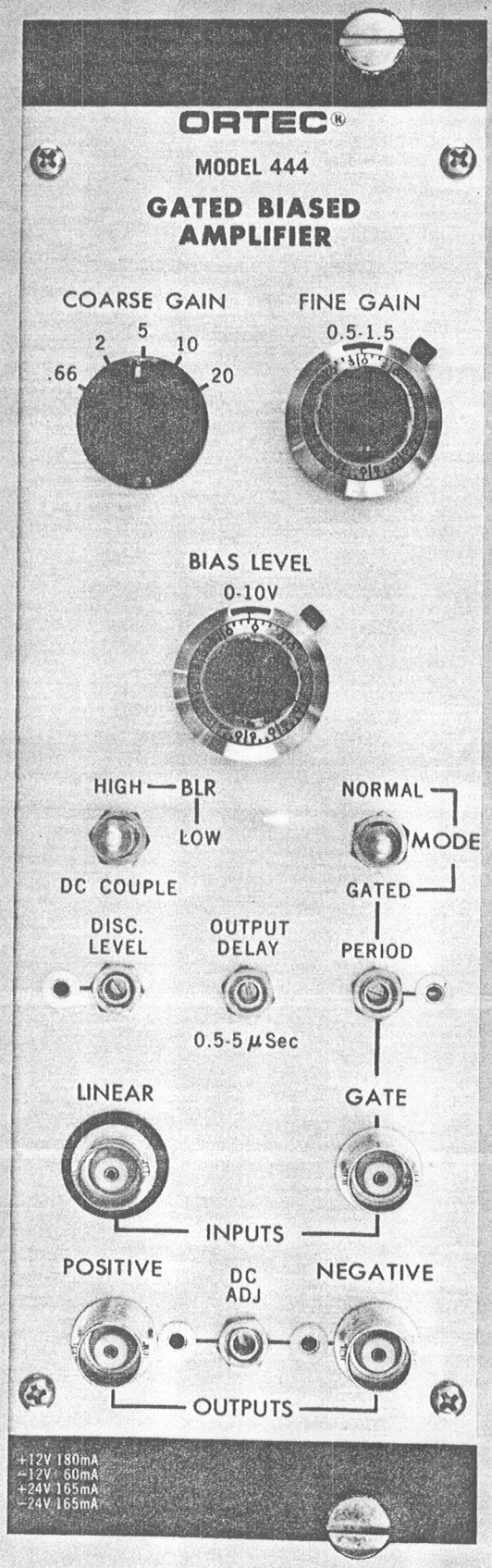
Shipments should be examined immediately upon receipt for evidence of external or concealed damage. The carrier making delivery should be notified immediately of any such damage, since the carrier is normally liable for damage in shipment. Packing materials, waybills, and other such documentation should be preserved in order to establish claims. After such notification to the carrier, please notify ORTEC of the circumstances so that we may assist in damage claims and in providing replacement equipment if necessary.


ORTEC®
MODEL 444
GATED BIASED AMPLIFIER
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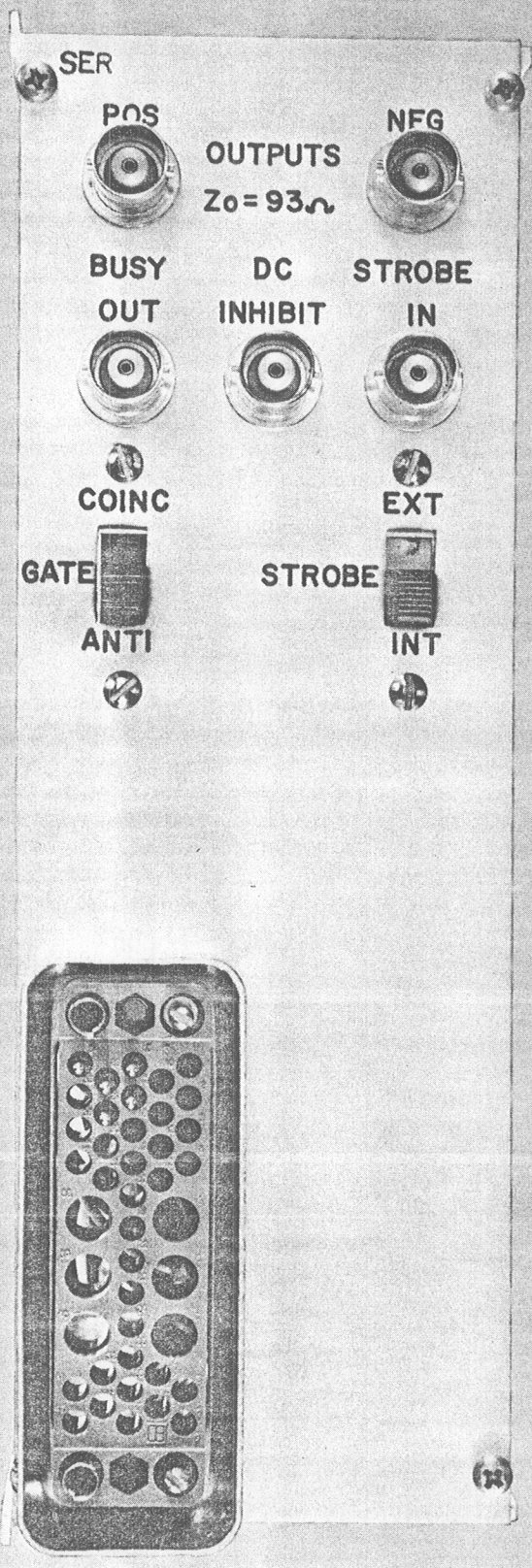
2
5
10
20
FINE GAIN
0.5-1.5
BIAS LEVEL
0-10V
HIGH
BLR
LOW
DC COUPLE
NORMAL
MODE
GATED
DISC. LEVEL
OUTPUT DELAY
0.5-5 μSec
PERIOD
LINEAR
GATE
INPUTS
POSITIVE
DC ADJ
NEGATIVE
OUTPUTS
+12V 180mA
−12V 60mA
+24V 165mA
−24V 165mA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ORTEC 444 GATED BIASED AMPLIFIER

1. DESCRIPTION

1.1 General

The ORTEC 444 Gated Biased Amplifier is an instrument module designed to permit an assured linear response of details in an expanded fraction of a total input spectrum. It includes a pulse stretcher, a biased amplifier, a linear gate, and a dc restorer. It features positive-on-positive pulse pileup rejection, and a fixed output pulse shape at an adjustable delay time or an external strobe time. Since amplitude is the only variable parameter of each linear output pulse, ambiguities are virtually eliminated from the system. Its correlated functions are interconnected within the module to provide optimum response and high performance. The 444 is compatible with all linear and logic instruments in the ORTEC 400 Series of modular instrumentation, designed in accordance with the preferred practices provisions of AEC Report TID-20893 (Rev. 2).

1.2 Basic Functions

The ORTEC 444 Gated Biased Amplifier expands a region of interest in a spectrum to allow maximum utilization of existing multichannel analyzers in high resolution and high counting rate spectroscopy applications.

The 444 features excellent temperature stability, integral linearity, response to high counting rates, and simplicity of operation. In addition, the linear gate section features total dc coupling with essentially zero pedestal and feedthrough and the internal automatic pulse pileup rejection reduces spectra distortion at high count rates.

The 444 is typically used between the main amplifier and a subsequent multichannel analyzer for spectrum expansion to permit better measurement of system resolution. Overall system resolution is improved by the utilization of baseline restoration, pulse pileup rejection, and linear gating facilities. Interfacing from the biased amplifier to the multichannel analyzer is accomplished with the internal strobed pulse stretcher which provides compatible standardized output pulses to the ADC input of any analyzer. The shape of these pulses is essentially independent of the original input pulse shape and bias level setting. This unit is especially useful in experiments utilizing Ge(Li) Detectors where the pulse shaping for best resolution typically results in an output pulse that does not satisfy the input requirements of the subsequent multichannel analyzer. Input pulse shapes from all available main amplifiers are directly compatible with the 444, e.g., active filter, RC, or delay line, either unipolar or bipolar waveshape.

The bias level features excellent temperature stability, $\leq \pm 20$ppM per degree C, and has a range of 0 to 10 volts controlled by a ten-turn bias control. Post gain above the bias level is continuously variable from 0.33 to 30 by a coarse gain switch and a ten-turn fine gain control providing excellent resetability.

The 444 output may be enabled or disabled by a positive gating pulse from 3 to 25 volts, e.g., the positive logic output from any NIM compatible module can be used for either coincidence or anticoincidence gating. In many applications it is desirable to process a linear signal according to selected coincidence and/or timing requirements, and thereby reduce the counting rate in subsequent linear analysis equipment, such as multichannel analyzers.

2. SPECIFICATIONS

2.1 Inputs

LINEAR	Positive unipolar or bipolar, 0.1 to 10V (100:1 dynamic range), ±12V max, T_r 100 nsec min, Z_{in} ≃1000Ω, dc-coupled or ac-coupled and dc-restored
GATE	⩾+3V (±25V max), width ⩾100 nsec, Z_{in} >2000Ω, dc-coupled
INHIBIT	⩾+3V (±25V max), Z_{in} ⩾1000Ω, dc-coupled
STROBE	⩾+3V (±25V max), Z_{in} ⩾1000Ω, dc-coupled

2.2 Outputs

LINEAR	Two linear outputs, POSITIVE and NEGATIVE, simultaneous through front panel (Z_o <1Ω) and rear panel (Z_o = 93Ω), range 0 to 10V, T_r ≃ 0.5μsec, flat topped pulse with width adjustable from 1 to 5μsec.
BUSY	Nominal +5V pulse, width equal to the time from the peak of the input signal to the end of the output pulse, as set by the pulse width control, or until the input discriminator has been reset, whichever is longer. Output impedance <10Ω, dc-coupled with T_r ⩽50 nsec

2.3 Performance

Integral Non-Linearity	<±0.05% (DC-Coupled or BLR-low), <±0.075% (BLR-high) for T_r >300 nsec; ⩽±0.1% for T_r >100 nsec and <300 nsec. Specified for dynamic range of 0.1 to 10V at pulse width ⩾400 nsec, and Gain <X15; 0.3 to 10V for Gain >X15
Temp. Stability	Specified in % of full scale input, 0 to 50°C
Bias Level	⩽±20 ppm (or 200μV)/°C
Post Gain	⩽±20 ppm/°C
Output dc Level	⩽±10 ppm (or ±100μV)/°C
Note:	Worst case is sum of above or ⩽±50 ppm/°C
Discriminator	0.005%/°C
Automatic Pile-up Rejection	After an input pulse has reached its peak, the input linear gate is closed and will not accept any subsequent input signals until both the output pulse has ended and the input discriminator is reset
Noise Contribution	⩽15μV, referred to input
Count Rate	The centroid of a pulser spectrum at 85% of full scale will shift less than 0.1% when modulated by 5 x 10^4 cps of random signals from a ^{137}Cs source-detector combination with photopeak at 70% of full scale, using ORTEC 450 or 451 amplifier with active filter time constant of 1μsec

Gate Feedthrough	Less than 1mV with gate closed
Gate Pedestal	Adjustable to 0V DC
Gain	Continuously variable from X0.33 to X30, product of COARSE and FINE Gain Settings
Stretcher Droop	The output pulse is essentially flat topped and will change less than 1mV/μsec

2.4 Controls

GAIN	COARSE switch (0.66, 2, 5, 10, 20) and FINE 10-turn precision potentiometer (0.5-1.5), for continuous Post Gain factor from X0.33 through X30, with resetability ≤0.01%
BIAS LEVEL	Continuously adjustable 0 to 10V, 10-turn precision potentiometer, with resetability ≤0.1%
INPUT COUPLING	3-position locking toggle switch, selects input coupling circuit
BLR HIGH	AC-coupled input with active baseline restorer, for input pulse duty cycle >20%
BLR LOW	AC-coupled input with passive baseline restorer, for input pulse duty cycle <20%
DC COUPLE	DC-coupled input, for input pulses from a dc-coupled source with no baseline offset
MODE	2-position locking toggle switch, selects inclusion or exclusion of gating circuit
NORMAL	Linear Gate circuit is bypassed
GATED	Linear Gate circuit is included, for either coincidence or anticoincidence mode as selected by rear panel switch
GATE PERIOD	Controls effective enable/disable period for gated mode. Range is 0.5 to 5μsec
DISC. LEVEL	~~Adjusts the delay period from peak of an input signal~~ must trigger discriminator to allow an output to be generated
OUTPUT DELAY	Adjusts the delay period from peak of an input signal to to rise of output pulse when using Internal Strobe. Range is 0.5 to 5μsec
DC ADJ.	22 turn control permits adjustment of output baseline to ±1V
GATE	Rear panel slide switch, selects either Coincidence or Anticoincidence Gated Mode operation
STROBE	Rear panel slide switch, selects either Internal or External Strobe to determine the output pulse time. Internal Strobe timing is delayed 0.5 to 5μsec after an input pulse peak by the Output Delay control. External Strobe timing is prompt

with the incidence of the external Strobe input pulse. Automatic reset at 25μsec maximum if not strobed, dependent on Output Delay adjustment

2.5 Connectors

LINEAR INPUT	BNC (UG-1094/A), front panel ($Z_{in} \approx 1000\Omega$)
GATE INPUT	BNC (UG-1094/U), front panel ($Z_{in} > 2000\Omega$)
POSITIVE OUTPUT	BNC (UG-1094/U), front panel ($Z_o < 1\Omega$), and rear panel ($Z_o = 93\Omega$)
NEGATIVE OUTPUT	BNC (UG-1094/U), front panel ($Z_o < 1\Omega$), and rear panel ($Z_o = 93\Omega$)
BUSY OUT	BNC (UG-1094/U), rear panel ($Z_o < 10\Omega$)
EXT INHIBIT	BNC (UG-1094/U), rear panel ($Z_{in} \geq 1000\Omega$)
STROBE IN	BNC (UG-1094/U), rear panel ($Z_{in} \geq 1000\Omega$)

2.6 Power and Mechanical

Power Required	+24V 165mA +12V 180mA -24V 165mA -12V 60mA
Weight (Shipping)	11 lbs (5 kg)
Weight (Net)	6.6 lbs (3 kg)
Dimensions	Standard double width module (2.70 by 8.714 inches) per TID-20893 (Rev.)

2.7 Related Equipment

The ORTEC 444 accepts signal input pulses from any shaping linear amplifier with an output compatible with its input requirements, such as ORTEC 410, 435A, 440A, 450, 451, or 485. The outputs are intended for measurement with a multichannel analyzer or a single channel analyzer, such as ORTEC 406A, 420A, or 455. They may also be used for increasing the sensitivity of any discriminator, as included in many other types of instruments.

3. INSTALLATION

3.1 General Installation Considerations

The ORTEC 444 is designed for installation in a standard Bin and Power Supply, such as the ORTEC 401A/402A. Since this bin is intended for rack mounting, it is necessary to ensure that any vacuum tube equipment operated in the same rack will have adequate cooling air circulation to prevent any localized heating of the 444 transistorized circuits. The temperature of equipment mounted in racks can easily exceed the recommended maximum unless precautions are observed. The ORTEC 444 should not be subjected to temperatures in excess of 120°F (50°C).

3.2 Connection to Power

The ORTEC 444 contains no internal power supply; therefore, it obtains its dc operating power from the standard Bin and Power Supply in which it is installed. Always turn power off for the Bin and Power Supply before inserting or removing any modules. The ORTEC 400 Series of modular instruments are designed such that it is not possible to overload the power supply with a full complement of modules in the bin. However, this may not be true when the bin contains modules other than those of ORTEC design; check the power supply for any overload conditions by testing the dc power levels after insertion of all modules.

The ORTEC 444 may be operated outside the 401A/402A Bin and Power Supply, using a power extension cable. Be sure that the cable used accounts properly for the grounding circuits recommended in AEC standards of TID-20893 (Rev.). Ground connections are included to ensure proper reference voltage feedback into the power supply, and these must be preserved by the remote cable. Be careful to avoid ground loops when the module is not physically installed in the bin during operation.

3.3 Linear Input Connection

Linear input pulses can be furnished from any ORTEC linear module of the 400 Series. These include amplifiers, delay circuits, gates, and other pulse handling equipment. The effective input range will be from the adjusted discriminator level (+0.1 to 1V) up through +10 volts.

When the linear input signals are furnished through a cable more than four feet long (approximately), the input should be terminated with the characteristic impedance of the cable. This can usually be avoided when shorter cables are used.

3.4 Linear Output Connections

The shaped linear output pulses can be furnished into any other ORTEC Series 400 linear module, or directly into the ADC input of a multichannel analyzer. It is important to preserve the pulse shape and amplitude of the output, thus the interconnecting cable should always be properly terminated. Either of two standard output impedances may be selected, according to the type and length of interconnecting cable and the input impedance of the instrument to which it is connected. The output is available through a front panel connector, with an output impedance of less than 1 ohm, or through a rear panel connector, with Z_0 = 93 ohms. For most applications proper resistive termination of the cable is attained by either of two methods indicated below.

One method is the series type termination, using the rear panel 93Ω Output connector and an appropriate length of 93 ohm coaxial cable to transfer the signal into the next module or instrument. The input impedance of the next equipment will probably be on the order of 1000 ohms or more. The total amplitude of each output pulse will be divided between the 93 ohm output impedance of the 444 and the input impedance of the next module, so a high input impedance is desirable when this series termination method is used.

An alternate method depends upon shunt termination at the remote end of the cable. For this, use the front panel 1Ω Output connector, and whatever type coaxial cable is desired. Then use a BNC Tee at the input to the next module, to accept both the cable and a BNC Terminator, selected to match the characteristic impedance of the cable when connected in parallel with the instrument's input impedance. For convenience, ORTEC stocks a limited quantity of BNC Tee connectors, in both 50 and 100 ohm BNC Terminators.

3.5 Gate Input

When Gate Input signals are required, they will be furnished through the BNC connector on the front panel of the 444. The function of an input pulse will be to enable or disable the 444 Linear Input gate through an adjusted Gate Period. The enable or disable function must be selected as either Coincidence or Anticoincidence by a rear panel slide switch.

Gate Input pulses are effective when they rise through +3 volts for a period of at least 100 nsec. A standard NIM Slow Logic positive pulse source may be used. The Gate Input circuit is protected to ±25 volts, so a wide variety of alternate sources can be used to initiate this control. When operating in the Coincidence mode, the Gate Period must be triggered before the peak of the linear input pulse and must be continued until after the peak has safely been sensed. When operating in the Anticoincidence mode, the Gate Period must be triggered prior to a discriminator response to the linear input and must be continued until the discriminator has been reset. Refer to Figure 3-1.

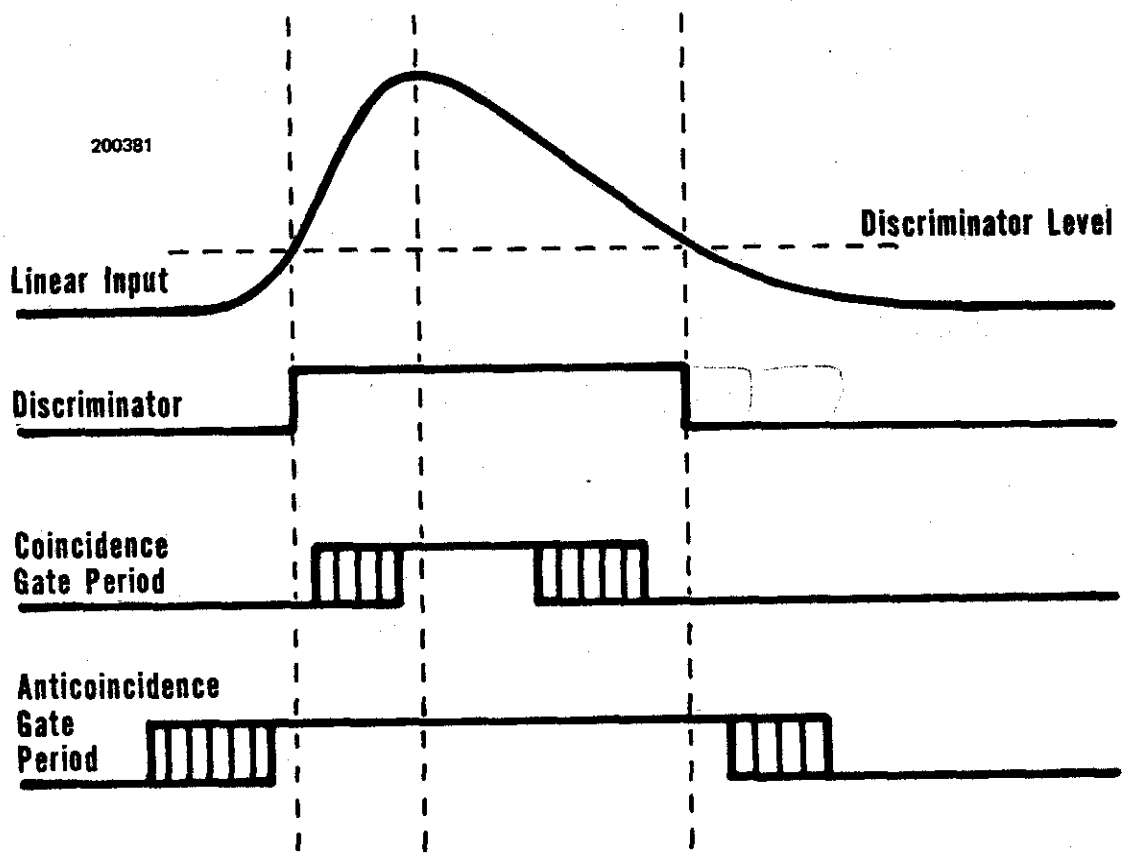


Figure 3-1. Timing Diagram for Coincidence and Anticoincidence Gating

No Gate Input is required if the front panel MODE switch is set at NORMAL. Likewise, if the front panel switch is set at GATED, and the rear panel mode selector is set at ANTI COINC, a Gate Input pulse is not required except when a linear input signal is to be rejected. When these switches are set for GATED and COINCIDENCE, respectively, a linear input pulse will be accepted only if it is accompanied by a time coincident Gate Input pulse.

3.6 Connection for Busy Output

The duration of each Busy Output signal is from the time an input pulse peak is detected until the resulting output pulse has been generated and the input discriminator has been reset if no INHIBIT signal is present. This identifies each period during which a new input pulse cannot be accepted in the

444. This output can be integrated externally to indicate the total dead time, or it can be furnished as a control to the pulse source and prevent generation of pulses when they cannot be accepted.

3.7 Use of Inhibit Input

The purpose of the Inhibit input is to permit blocking the 444 Linear Gate during periods beyond its own busy period to account for system dead time. When any linear signals processed by the 444 cannot be measured in subsequent instruments of a system such as a multichannel analyzer, and a signal indicating such a condition (e.g. ADC busy) is available, the INHIBIT function can be used in the 444 to reduce unnecessary loading for the remaining system components.

3.8 Use of External Strobe

During normal operation of the 444, each output pulse will be generated as a function of a linear input peak and a linear delay from 0.5 to 5μsec according to the adjustment of the front panel control. If external time synchronization of the output pulses is desired, the Strobe switch on the rear panel can be set at External and each output pulse will then occur when it is triggered by a signal through the Ext. Strobe connector on the rear panel.

Typical examples of conditions which could use the External Strobe to advantage include (1) delay required greater than the 5μsec maximum or (2) an output pulse time which is not dependent upon the peak detection time. In either case, consider the logic when setting up the Ext. Strobe pulse source. If the strobe occurs before the input peak, the output pulse will not have its characteristic flat top and may even fail to reach its full amplitude. If the strobe is delayed longer than 25μsec, an output will not be generated; this is because the stretcher will automatically reset without generating an output at a delay of 5 to 25μsec depending on the setting of the front panel output delay control.

4. OPERATION

4.1 Selection of Input Circuit Coupling

Any of three linear input circuits can be selected with the locking toggle switch on the front panel. They are DC Coupled, Active Baseline Restorer (HIGH), or Passive Baseline Restorer (LOW). The proper selection will depend on the type of output circuit in the module from which linear pulses are furnished into the 444.

The DC Couple switch position provides an optimum signal transfer circuit with 1000 ohms input impedance if the pulses are furnished from an amplifier with a dc-coupled output and a properly adjusted zero baseline. If the source does not include baseline restoration, use a capacitive coupling into the 444 and select either HIGH or LOW baseline restoration as the input circuit.

For any ac-coupled linear signal input, select one of the DC-Restore input circuits in the 444. In general, the Active (HIGH) circuit is intended for higher count rates, and Passive (LOW) for lower count rates. There is no precise dividing line, because of the various shaping time constants which may affect pulse shape. For 1μsec pulses, the division is approximately 15,000 counts per second. The most practical method for selecting between Active and Passive is an observation of the Output, using the circuit which provides the better results.

4.2 Discriminator Level Adjustment

The purpose for the adjustable discriminator level is to prevent response to all noise pulses. Therefore, it should be adjusted high enough in its +0.1 to +1 volt range to ensure discrimination against the maximum noise amplitude which may exist at the input to the 444 in the system. Since the logic in the 444 prevents response to a new input pulse until the discriminator is reset, but permits acceptance at that time unless an output pulse has not been generated, too high a setting of the discriminator level can permit a small amount of pileup to occur if the input pulse has a very long time constant decay. Although this interference is possible, it is unlikely in most applications. Still, an unnecessarily high adjustment is not recommended.

4.3 Output Delay Adjustment

When using the Internal Strobe, the delay adjustment permits normalizing timing in the system in which the 444 is operated. The delay interval is measured from the time the internal stretch amplifier senses a peak amplitude in the accepted linear input pulse, and is adjustable through the range of 0.5 to 5μsec. At the end of this delay period, the Width control opens the output gate and applies the peak amplitude pulse to the input of the biased amplifier portion of the 444.

4.4 Gain Adjustment

The Coarse and Fine Gain controls permit adjustment of the amplification factor used to expand the linear pulse amplitude which exceeds the bias cut. Since there is an overlap of the combined gain factors, the gain may be adjusted for any value between 0.33 and 30. The post amplification factors of less than 1, that is, gains of 0.33 to 1, are provided to allow an output full range compression from ±10 volts down to ±3.3 volts. This simplifies the interface with analog to digital converters with a linear range of less than 10 volts.

4.5 Bias Level Adjustment

After chosing the desired expansion factor, this is the post gain, the bias control should be adjusted such that the radiation peak of principal interest is conveniently located within the input voltage range of the ADC which is to encode the linear signal.

The front panel Bias Level control consist of a ten-turn dial and precision potentiometer which reads directly the adjusted bias level in volts. It may be set at any level within its 0.00 through 10.00 volts range and locked to prevent accidental readjustment. The selected level will be the bias cut point for all linear pulses as they pass through the biased amplifier, and the amplitude by which each linear pulse

exceeds the bias level will be expanded by a factor of 0.33 through 30, determined by the Gain controls, and furnished promptly to all four Output connectors. In a pulse height analysis system, the adjusted bias level will determine the equivalent energy level in the spectrum which will be measured as the minimum energy.

4.6 Output DC Adjustment

The quiescent level for the output, through both the front and rear panel connectors, should be at ground potential. Use the test point for the front panel Output connector which is to be used (either Negative or Positive), and adjust the screwdriver control as necessary to set the level at ground potential when there are no input signals to the 444.

4.7 Gated Operation

No Gate Input pulse is required if the front panel Mode switch is set at Normal. Likewise, if this switch is set at Gated and the rear panel slide switch is set at Anti-Coincidence, linear input pulses can be accepted when there is no signal through the Gate Input connector. Whenever a signal is furnished through the Gate Input and Anti-Coincidence is effective, all linear input signals are inhibited throughout the triggered Gate Period. To be effective, the Gate Period must be adjusted to overlap the duration of discriminator response to any pulse which is to be inhibited by the Gate Input signal. If the linear input triggers the discriminator before the Gate Input, or if the Gate Period permits termination of the Gate control prior to discriminator recovery, there will be an output but its amplitude will not usually reflect the input peak amplitude.

When the 444 is set for Gated Coincidence operation, a linear input signal will be accepted for stretching only if there is a time coincident Gate Input. The Gate Input signal must occur before the linear input peak, and the Gate Period must be long enough to continue the control beyond the internal detection of the peak amplitude. Refer to Figure 3-1.

4.8 Overall Logic

When an input pulse arrives at the Linear Input, it is applied directly to the discriminator. As its amplitude rises through the adjusted discriminator threshold, the discriminator may be fired or it may still be set because of not having recovered from a previous input pulse. The linear input pulse will not be accepted unless the discriminator had recovered and can be triggered by the new pulse; it will also be rejected if (1) an output pulse has not been completed for a previously accepted input; (2) the operating mode is Gated Coincidence and no Gate Input has been furnished; (3) the operating mode is Gated Anti-Coincidence, a Gate Input signal has been furnished, and the Gate Period is still effective; or (4) there is an Inhibit signal present.

When the discriminator is triggered prior to a Coincidence Gate Input, the linear input signal is applied to the stretch circuit at the leading edge of the Gate Input. This is a critical time, and an output signal will result; its amplitude is equal to (1) the peak input amplitude, or (2) the amplitude at the release (critical) time if this occurs after the peak. Thus, it is important that the gate be released during the rise time of a linear input pulse. By similar logic, the end of an effective Gate Period should never occur before the peak amplitude has been sensed, or there will be a false amplitude output.

4.9 Internal Adjustment

The output pulse width is fixed at 2.5μsec fwhm when the 444 leaves the factory. These pulse widths can be readjusted, if required with an internal control.

5. CIRCUIT DESCRIPTION

Refer to the Block Diagram and Schematics at the end of this manual.

5.1 Baseline Restorer

The input signals to the 444 will pass either through or around the Baseline Restorer circuit, as selected by front panel switch S1. When the switch is set at DC Couple, the circuit is bypassed. If baseline restoration is desired, the switch can be set at either Low or High, according to the relative count rate of the input signals. When S1 is set at Low, the baseline is restored by a constant current of 100μA, providing a restoration rate of approximately 10mV/μsec. When S1 is set at High, the current is 3mA, for a restoration rate of about 300mV/μsec. These voltage restoration rates can be varied by changing the value of C2. The baseline restoration circuit includes Q1, Q2, Q3, Q4, and D1.

5.2 Buffer Amplifier

The restoration circuit is followed by a non-inverting buffer amplifier, including Q5 through Q8 and Q53, with a gain of approximately one. The gain of this stage is given by the ratio $\frac{R21 + R15}{R15}$. The 444 is dc-coupled from this stage to the output, so an adjustment is provided in each stage to set its dc level at zero. Potentiometer R13 should be adjusted for a zero volt level at the output of the buffer amplifier, measured at TP1. The Buffer Amplifier drives the Input Gate and the Discriminator.

5.3 Input Gate

Transistor Q9 is the shunt type Input Gate. When the front panel Mode switch is set at Normal, Q9 remains off until the peak of the input pulse, when it saturates and clamps the gate of Q10 to ground. Q9 continues in saturation until the input signal falls below the Discriminator level and the 444 Output pulse has been completed, and the Input Gate is closed through this time. This prevents the 444 from accepting a second pulse until it has completed processing the first pulse, and eliminates positive on positive pile-up. Details are shown in Figures 5-1 and 5-2.

When the Mode switch is set at its Gated position, the functional mode must be selected by the rear panel Coinc/Anti switch, and the Input Gate provides the added function together with its pile-up rejection function. When the Coincidence mode is selected, Q9 will be normally turned on and saturated, clamping the gate of Q10 to ground. In order to open the gate, a logic pulse must be furnished through the Gate input BNC to turn Q9 off. The input logic pulse is reshaped for an adjusted Gate Period by IC5, Q31, and Q32, and applied to the input gate drive circuit, Q24, Q25, and Q27, to open gate Q9 for the duration of the Gate Period. The Gate Period must overlap the peak of the linear input signal if the input signal is to be accepted.

When the Anti-Coincidence mode is selected, the control of Q9 is the inverse of the above discussion. Q9 will normally be off, the gate will be open except when it is closed by a Gate input logic pulse, and linear input signals will normally be accepted. In order to obtain proper Anti-Coincidence control, the Gate Period which is triggered by the Gate input pulse must totally overlap the time during which the linear input pulse exceeds the discrimination level. If the range of the Gate Period needs to be increased, change the value of C34 to a larger capacity for the longer control period.

5.4 Busy Output

The Busy Output is a monitor of the internally created dead time in the 444. This signal begins at the peak of the linear input and continues to the completion of the 444 output pulse, ending then only if all of the conditions which will enable the Input Gate have been fulfilled. Refer to the timing diagrams of Figures 5-1 and 5-2, and to Section 4.8.

5.5 Discriminator

The Discriminator permits the 444 to reject all input pulses which fail to rise above the selected discrimination level, such as noise pulses. The discriminator level can be adjusted from +0.1 through +1V with front panel control R125. When the discriminator level is exceeded by a linear input signal and the Input Gate is open, a signal is sent to the Stretch Amplifier to stretch the input pulse.

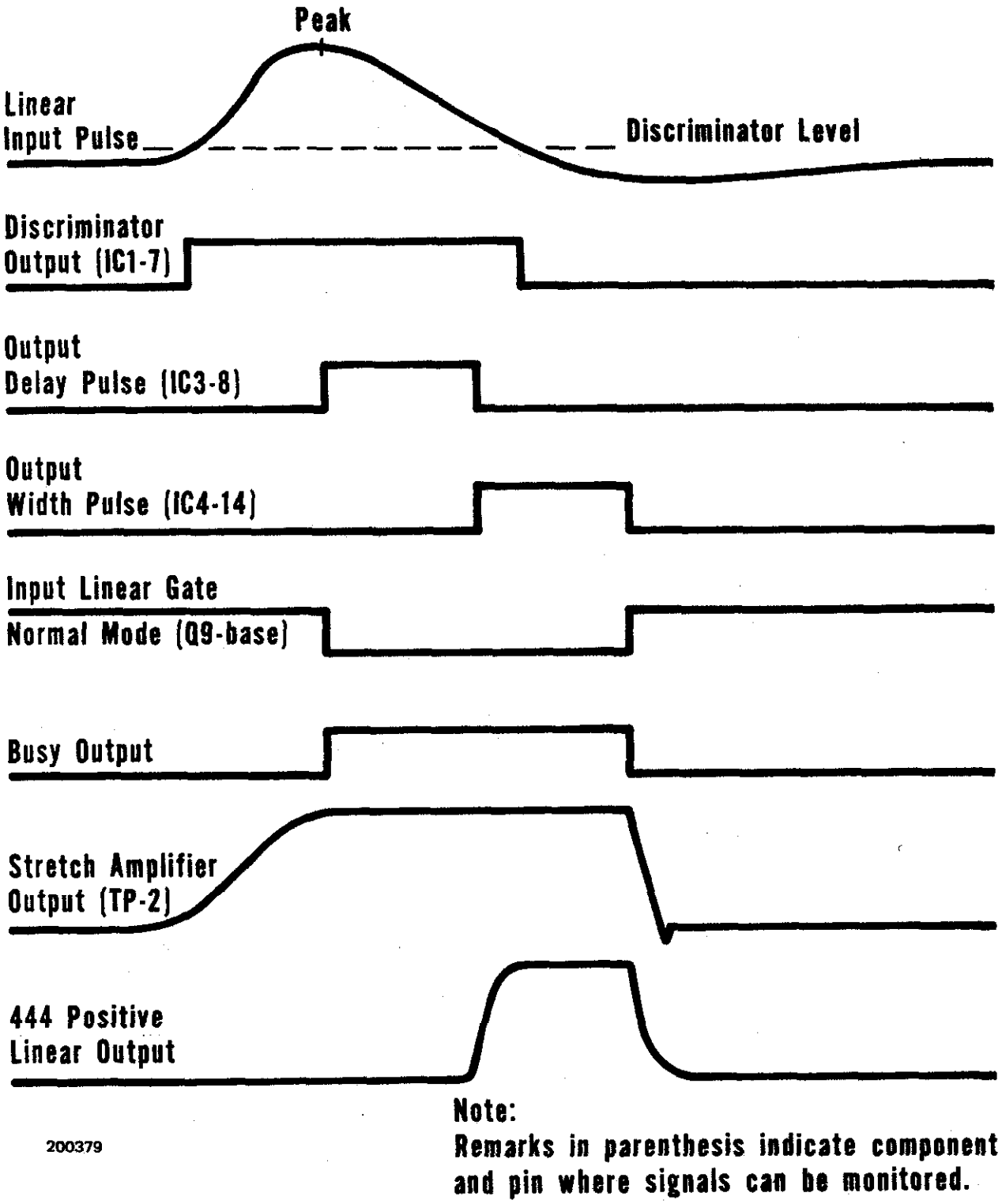


Figure 5-1. 444 Timing Diagram for Response to a Single Input

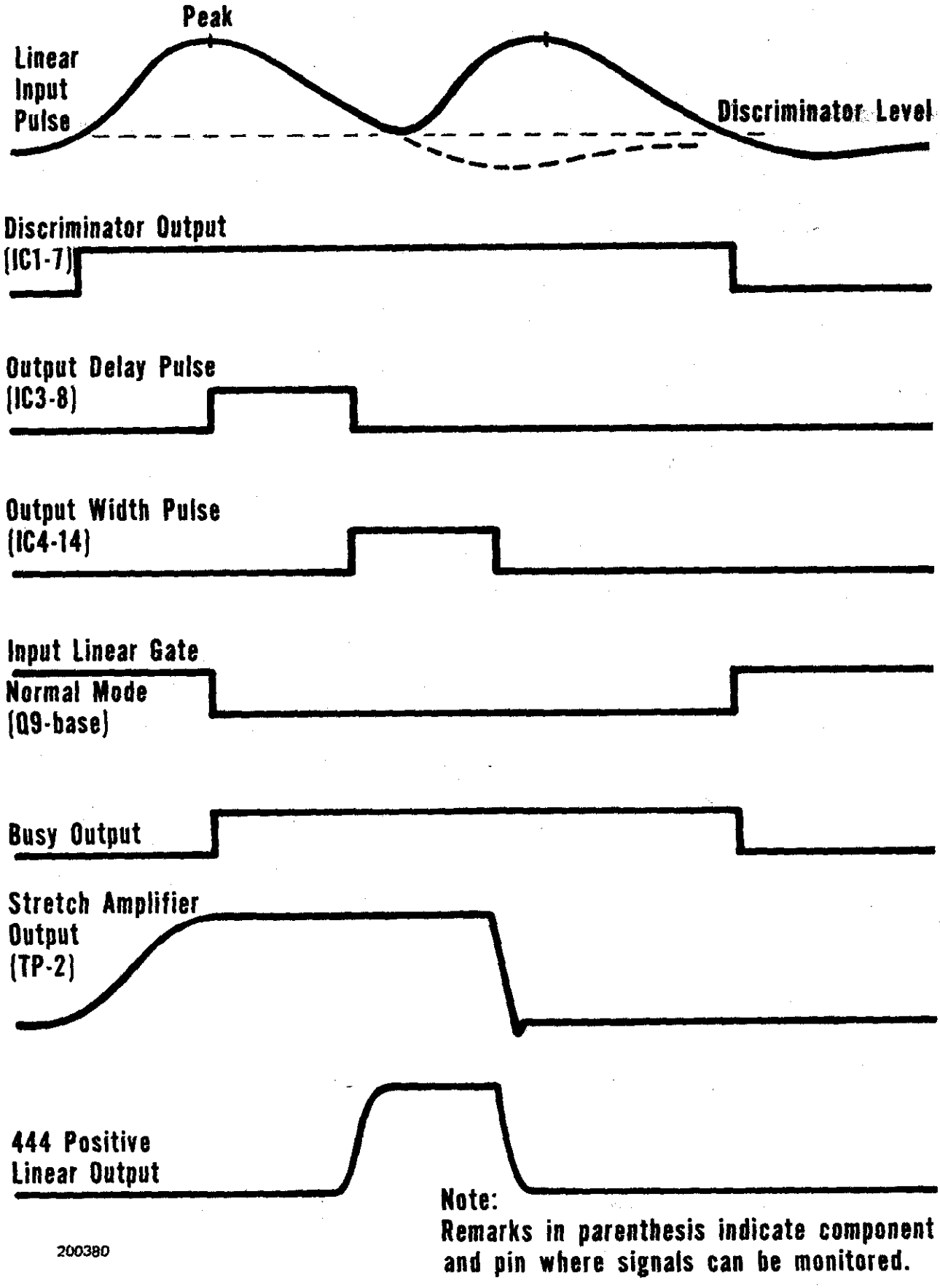


Figure 5-2. 444 Timing Diagram for Pile-Up Input Pulses

5.6 Stretch Amplifier

The Stretch Amplifier is a non-inverting amplifier composed of Q10 through Q23, Q51, and Q52. The amplifier loop is normally closed, with current through Q29 and D11. When the Discriminator sends its signal to stretch the input pulse, the current through Q29 is switched to Q28. Then stretch capacitor C10 is charged through D11 to the peak voltage of the input signal. After the peak has occurred, D11 is back biased and the peak voltage is stored on C10 until Q29 is switched on again at the end of the output pulse. A high input impedance, non-inverting amplifier, Q18 to Q20 and Q21 to Q23, acts as a buffer and driver for the voltage on capacitor C10. This amplifier is included inside the stretch amplifier loop to provide better linearity and stability. Q15-Q17 monitors the voltage across D11 and produces a peak detect signal when D11 becomes back biased. The peak detect signal is routed to the control logic to initiate the delay signal, which will initiate the output width signal. Potentiometer R42 is provided to adjust the voltage at TP2 to zero when the input voltage to Q10 is zero.

5.7 Output Pulse Delay

The Delay circuit consists of Q41 and Q42 and two gates of IC3 which form a one shot multivibrator. The leading edge of the peak detect signal triggers this stage at IC3 Pin 6, and initiates the delay. The width of the Delay pulse can be varied from 500 nsec to 5μsec with front panel control R117; this range can be increased by using a larger value for C30.

The leading edge of the Delay pulse, at IC4 Pin 6, sets the flip-flop, IC3 and IC4, which in turn controls the Input Gate through IC2 and IC8. The circuit of IC3 and IC4 is actually a one shot multivibrator, with the additional feature that it can be reset at IC3 Pin 1, and thus is normally operated as a flip-flop.

5.8 Output Pulse Width

The Delay pulse is routed to the Output Pulse Width control circuit, including Q47 and gates in IG4 and IC7. The trailing edge of the Delay pulse energizes the Width circuit at IC4 Pin 2, to generate an output pulse width of 0.5 to 5μsec, depending on the setting of R61. This internal adjustment is preset at the factory for an output pulse width of 2.5μsec. The range of adjustable widths can be increased by using a larger value for capacitor C25. This output pulse will drive the Output Linear Gate, which includes Q26, and Q35 to Q38.

5.9 External Strobe

The External Strobe circuit is enabled when the rear panel switch S3 is set at External. C32 increases the duration of the Delay pulse for this control mode. The Output Pulse Width control circuit can be triggered only by the Strobe Input, IC4 Pin 9. If an External Strobe signal is supplied while the output Delay circuit is set, an output will be generated promptly, controlled by the Width control circuit. The Width pulse is differentiated, and its trailing edge resets the IC3/IC4 flip-flop at IC3 Pin 1 through Q48. Simultaneously, the Delay one-shot is reset with the current switch, Q44-Q46, to recharge C30 and C32 rapidly.

In the event that no Strobe pulse is furnished while the Delay flip-flop is set, the trailing edge of the Delay pulse, differentiated at Q47, resets the IC3/IC4 flip-flop and enables the Linear Gate.

The duration of the Delay before automatic reset of the logic without generating an Output (because the Width circuit is not triggered) is controlled by the setting of R117. The range is 5 to 25μsec, since C32 is included in the circuit.

5.10 Output Linear Gate

The Stretch Amplifier is followed by an Output Gate, which in turn connects to the Bias Amplifier. The Gate circuit, Q35-Q38, will normally drain current from the Bias stage through R1 (on 444-0301-S1) to keep diode D1 in a back biased condition. This effectively disconnects the Stretch Amplifier output from the Post Amplification stages and the 444 Linear Outputs. The Output Pulse Width circuit will turn Q38 off, to strobe the Stretch Amplifier output into the Bias stage for a time equal to the Width pulse duration.

5.11 Bias Amplifier Stage

Operational amplifier A3 is the Bias Amplifier Stage. It is a summing junction for the current, i_s, from the Stretcher output and the current, i_b, from the bias level current source, as shown in Figure 5-3. The amplifier feedback loop is divided into two parallel branches by diodes D1 and D2, and the non-linear characteristics of the diodes allows only one feedback path to be active at any one time. When the net input current, $i_s - i_b$, is positive, D2 conducts and current flows through R5 to close the feedback loop with a total gain of unity for the stage since $\frac{R5}{R75 + R1} = 1$.* When the net input current is negative, D1 conducts and current flows through R4; in this case, the gain of the stage is $\frac{R4 + R\,(D1)}{R75 + R1} \simeq \frac{1}{50}$. The signal current, i_s is given by $\frac{e_s}{R75 + R1}$; the bias current, i_b, is determined by the setting of the Bias Level control, R47. By this method, a signal which exceeds the bias level will be furnished through to the Post Amplifier, while all signal levels less than the bias will be effectively disconnected from the Post Amplifier.

The dc balance for the A3 amplifier is obtained by monitoring TP3 while adjusting R3 on the 444-0301 printed circuit. The bias current supply is encapsulated to obtain better temperature stability, and is factory adjusted for a 10 volt bias level range using R46.

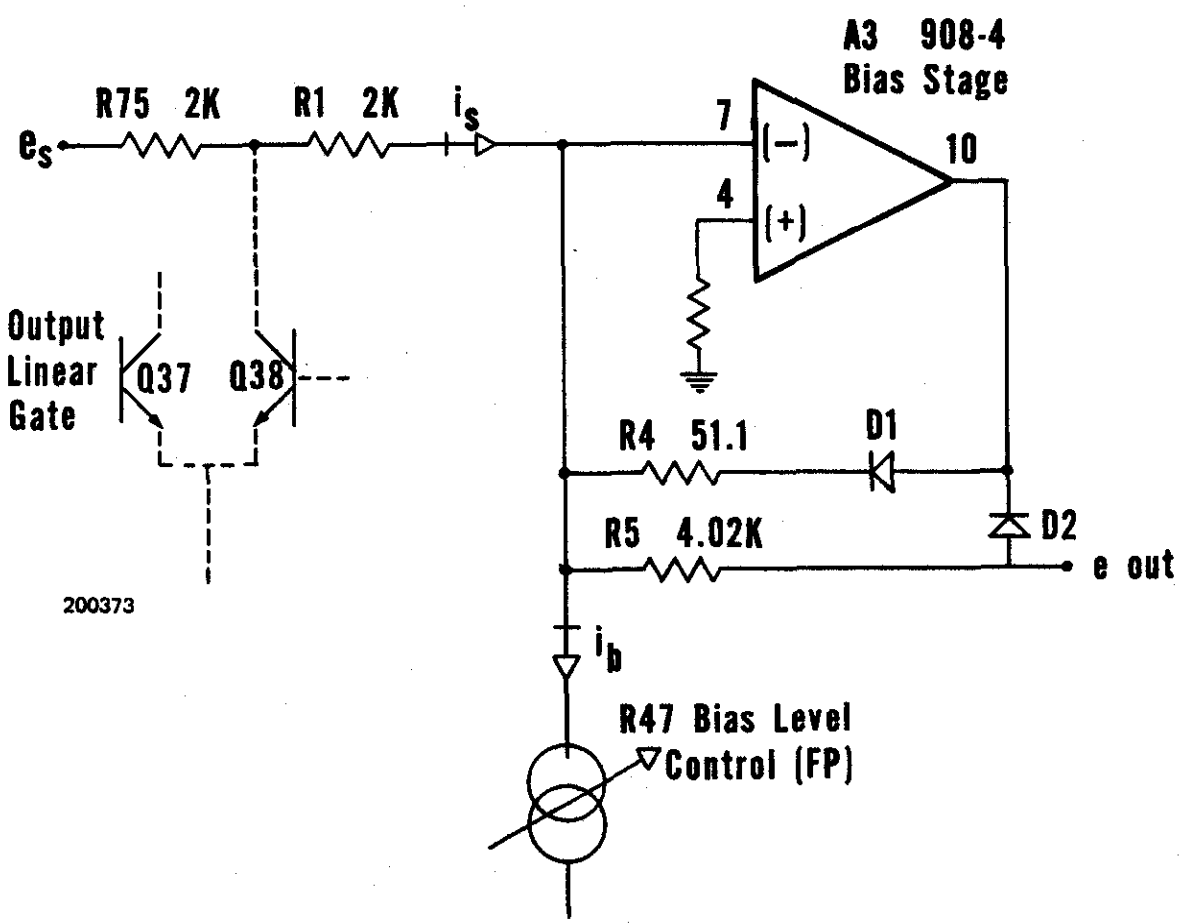


Figure 5-3. Bias Amplifier Stage

*R75 is located on Drawing 444-0201-S1

5.12 Post Amplification and Output Stages

The Bias Amplifier stage is followed by a 3:1 passive attenuator, R6 through R8, which make up the Fine Gain control. R10 is adjusted to compensate for the negative Output Amplifier input current when no signal is present.

Amplifier A1 is feedback in a non-inverting configuration, with a closed loop gain given by:

$$\left(\frac{R7x + R6}{R8 + R7 + R6}\right) \cdot \left(\frac{R11 + Rn}{R11}\right)$$

The first factor is Fine Gain, ranging from 0.5 to 1.5. The second factor is Coarse Gain, with values of 0.66, 2, 5, 10, and 20. R7x is defined as the resistance between the wiper arm of R7 and R6. Rn takes the value of R18 through R24, depending on the Coarse Gain switch setting.

The Negative Output of the 444 is the output of amplifier A1. The Positive Output is obtained by simply inverting the Negative Output with Amplifier A2, where the closed loop gain is given by $\frac{R37}{R38}$. In both Amplifiers, the dc baseline is balanced with the DC Adjust control, R48, located on the front panel. Transistors Q1 through Q4 provide current limitation for the linear outputs, to prevent damage by a short across one of the output connectors. If the output duty cycle is such that it exceeds the power dissipation rating of the operational amplifier, these same transistors will current-limit the supplies to avoid any damage to the instrument.

6. MAINTENANCE

6.1 Testing Performance of 444 Gated Biased Amplifier

6.1.1 Introduction

The following paragraphs are intended as an aid in the installation and checkout of the ORTEC 444. These instructions present information on waveforms at test points and output connectors.

6.1.2 Test Equipment

The following test equipment, or equivalent, is needed:

(1) ORTEC 419 Pulse Generator
(2) Tektronix 580 Series Oscilloscope
(3) 100 ohm BNC terminators
(4) Vacuum tube voltmeter
(5) ORTEC Pulse Shaping Amplifier
(6) Schematic and Block Diagrams for 444 Gated Biased Amplifier

6.1.3 Preliminary Procedures

(1) Visually check the module for possible damage during shipment.
(2) Plug module into bin and check for proper mechanical alignment.
(3) Connect ac power to the Nuclear Standard Bin and Power Supply, ORTEC 401A/402A.
(4) Switch ac power on and check the dc power supply voltages at the test points on the 401A control panel.

6.1.4 Pulse Stretcher Circuit

(1) Feed the output from the ORTEC 419 Pulse Generator into the input of the shaping Amplifier.
(2) Set the Amplifier controls for a gain of approximately 200, using appropriate integration and differentiation time constants.
(3) Set the 444 controls as follows:

Front panel

Coarse Gain	X2
Fine Gain	X0.5
Bias Level	000
Input Switch	DC Couple
Mode Switch	Normal

Rear panel

Anti/Coinc Switch	Anti
Strobe Switch	Internal

(4) Adjust the 444 Disc. Level control counterclockwise, for a +100mV setting.
(5) Verify the dc output of the shaping amplifier to be 0V, and adjust the 419 Pulse Generator for a +100mV output pulse from the Unipolar output of the amplifier.
(6) Connect the positive unipolar output of the amplifier to the input of the 444. Load the 444 Positive front panel output with 100 ohms.
(7) Verify the dc output of the 444 to be 0V, and monitor the 444 Positive Output; observe an essentially square wave 100mV pulse, readjust the Pulse Generator amplitude if necessary.
(8) Adjust the 419 Pulse Generator for a 500mV input to the 444.
(9) Observe the 444 Positive Output; it should be a flat top peak of 500 ±25mV, and the top should have a smooth slope of less than 1mV/μsec. See Section 6.2 if the peak amplitude is not within tolerance.
(10) Increase the input signal to the 444 to 10 volts; the output should be essentially 10 volts.

(11) The time at which the output occurs should be adjustable from 0.5 to 5μsec after the peak of the input pulse, using the front panel Output Delay. The duration of the output should be about 2.5μsec, as shipped from the factory, and should be adjustable at fwhm from 0.5 to 5 μsec, using the internally mounted Width control (refer to Section 5.8).
(12) Select the Gated position for the front panel Mode switch, and Coinc. with the rear panel Anti/Coinc switch. The 444 output should disappear.
(13) Select the Anti. position with the rear panel switch, and the 444 output should reappear. A more complete check of the 444 Linear Gate can be made if a logic pulse is available which is in time coincidence with the linear input.
(14) Increase the 444 input amplitude to the saturation level of the amplifier, approximately 11 volts; the 444 output should be greater than 10.5 volts.
(15) Connect the amplifier output to the 444 Gate Input and monitor the Gate Period pulse with the oscilloscope. The Gate Period should be adjustable from 0.5 to 5μsec.

6.1.5 Pulse Pileup Test

A dual, with variable delay high frequency pulser,is needed to check the operation of the 444 pileup circuit.

(1) Connect the dual pulser to the 444 input.
(2) Monitor the 444 input and Positive Output simultaneously with the oscilloscope.
(3) Adjust the 444 Output Delay control fully clockwise.
(4) Decrease the time interval between input pulses gradually.
(5) The second pulse should be blocked by the 444 when the time interval between the peaks of two consecutive input pulses becomes 8 to 15μsec.

6.1.6 Bias Amplifier Circuit

(1) Adjust the 419 Pulse Generator amplitude for a +10V pulse from the Unipolar Output of the shaping Amplifier. Set the 444 controls as in (3) of paragraph 6.1.4.
(2) Monitor the 444 Positive Output, and observe an essentially square wave +10V pulse.
(3) Increase the Bias Level control setting to 900. Observe the 444 output amplitude as it decreases to 1 volt.
(4) Set the Bias Level at 1000 divisions, and the output pulse amplitude should be approximately zero ±100mV.

6.2 Calibration Procedures

6.2.1 Linear Gate Pedestal Adjustment

The 444 input has a shunt type gate, which clamps the signal line to ground. If the signal line is not at ground potential in the quiescent condition, a pedestal is introduced by the gating action. This can be avoided by adjusting the output of the Buffer Amplifier (TP1) to zero volts, and then adjusting the output of the Stretch Amplifier (TP2) to zero volts. Use the following procedure to make these adjustments:

(1) Set the Mode switch at Normal.
(2) Set the Input switch for the circuit desired; if the DC Couple position is used, insure that the dc level is at zero from the amplifier which drives the 444.
(3) Monitor TP1 with a digital voltmeter, and adjust R13 on board 444-0201 for zero volts.
(4) Switch the Input coupling to its alternate positions; the voltage at TP1 should remain at zero volts ±20mV.
(5) Monitor TP2 with the voltmeter and adjust R42 for zero volts.
(6) The 444 is now adjusted for a zero pedestal. These adjustments are required whether the linear gating function of the 444 is to be used or not.

NOTE: If the Input coupling is set for DC Couple and the amplifier output is not set at zero volts, the 444 will appear to have a pedestal since the 444 gate circuit will be chopping a dc voltage.

6.2.2 Discriminator Adjustment

The 444 discriminator level should be set well above the system noise because each pulse that exceeds the discriminator level will be stretched, whether it is noise or a legitimate signal. If the discriminator level is set far below the system noise, the 444 pileup rejection circuit may completely block the input and prevent any outputs from occurring. Normally, a discriminator level of 100mV is adequate. In the presence of noise, a precise discriminator level setting can be made as follows:

(1) Apply a 0.5μsec shaped signal to the 444 input, with an amplitude equal to the desired discriminator level setting.
(2) Monitor the 444 input and output signals with an oscilloscope.
(3) Adjust the 444 Disc. Level control until the output pulse rate is approximately one-half of the input pulse rate.

The discriminator is now properly adjusted.

6.2.3 Bias Amplifier Stage DC Adjustment

The dc output level of the bias amplifier should be adjusted to zero volts. To ensure proper adjustment, proceed as follows:

(1) Set the Bias Level control at 000, the Fine Gain at 500 (minimum), and disconnect any linear input from the 444.
(2) With a vacuum tube type voltmeter, monitor TP3 on the 444-0301 printed circuit board.
(3) Adjust R2 on the same printed circuit to obtain zero ±1mV at TP3.

6.2.4 Bias Level Range Adjustment

The upper end of the Bias Level range is factory adjusted to be +10 volts. If a readjustment or change is necessary, proceed as follows:

(1) Repeat steps 1, 2, and 3 of paragraph 6.1.4.
(2) Feed the Positive Unipolar output from the main amplifier into the 444 Linear Input. Monitor TP3 with the oscilloscope, and adjust the Pulse Generator output amplitude to obtain -10 volts at TP3.
(3) Set the Bias Level control at 500, and lock.
(4) Monitor TP3, and adjust R46 for one half of the desired full range amplitude. For example, adjust for 5 volts to obtain a 10 volt full range. Note that the Bias Level control dial is calibrated directly in volts only if the full range of the bias is retained at the factory preset 10 volt level.

6.3 Suggestions for Troubleshooting

6.3.1 General

In situations where the 444 is suspected of malfunction, it is essential to verify such malfunction in terms of simple pulse generator impulses at the input and output. The 444 must be disconnected from its position in any system while routine diagnostic analysis is performed with a test pulse generator and an oscilloscope. It is imperative that testing not be performed with a source and detector until the amplifier and pulse stretcher system performs satisfactorily with the test pulse generator.

The testing instructions in Section 6.1 of this manual and the circuit descriptions in Section 5 should provide assistance in isolating the region of any trouble and repairing the malfunction. The two side plates can be removed completely from the module, with a minimal chance of accidentially short-circuiting portions of the etched board.

If necessary the ORTEC 444 may be returned to ORTEC for repair service at a nominal cost. Our standardized procedure requires that each repaired instrument receive the same extensive quality control test that a new instrument receives.

6.3.2 Possible Problems and Their Solutions

Problem: Unable to get an output pulse.
Solutions:

(1) If the Input switch is set at DC Couple, switch it to BLR High. If this causes the output to appear, a dc level is probably being applied to the 444 input and this locks up the pulse pileup circuit. Adjust the dc output level to zero on the amplifier feeding the signals to the 444.

(2) Adjust the Disc. Level control clockwise. If the output appears, the discriminator was probably set below the system noise level and noise pulses were locking up the pulse pileup circuit.

(3) If the Mode switch is set for the Gated mode, switch it to Normal. If an output occurs, the gating logic is probably not in time coincidence with the linear input signals.

(4) Set the Bias Level control at 000. If an output occurs, the bias level was set too high, biasing off the input signal completely.

6.4 Typical Operating Voltage Levels

The following voltages are intended to indicate the typical dc voltages which can be measured on the printed circuit boards. In some cases, the circuit will perform satisfactorily even though, due to component variation, there may be some voltages that measure other than the typical values. Therefore, these voltages should not be considered as absolute, but rather are intended to serve as an aid in trouble-shooting.

6.4.1 Conditions and Control Settings

Disconnect any Linear Input, and connect a 100 ohm terminator to the 444 Linear Input connector.

Set the controls as follows:

Coarse Gain	X2
Fine Gain	X0.5
Bias Level	000
Input Switch	DC Couple
Mode Switch	Normal
Anti/Coinc Switch	Anti
Strobe Switch	Internal
Disc. Level	Fully clockwise
Gate Period	Fully clockwise
Output Delay	Fully clockwise
DC Adjust	Set for Positive Output dc level at zero ±1mV

Set all internal adjustments per factory quality control procedures, Section 6.2.

6.4.2 Tabulated Voltages for the 444-0201 Board

TYPICAL DC VOLTAGES

LOCATION	VOLTAGE	LOCATION	VOLTAGE
Q1B	+ 12	Q9E	0
Q1C	+ 0.014	Q9B	+ 0.600
Q2B	- 12	Q10D	+ 20.6
Q2C	- 0.485	Q11G	0
Q3E	- 0.580	Q11D	+ 21.900
Q3C	+ 12.5	Q12B	- 2.700
Q4E	- 0.580	Q14C	+ 0.570
Q5B	0	Q15E	- 0.020
Q6B	0	Q16C	+ 24.00
Q8E	0	Q17C	+ 0.010

LOCATION	VOLTAGE	LOCATION	VOLTAGE
Q18G	- 0.020	Q48B	+ 0.110
Q18D	+ 19.3	Q48C	+ 11.9
Q20B	- 2.400	Q49E	+ 4.000
Q21E	+ 19.9	Q49C	+ 5.000
Q22E	0	Q50E	+ 4.650
Q23E	+ 17.0	IC1-4	- 5.900
Q24C	+ 0.640	IC1-2	0.000
Q24B	- 12	IC1-3	+ 0.620
Q25B	+ 0.530	IC1-7	- 0.510
Q26B	- 12.0	IC1-8	+11.20
Q27E	+ 0.790	IC2-14	+ 1.850
Q27B	+ 0.090	IC2-8	+ 0.950
Q28C	+ 0.570	IC2-3	+ 1.600
Q28B	- 2.400	IC2-5	+ 0.140
Q31B	+ 18,200	IC3-3	+ 0.200
Q31C	+ 0.780	IC3-5	+ 3.800
Q32B	+ 0.460	IC3-8	+ 0.110
Q33B	+ 0.685	IC4-5	+ 2.100
Q33C	+ 0.140	IC4-3	+ 3.800
Q34E	0.00	IC4-14	+ 0.110
Q35B	- 0.360	IC4-8	+ 2.100
Q36E	+ 0.330	IC4-9	- 0.500
Q36C	- 12.50	IC5-3	+ 2.100
Q37E	- 12.6	IC5-14	+ 3.800
Q38B	- 12	IC5-8	+ 0.100
Q38C	- 6.2	IC5-5	+ 3.800
Q39B	+ 6.00	IC6-3	+ 0.110
Q39C	+ 1.000	IC6-14	+ 0.090
Q40B	+ 0.450	IC6-8	+ 1.600
Q41B	+ 0.450	IC6-5	+ 2.500
Q42B	+ 6.750	IC6-6	- 0.500
Q42C	+ 0.770	IC6-14	+ 0.110
Q44E	+ 7.400	IC7-3	+ 0.110
Q45B	+ 7.400	IC7-5	+ 2.100
Q46B	+ 0.00	IC8-5	+ 2.500
Q47B	+ 0.110	IC8-14	+ 2.100
Q47C	+ 11.9		

6.4.3 Tabulated Voltages for the 444-0301 Board

TYPICAL DC VOLTAGES

LOCATION	VOLTAGE	LOCATION	VOLTAGE
A1-1	+ 24	A3-10	+ 0.500
A1-4	0	A3-11	+ 12.0
A1-9	- 24	A3-13	- 12.0
A1-10	0	CS-1	+ 24
A1-11	+ 12.5	CS-8	- 6.300
A1-13	- 12.5	CS-9	- 24
A2-1	+ 24	CS-13	- 12
A2-4	0	Q1E	- 13.200
A2-9	- 24	Q1B	- 21.800
A2-10	0	Q2B	+ 13.200
A2-11	+ 12.5	Q2C	+ 21.800
A2-13	- 12.5	Q3B	+ 13.200
A3-1	+ 24	Q3C	+ 21.800
A3-4	0	Q4B	- 13.200
A3-9	- 24	Q4C	- 21.800

7. APPLICATIONS

7.1 Operation in Spectroscopy Systems

High-Resolution Alpha-Particle Spectroscopy System

The block diagram of a high resolution spectroscopy system for measuring natural alpha-particle radiation is shown in Figure 7-1. Since natural alpha-particle radiation only occurs above several MeV, an ORTEC 444 Gated Bias Amplifier is used to suppress the unused portion of the spectrum and to shape the output pulses after biasing to avoid pulse height analyzer nonlinearities.

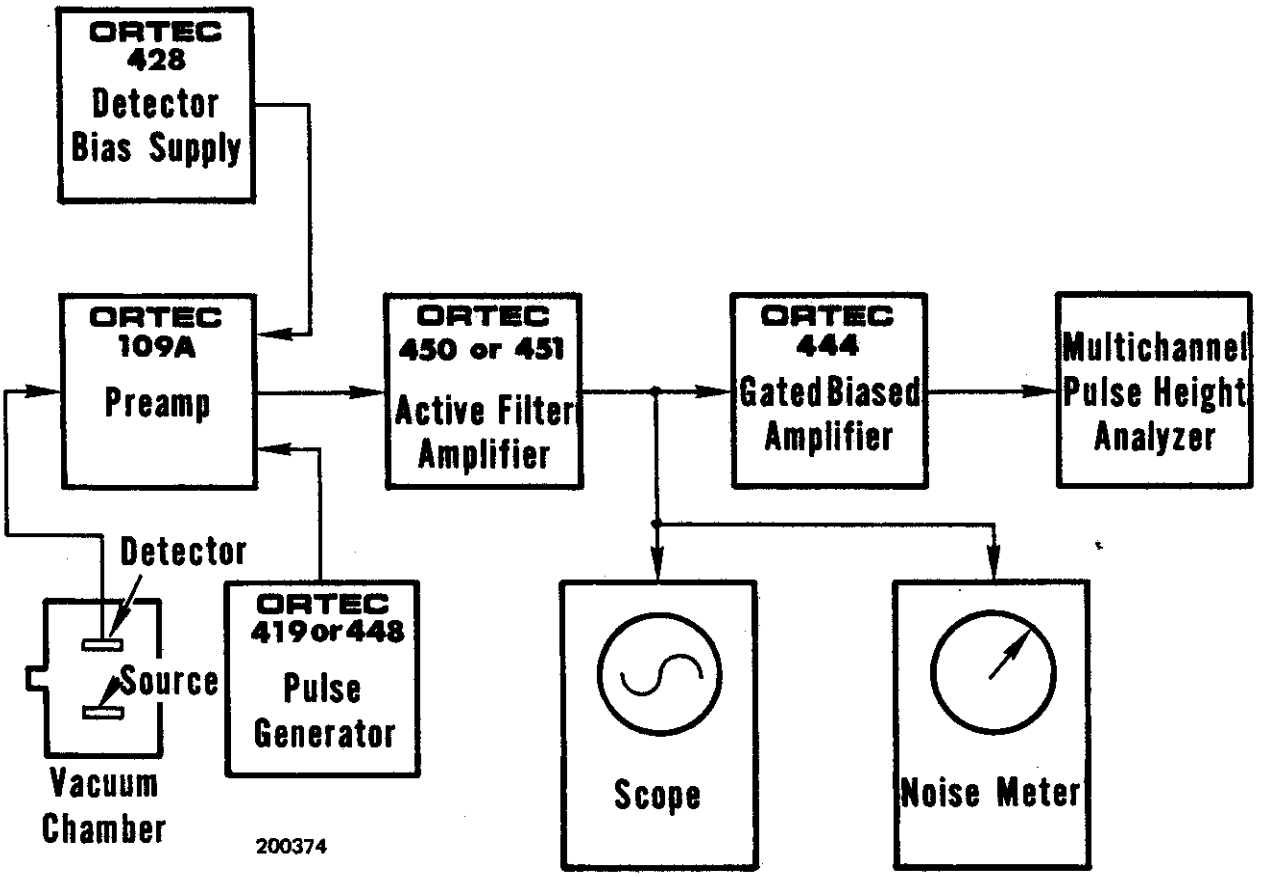


Figure 7-1. High Resolution Alpha Particle Spectroscopy System

Alpha particle resolution is obtained in the following manner:

(1) Using maximum preamplifier gain, medium amplifier gain, and minimum biased amplifier gain and bias level, accumulate the alpha peak in the multichannel analyzer.

(2) Slowly increase the bias level and biased amplifier gain until the alpha peak is spread over 5 to 10 channels and the minimum to maximum energy range desired corresponds to the first and last channels of the analyzer.

(3) Calibrate the analyzer in keV per channel using the pulser and the known energy of the alpha peak.

(4) The resolution can be obtained by measuring the full width at half maximum of the alpha peak in channels and converting to keV.

7.2 High Resolution Gamma Spectroscopy System

A high resolution gamma system block diagram is shown in Figure 7-2.

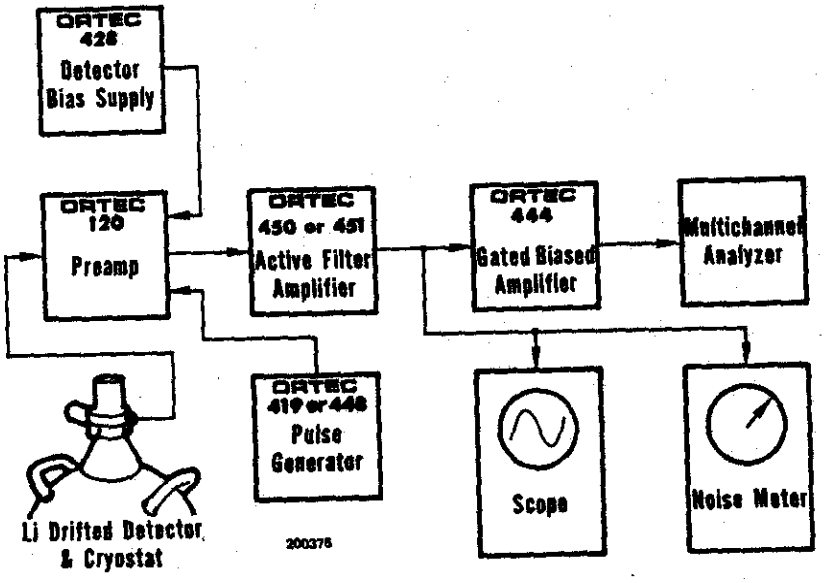


Figure 7-2. High Resolution Gamma Spectroscopy System Using a Lithium Drifted Germanium Detector

When using lithium drifted germanium detectors cooled by a liquid nitrogen cryostat, it is possible to obtain resolutions from about 1 keV fwhm up (depending on the energy of the incident radiation and the size and quality of the detector). Reasonable care is required to obtain such results. Some guide lines for obtaining optimum resolution are:

(1) Keep interconnection capacities between the detector and preamplifier to an absolute minimum (no cables).

(2) Keep humidity low near the detector-preamplifier junction.

(3) Operate in amplifier and preamplifier gain regions which provide the best signal-to-noise ratio.

(4) Operate at the highest allowable detector bias to keep the input capacity low.

7.3 Typical System Block Diagrams

This section contains block diagrams illustrating how the 444 and other ORTEC 400 Series modules can be used in experimental setups.

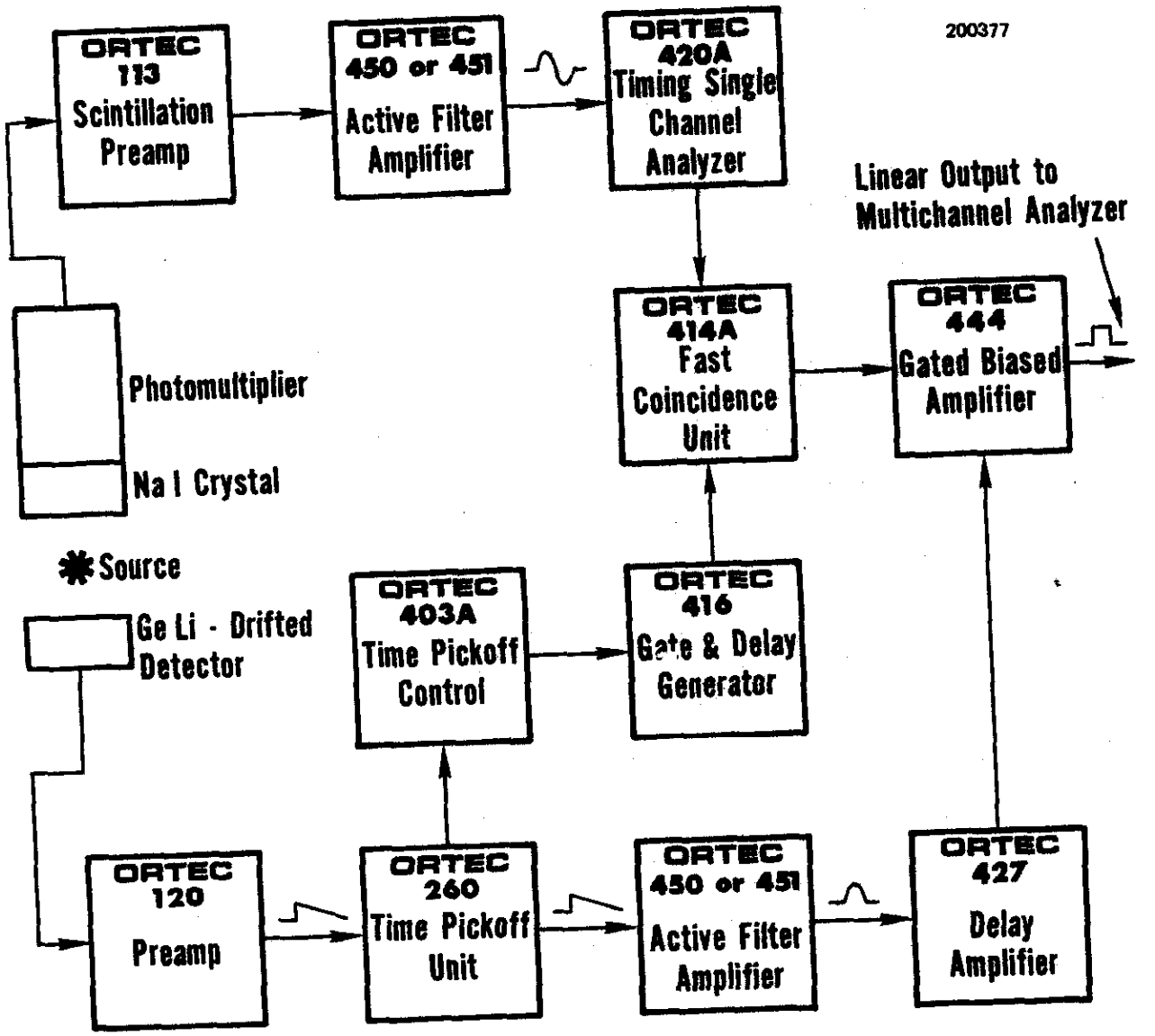


Figure 7-3. Gamma Ray-Gamma Ray Coincidence Experiment - Block Diagram

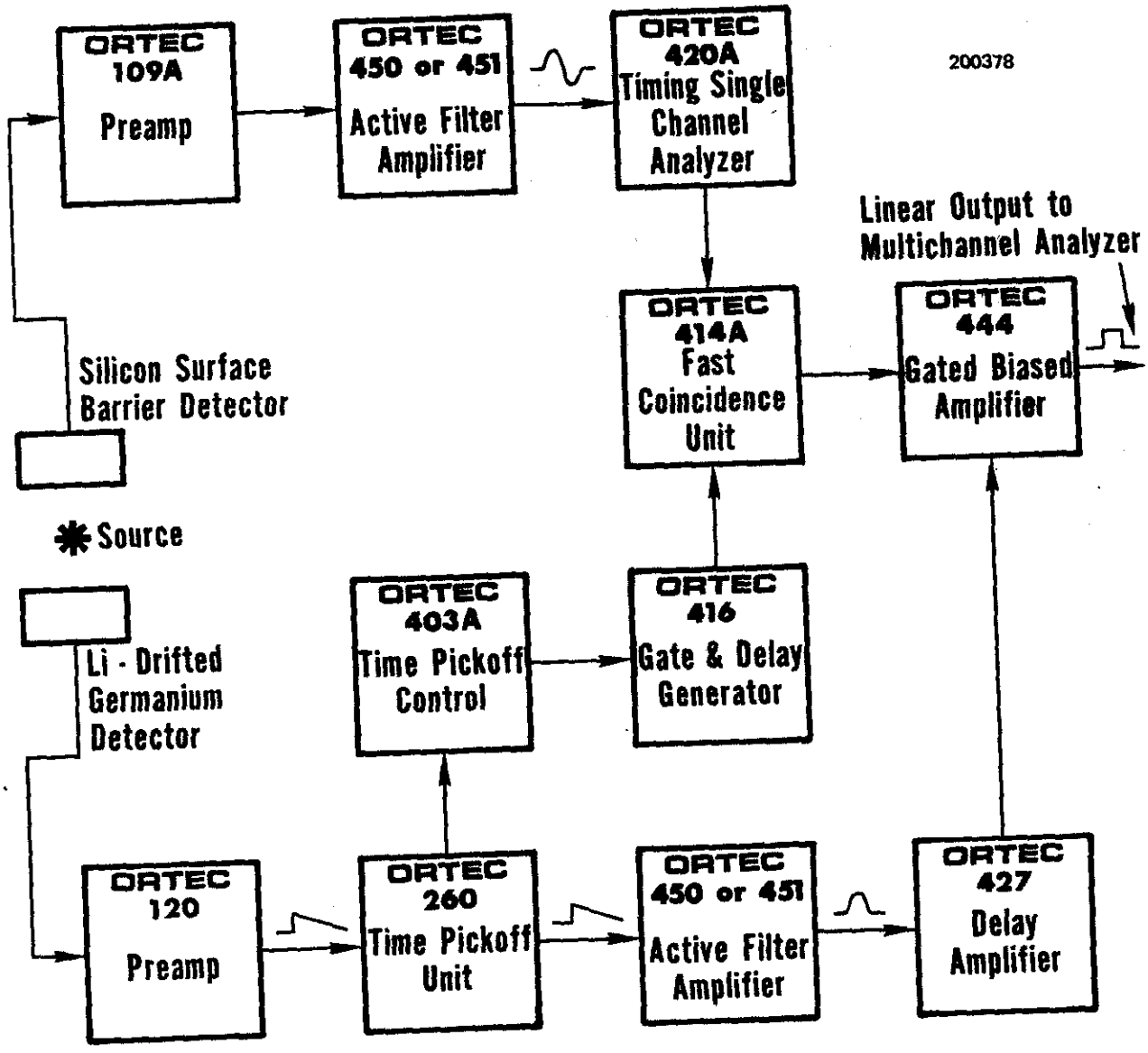
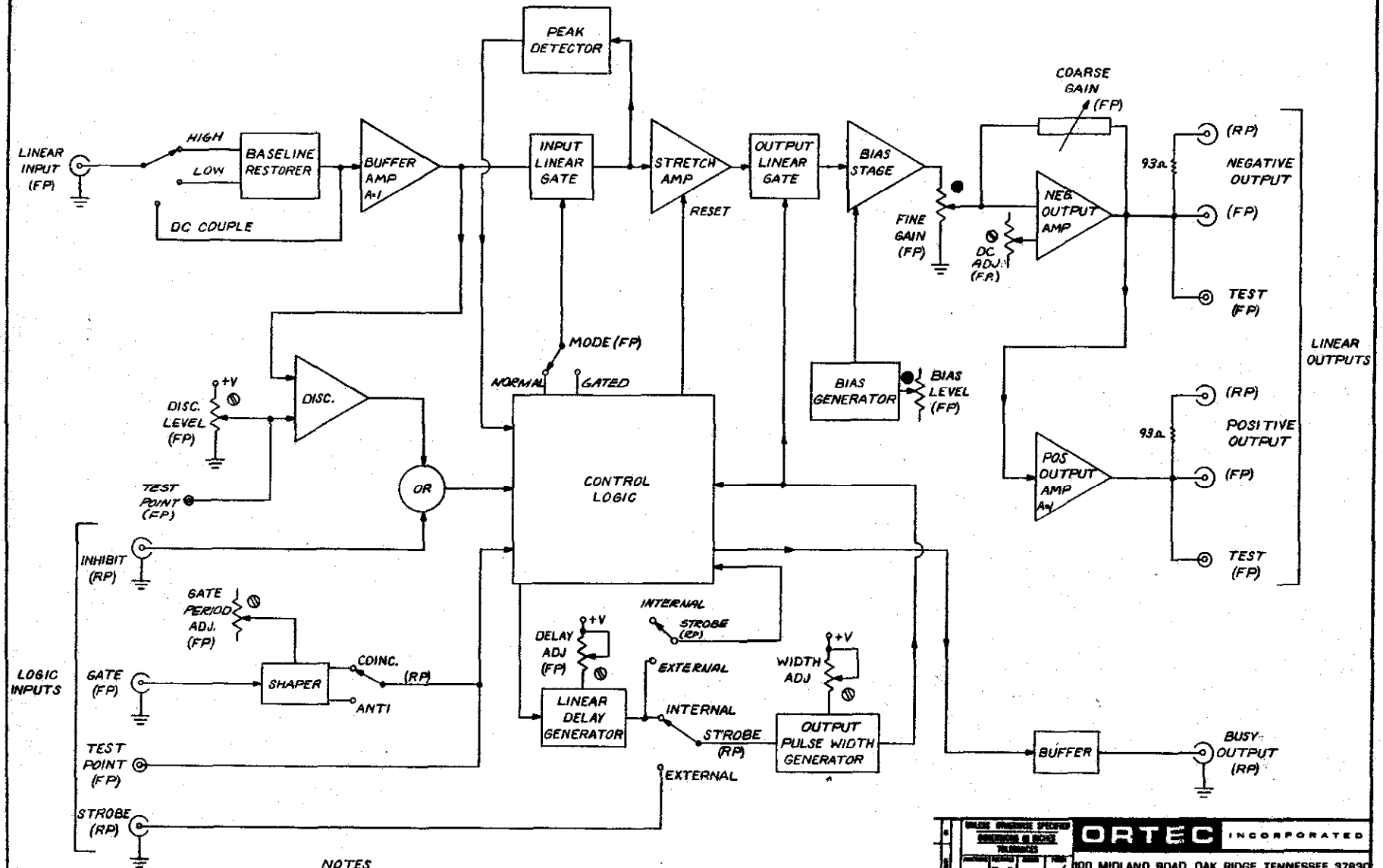


Figure 7-4. Gamma Ray-Charged Particle Coincidence Experiment - Block Diagram

BIN/MODULE CONNECTOR PIN ASSIGNMENTS
FOR AEC STANDARD NUCLEAR INSTRUMENT MODULES
PER TID-20893

Pin	Function	Pin	Function
1	+3 volts	23	Reserved
2	- 3 volts	24	Reserved
3	Spare Bus	25	Reserved
4	Reserved Bus	26	Spare
5	Coaxial	27	Spare
6	Coaxial	*28	+24 volts
7	Coaxial	*29	- 24 volts
8	200 volts dc	30	Spare Bus
9	Spare	31	Carry No. 2
*10	+6 volts	32	Spare
*11	- 6 volts	*33	115 volts ac (Hot)
12	Reserved Bus	*34	Power Return Ground
13	Carry No. 1	35	Reset
14	Spare	36	Gate
15	Reserved	37	Spare
*16	+12 volts	38	Coaxial
*17	- 12 volts	39	Coaxial
18	Spare Bus	40	Coaxial
19	Reserved Bus	*41	115 volts ac (Neut.)
20	Spare	*42	High Quality Ground
21	Spare	G	Ground Guide Pin
22	Reserved		

**These pins are installed and wired in parallel in the ORTEC 401A Modular System Bin.*



NOTES

1. (FP) INDICATES FRONT PANEL.
2. (RP) INDICATES REAR PANEL
3. ⊘ INDICATES MULTITURN SCREWDRIVER ADJUSTMENT.
4. ● INDICATES MULTITURN KNOB ADJUSTMENT.

UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES TOLERANCES

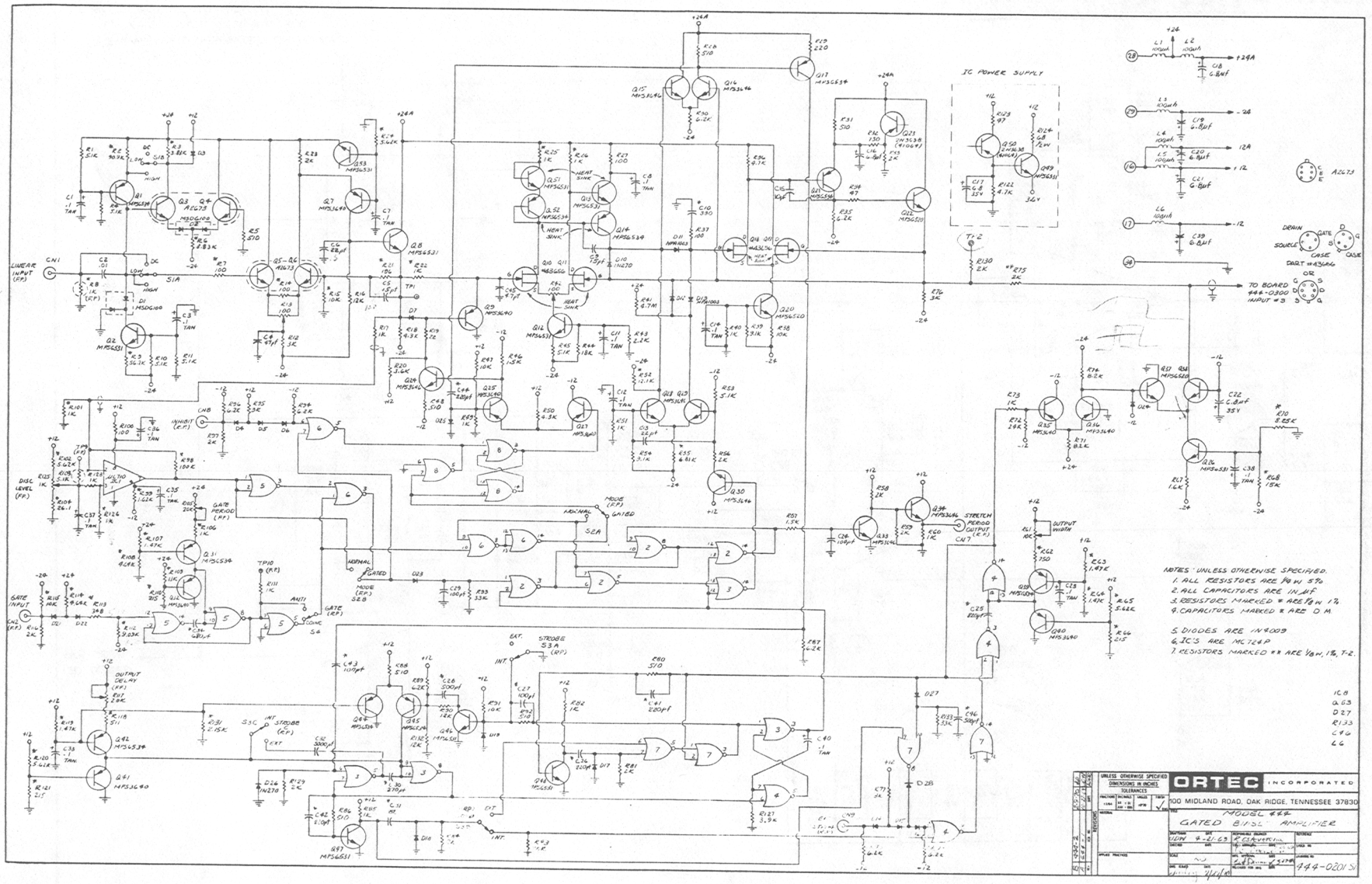
ORTEC INCORPORATED

100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830

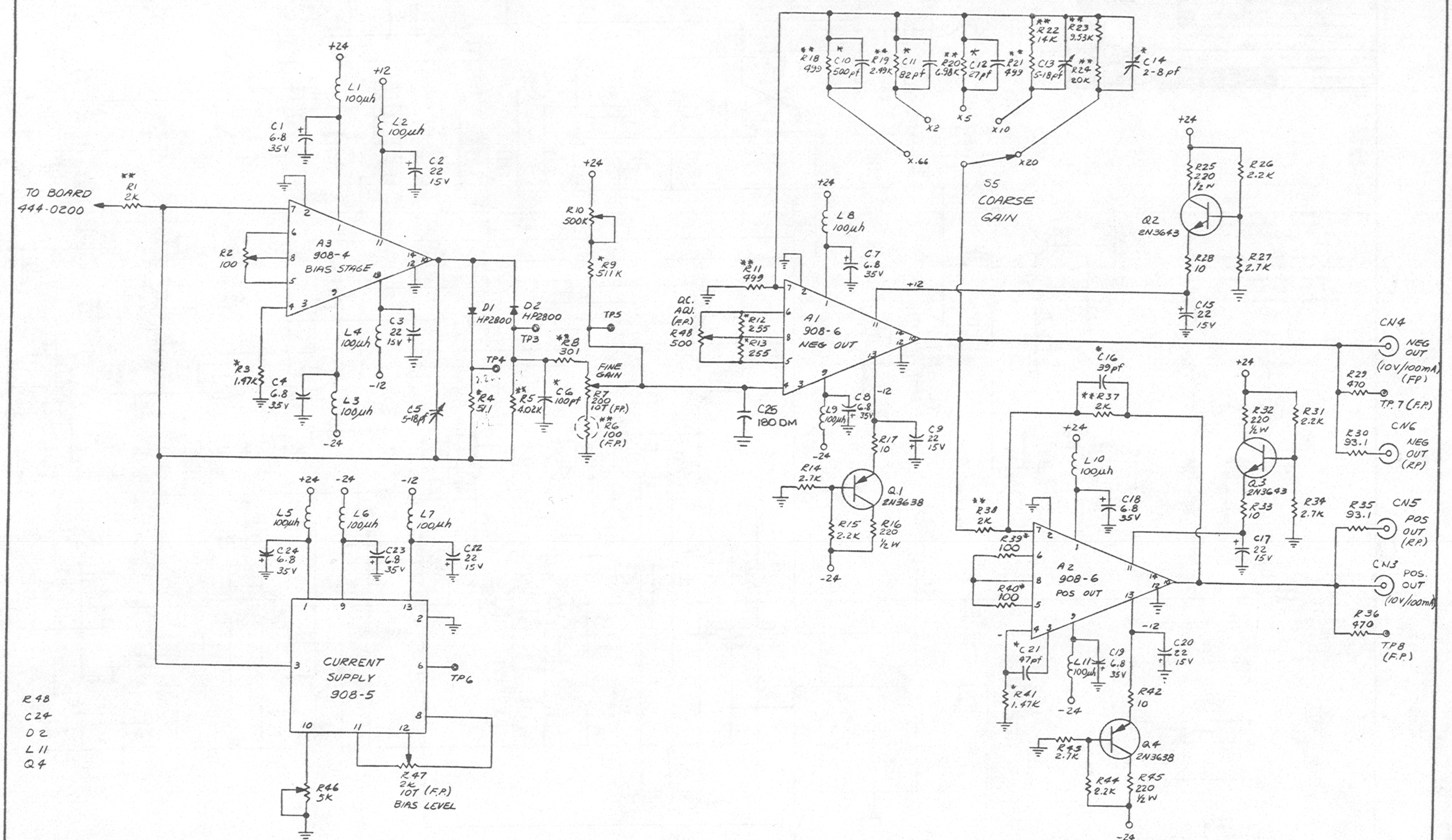
GATED BIASED AMPLIFIER BLOCK DIAGRAM

M.KENT 4-29-69 R.E.STEVERENA

444-0101-B1


IC POWER SUPPLY
NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTORS ARE ¼W 5%
2. ALL CAPACITORS ARE IN μF
3. RESISTORS MARKED * ARE ¼W 1%
4. CAPACITORS MARKED * ARE D.M.
5. DIODES ARE IN4009
6. ICS ARE MC724P
7. RESISTORS MARKED ** ARE ⅛W, 1%, T-2.
IC 8
Q 63
D 27
R 133
C 96
L 6
UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES
TOLERANCES
ORTEC INCORPORATED
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830
MODEL 444
GATED BI/SL AMPLIFIER
444-0201 SH

7-29-70



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE ¼W, 5%
2. ALL CAPACITORS ARE IN µf CER.
3. RESISTORS MARKED * ARE ⅛W 1%.
4. CAPACITORS MARKED * ARE D.M.
5. RESISTORS MARKED ** ARE ⅛W, 1%, T-2

REV	ECN NO	DATE	APPR
B	444-2	2-9-70	BD
A	444-1	10-27-69	JDW

REVISIONS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES
TOLERANCES
FRACTIONS ±1/64 DECIMALS XX ±.01 XXX ±.005 ANGLES
FINISH ✓
MATERIAL
APPLIED PRACTICES

ORTEC INCORPORATED
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830

TITLE MODEL 444
GATED BIASED AMPLIFIER

DRAFTSMAN JDW DATE 4-1-69
CHECKED
SCALE
DWG ISSUED
RESPONSIBLE ENGINEER
MFG. APPROVAL
RELEASED FOR MFG
REFERENCE
STOCK NO.
DRAWING NO. 444-0301-31