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P R E L I M I N A R Y

ORTEC 934
QUAD CONSTANT FRACTION
100 MHz DISCRIMINATOR
INSTRUCTION MANUAL

ORTEC 934

QUAD CONSTANT FRACTION 100 MHz DISCRIMINATOR

Operating and Service Manual Manuscript

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934-0201-S1

1. DESCRIPTION

The ORTEC 934 Quad Constant Fraction 100 MHz Discriminator is a single-width NIM module that includes four independent fast constant fraction discriminators. Each section of this instrument accepts negative input pulses and generates three simultaneous NIM-standard fast negative logic pulses for each input pulse that exceeds the adjusted threshold level. The design of this instrument utilizes advanced ORTEC hybrid circuit technology to achieve maximum performance and high reliability in a high-density package.

The constant fraction technique permits optimum timing measurements to be made with photomuptiplier tubes or fast solid state detectors. Each input signal is split so that a portion of the signal is delayed and subtracted from a fraction of the undelayed signal. The resulting bipolar constant fraction signal has a baseline crossover that is virtually independent of the input signal amplitude. The zero crossing point is detected and used to provide precisely timed logic pulses for a wide dynamic range of input signals.

Each of the four channels includes an independently adjustable threshold level to prevent output signals from being generated in response to noise or small-amplitude input signals. The input circuit has an impedance of 50Ω and is protected against overload. The input signals should be furnished through 50Ω coaxial cable to ensure proper termination with minimum reflections at the input of the 934.

Each channel of the 934 includes an updating one-shot and output voltage driver circuit. This circuit generates three simultaneous negative NIM fast logic signals for each input signal that satisfies the discriminator criteria.

The constant fraction shaping delay for each discriminator channel is determined by the length of 50Ω coaxial cable that must be added between two front panel LEMO connectors. The shaping delay can be optmiized for each specific application. This optimization requires prior knowledge of the rise time and nominal width of the input signals to the 934.

A common gating circuit can be used to control responses in all four channels simultaneously. The position of a rear panel switch determines whether the gating signals from the bin are accepted or not. The bin must be constructed with a Gate input connector on the rear panel and distribution of the gating line through pin 36 of each power connector in the bin.

The 934 operates in an ORTEC 401A/402D or M/400N NIMBIN^{R} that includes distribution of dc power at ±24 V, ±12 V, and ±6 V. By using either of these recommended bins and power supplies, a full complement of 12 ORTEC 934 modules can be operated in the bin, with a total capacity of 48 constant fraction discriminator channels.

2. SPECIFICATIONS

2.1. PERFORMANCE

Number of Channels Four, completely independent except for gating.

Input/Output Rate >100 MHz (typically >110 MHz).

Pulse Pair Resolution <10 ns (typically <9 ns).

Walk ≤±150 ps, 200:1 dynamic range (-50 mV to -10 V) with $t_r \leq 1$ ns, $t_{pw} \geq 10$ ns, $t_{d(Tot)} \geq 3$ ns, threshold = 30 mV.

Time Slewing <750 ps from half-fire, measured with $t_r = 1.8$ ns, $t_f = 2.0$ ns, $t_{pw} = 3.1$ ns at half-height, $t_{d(Tot)} = 1.5$ ns, threshold = 30 mV.

Propagation Delay 13 ns typical from input to output using $t_d = 1.5$ ns.

Operating Temperature Range 273 to 323 K (0 to 50°C).

Threshold Temperature Instability <0.1% per degree from 273 to 323 K (0 to 50°C). Referenced to -12 V power supply level.

Propagation Delay Instability <15 ps per degree (typically <10 ps per degree) from 273 to 323 K (0 to 50°C).

Output Width Temperature Instability <0.2% per degree from 273 to 323 K (0 to 50°C).

2.2. CONTROLS

Threshold (T) 20-turn front panel screwdriver adjustment for each discriminator channel; variable from -30 to -1000 mV. The adjusted level can be measured on the adjacent test point, where a dc voltmeter will indicate 10X threshold (-0.3 to -10 V).

Updating Width (W) 20-turn front panel screwdriver adjustment for each discriminator channel; variable range <6 ns to >150 ns.

Shaping Delay A pair of LEMO connectors for each discriminator channel accepts 50Ω coaxial cable to adjust the required shaping delay; total shaping delay is ∿0.7 ns plus delay of external cable.

Walk (Z) 20-turn screwdriver front panel adjustment in each channel for precise setting of the walk compensation network for each application. The zero-crossing reference can be measured at the adjacent front panel test point with a dc voltmeter. Under most conditions a level of -0.5 mV to -1.5 mV should be set.

Gate Rear panel On/Off toggle switch to control use of a master gate signal that can be furnished to all four channels in the module.

2.3. INPUTS

Input Front panel LEMO connector for each discriminator channel. Linear range 0 to -10 V. Signal input impedance 50Ω, dc coupled. Input protected. Input reflections <10% for signals with rise time >2 ns.

Gate Master gate signal enabled by the rear panel Gated-Ungated locking toggle switch; connected through pin 36 in the NIM power connector to a gate line that is common to pin 36 at all module locations in the bin. When the switch is set at Gated, a clamp to ground from +5 V inhibits operation of all four discriminator channels.

2.4. OUTPUTS

Out Three bridged updated negative outputs are furnished through front panel LEMO connectors; each discriminator channel is independent from the other channels in the module. Amplitude at each connector, -800 mV into 50Ω; width adjustable from <6 ns to >150 ns; rise and fall times typically <2 ns.

Threshold Monitor Front panel test point for each discriminator channel permits monitoring the threshold level adjustment with an external dc voltmeter; indications of -0.3 to -10 V correspond to adjusted threshold levels of -30 to -1000 mV.

CF Monitor Front panel LEMO connector for each discriminator channel permits observation of the constant fraction shaped signal; 50Ω cable required.

Walk Monitor Front panel test point permits monitoring the actual dc voltage level that is set for the zero-crossing reference, which should normally be set in the range from -0.5 mV to -1.5 mV.

2.5. ELECTRICAL AND MECHANICAL

Power Required +6 V, 150 mA; -6 V, 280 mA;
+12 V, 75 mA; -12 V, 30 mA;
+24 V, 0 mA; -24 V, 80 mA;
110 V ac, 20 mA.
Total dissipation, 8.0 W.

Dimensions NIM-standard single width module (1.35 x 8.714 in. front panel) per TID-20893 (Rev.).

2.6. ACCESSORY

A small screwdriver is included with each 934 Quad CF Discriminator, and can be used for threshold, width, and walk adjustments.

3. INSTALLATION

3.1. GENERAL

The 934 power requirements must be furnished from a nuclear-standard bin and power supply that includes the ±6 V power distribution, such as the ORTEC 401A/402D Bin and Power Supply. The ORTEC M400/N NIMBIN also provides the required power distribution and, in addition, includes the wiring and rear panel connector necessary for the common gating line that can be used with the 934.

The bin and power supply in which the 934 will normally be operated is designed for relay rack mounting. If the equipment is rack mounted, be sure that there is adequate ventilation to prevent any localized heating in the 934. The temperature of equipment mounted in racks can easily exceed the maximum limit of 50° C (323 K) unless precautions are taken.

3.2. CONNECTION TO POWER

Turn off the Bin Power Supply before inserting or removing any modules. ORTEC modules are designed so that a full complement of these modules in the 12 bin positions will not overload an ORTEC 402D Power Supply. However, this may not be true when a different power supply is used or when modules not designed by ORTEC are included in the bin. To be sure of proper operation, check the dc voltage levels of the power supply after all modules have been installed in the bin. ORTEC bins and power supplies include convenient test points on the power supply control panel to permit monitoring these levels.

3.3. INPUT CONNECTIONS

Each discriminator channel includes an input connector on the front panel that is terminated internally in 50Ω. Connect the source of negative input signals to this connector through a 50Ω coaxial cable and a mating LEMO connector. Any of the four channels can be provided with an input signal and will operate independently from all other channels.

3.4. OUTPUT CONNECTIONS

There are three output connectors for each channel. These connectors furnish three identical, simultaneous, negative NIM logic signals for each input pulse that exceeds the adjusted threshold level. The updating width of the output pulses can be adjusted by the front panel W control associated with that channel.

Each output connection should be furnished through a mating LEMO connector and a 50Ω coaxial cable to a 50Ω load impedance. For best results, terminate one unused output connector in each active channel with a 50Ω terminator on the front panel. Termination is not necessary for unused channels.

3.5. GATING

If the 934 is operated in an ORTEC M400/N NIMBIN or equivalent, gating control can be accepted simultaneously for all four discriminator channels from the common gating line that is wired through the rear panel power connector. To accept gating control, set the rear panel locking toggle switch at Gated. To inhibit this control for the module, set the switch at Ungated. The switch is accessible when the module is installed in the bin and can be changed at any time.

3.6. CONSTANT FRACTION DELAY CABLE SELECTION

The shaping delay for each channel is adjusted by selecting an appropriate length of 50Ω coaxial cable and adding it between the two Delay LEMO connectors on the front panel. The length of cable determines the amount of external signal delay that is added to the ∿0.7 ns internal delay to constitute the total constant fraction shaping delay.

$$t_{D(Tot)} \simeq t_{d(Ext)} + 0.7 \text{ ns.}$$

The primary useage of the 934 is expected to be in fast timing or counting experiments with scintillators and photomultiplier tubes (PMT's). In these applications, the constant fraction shaping delay, $t_{D(Tot)}$, is selected so that the zero-crossing of the bipolar timing signal occurs after the attenuated, undelayed portion of the constant fraction signal has reached its maximum amplitude. Thus the zero-crossing occurs at the same fraction of the input pulse height, regardless of the amplitude of the input signal.

Selection of the constant fraction shaping delay for best timing performance with a given scintillator and PMT is usually accomplished experimentally. The randomly generated signals from the anode of the PMT are applied to the input of one channel of the discriminator. Each of the two CF Delay connectors should be terminated with a 50Ω terminator. The CF Monitor signal can then be observed on a fast oscilloscope (bandwidth ≥300 MHz), which is terminated in 50Ω and triggered internally. The Monitor signal represents the attenuated, undelayed portion of the constant fraction signal with no delayed signal subtracted from it. The addition of

the appropriate external CF shaping delay, $t_{D(Ext)}$, causes the resulting bipolar signal at the CF Monitor to cross the baseline after the peak of the attenuated, undelayed signal and before approximately 0.9 times its maximum amplitude. A useful empirical formula for the initial trial selection of the external shaping delay is

$$t_{D(Ext)} \approx 1.1t_r - 0.7 \text{ ns}$$

where t_r is the 10% to 90% risetime of the anode pulse. Walk adjustment can then be accomplished while observing the delayed CF Monitor signal on a fast oscilloscope, which is triggered externally by the output signal from the constant fraction discriminator. The walk potentiometer (Z) should be adjusted so that the bipolar constant fraction signals for all amplitudes cross through the baseline at approximately the same time.

Figure 3.1(a) illustrates the anode signals from an RCA 8850 PMT with a 1" x 1" KL236 scintillator and a ^{60}Co source. The (b) and (c) portions of Fig. 3.1 show the resulting delayed CF Monitor signal seen on a sampling oscilloscope, triggered by the discriminator output signal. The CF delay and walk adjust have been set properly and the spread in the zero-crossing time is less than 100 ps.

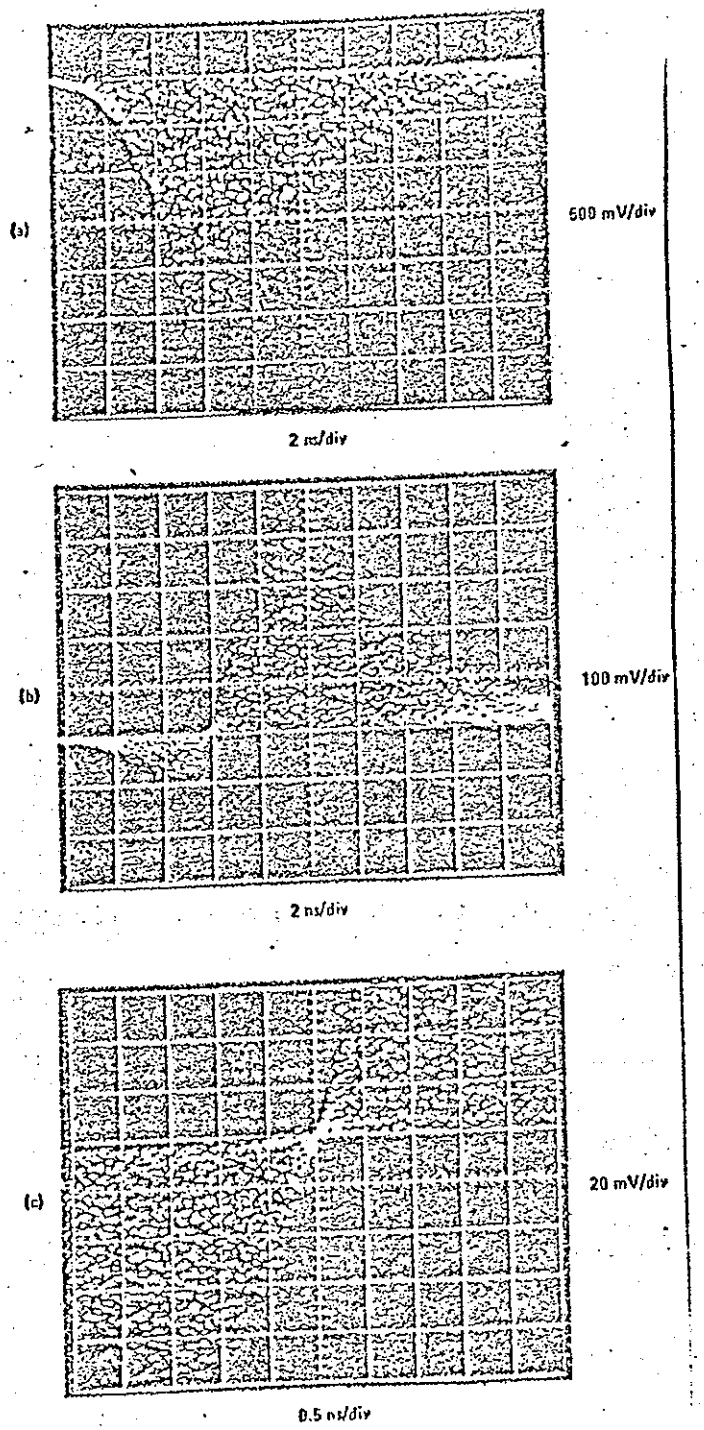

Fig. 3.1(a) RCA 8850 PMT anode signal with a 1" x 1" KL236 scintillator and ^{60}Co source. (b) Constant fraction zero-crossing monitor signal, triggered by the discriminator output for the anode signal shown above. (c) Expanded view of the constant fraction zero-crossing monitor signal. CF delay ≈ 3 ns; threshold = 30 mV.

4. OPERATING INSTRUCTIONS

Each channel has an input connection and up to three output connections. The discriminator threshold, the updating output width, and the walk characteristics can be adjusted in each channel independently as required by the application.

To adjust the threshold level, measure the dc voltage from the front panel threshold monitor test point to ground for the active channel. The nominal range of voltages at this test point is from -300 mV to -10 V, corresponding to the actual threshold which is 10% of the test point voltage. Use the special accessory screwdriver that is furnished with the 934 to set the threshold level with the control marked T.

To adjust the updating output width, provide an input pulse that exceeds the adjusted threshold at a rate less than 5 MHz and observe the width of an output pulse from any of the three output connectors. Use the special accessory screwdriver that is furnished with the 934 to set the control marked W for the output width in the active channel; the width can be adjusted within the specified range from <6 ns through >150 ns.

To adjust the walk characteristics, connect the signal source to be used to the Input connector in the active channel and connect the signal from the constant fraction Monitor connector to a fast oscilloscope through a 50Ω delay. The constant fraction shaped signal can be observed on the oscilloscope, triggered by an undelayed output signal from the active discriminator channel. Select the constant fraction shaping delay according to the information in Section 3.6. Adjust the walk (Z) control, which sets the zero-crossing reference,

so that the bipolar constant fraction signals for all input amplitudes cross through the baseline at approximately the same time. The adjacent test point can be used for resettability of the zero-crossing reference. Under most operating conditions, the dc voltage level at the test point should be in the range from -0.5 mV to -1.5 mV. Use the special accessory screwdriver that is furnished with the 934 to adjust the Z control.

Each unused channel can be disregarded without affecting operation in any of the active channels.

5. THEORY OF OPERATION

A complete schematic of the ORTEC 934 Quad Constant Fraction 100 MHz Discriminator is included at the back of this manual. Figure 5.1 is a simplified block diagram of the instrument that can be used as a reference to describe how it operates.

An input of 0 to -10 V amplitude starts at time zero and is applied simultaneously to the constant fraction (CF) circuitry and to the leading edge discriminator (LLED) circuitry. The LLED has an adjustable threshold, ranging from -30 mV to -1 V, that determines the minimum input signal amplitude that is required to produce an output pulse from the instrument. If the input signal exceeds the LLED threshold, that comparator produces an output pulse that arms zero crossing gate G1.

A differential transformer technique is used to passively form the constant fraction bipolar signal. An associated thick film resistive network ensures proper impedance matching. The CF circuit sets a constant fraction attenuation factor of f = 0.2. The related 50Ωshaping delay must be provided externally. Walk adjustment is accomplished by varying the voltage applied to one input terminal of the CFA. Note that access for monitoring the bipolar signal is provided through buffer amplifier A1. The CFA output is furnished to gate G1, which must have been armed by the LLED output to permit a response to be generated.

The passively formed constant fraction bipolar timing signal is amplified by CFA and crosses the logic threshold at the zero crossing gate at time t_{CF}. Time t_{CF} is determined by the selection of the

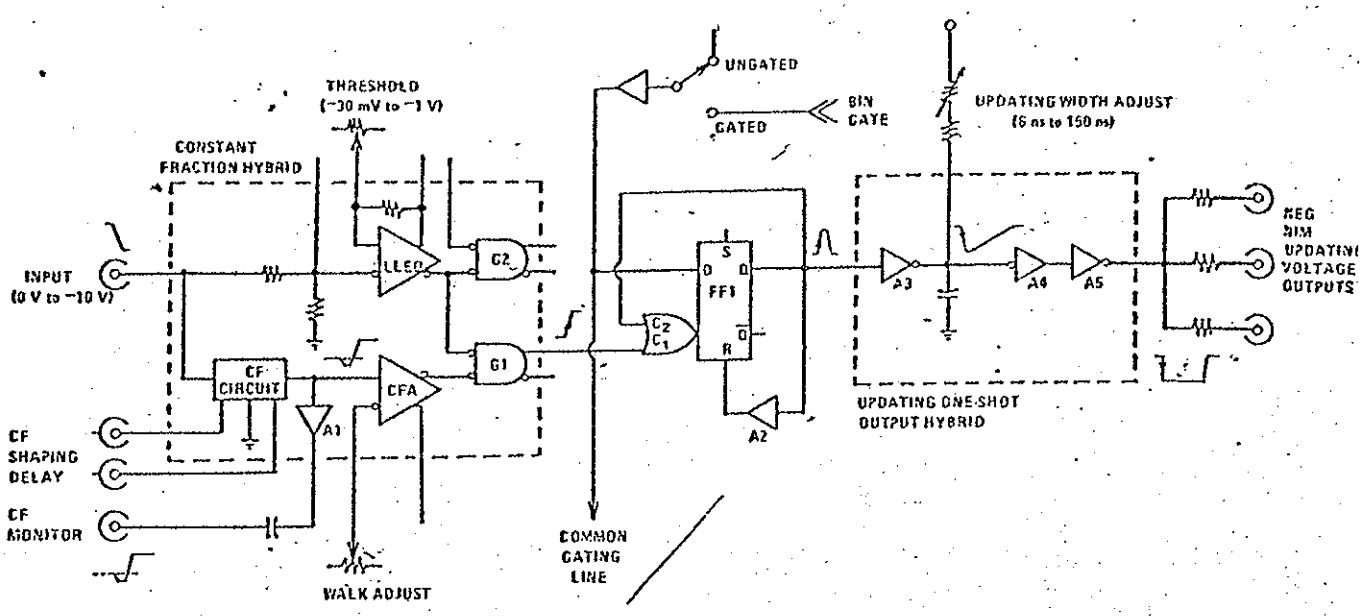

Fig. 5.1. Simplified Block Diagram of One Channel in the 934.

external constant fraction shaping delay, $t_{D(Ext)}$, subject to the rise times and pulse shapes of the input signals. A fixed internal delay of 0.6 ns to 0.7 ns must be added to $t_{D(Ext)}$ to obtain the total constant fraction shaping delay, $t_{D(Tot)}$.

$$t_{D(Tot)} \approx t_{D(Ext)} + 0.65 \text{ ns.}$$

The timing logic signal from gate G1 triggers a fast one-shot, comprised of an ECL type D master-slave flip flop, FF1, and amplifier A2. FF1 produces a reshaped logic pulse with a fixed 2 ns width for each signal from gate G1. The reshaped signal drives a hybridized updating one-shot and output circuit that includes a capacitor and amplifiers A3 through A5. The updating capacitor is charged to its maximum capacity at each signal through A3. At the end of the 2 ns charging interval, the updating capacitor begins to discharge through the series resistance that includes the width adjustment. A4 and A5 amplify and shape the signal on the updating capacitor to a fast

voltage output signal that is capable of driving three 50Ω loads simultaneously with NIM standard negative fast logic pulses. The output width of the updating one-shot is continuously variable from less than 6 ns to greater than 150 ns. Each reshaped logic signal that occurs at the input of the updating hybrid during the width of an output pulse extends that output pulse by one full preset updating width.

A common gating circuit can be used to simultaneously enable or inhibit the output responses of all four channels in the 934. The position of the rear panel Bin Gate switch determines whether gating signals from the bin are accepted or not. Gating control is established at the D input of the ECL type D master-slave flip flop in each channel.

The dc power requirements are shown in schematic 934-0201-S1. The power levels at +6, -6, +12, -12, and -24 V are all obtained directly from the bin power supply. The ORTEC Hybrid packages also require dc power at -3.0 V, -5.2 V, and +6.0 V; each of these levels is obtained from a regulator and is adjustable on the printed circuit board. Monitor points are provided on the board for each of the adjustable dc power levels.

6. MAINTENANCE

6.1. CALIBRATIONS

Four precise dc voltage levels are generated in the 934 to provide operating power for the integrated circuit packages and the ORTEC Hybrids. There are test points on the printed circuit at which the voltage levels can be monitored while they are adjusted. If any of the levels needs adjustment, use the following procedure:

1. Adjust R6 for a reading of -5.2 V at both TP1 and TP2.
2. Adjust R14 for a reading of -3.0 V at TP3.
3. Adjust R27 for a reading of +6.0 V at TP4.

6.2. TYPICAL DC VOLTAGES

Table 6.1 lists typical values for voltages at various points in the printed circuit when the instrument is operating properly. The readings are not absolute, but are furnished as a guide to check any portion of the system that is suspected of malfunction. All voltages were measured with respect to ground, with the T and W controls set at minimum, and the Z control set for -5 mV.

The readings shown for A101, IC101, Q101, and A102 were taken in the components in channel 1. They are typical for readings that should also be present at the equivalent circuit points in channels 2 through 8.

Table 6.1. Typical DC Voltages

IC1	pin 1	-12.0	IC2	pin 1	-12.0
	2	-5.2		2	-5.2
	3	-5.2		3	-5.2
	4	-12.0		4	-12.0
	5	-12.0		5	-12.0
	6	-5.84		6	-5.86
	7	+12.0		7	-12.0
	8	0		8	0

Table 6.1. (Continued)

IC3	pin 1	-12.0
	2	-0.89
	3	-0.89
	4	-12.0
	5	-12.0
	6	-3.48
	7	+12.0
	8	0

IC4	pin 1	-12.0
	2	0
	3	0
	4	-12.0
	5	-12.0
	6	+6.61
	7	+12.0
	8	0

Q1	E	-5.2
	B	-5.82
	C	-8.44

Q2	E	-5.20
	B	-5.87
	C	-6.02

Q3	E	-3.0
	B	-3.45
	C	-12.0

Q4	E	+6.0
	B	+6.62
	C	+12.0

Q5	E	-0.68
	B	-0.08
	C	0

A101	pin 1	0.0
	2	0.0
	3	-0.73
	4	0.0
	5	+5.92
	6	0
	7	-1.15
	8	-5.2
	9	+0.18
	10	-1.77
	11	0
	12	-5.09
	13	+0.11
	14	-1.81
	15	0
	16	-13.8
	17	0.0
	18	0.0
	19	0.0
	20	0.0

A102	pin 1	-1.81
	2	-5.2
	3	-3.0
	4	0.0
	5	+0.43
	6	+0.43
	7	+6.0
	8	-3.0
	9	0
	10	0

Q101	E	-1.77
	B	-2.50
	C	-5.20

Table 6.1. (Continued)

IC101	pin 1	0.0
	2	-1.81
	3	+0.06
	4	-1.74
	5	-4.87
	6	0.0
	7	-1.81
	8	-5.2
	9	0.0
	10	-0.68
	11	0.0
	12	0.0
	13	0.0
	14	0.0
	15	0.0
	16	0.0

6.3. FACTORY SERVICE

This instrument can be returned to the ORTEC factory for service and repair at a nominal cost. The ORTEC standard procedure for repair ensures the same quality control and checkout that are used for a new instrument. Always contact Customer Services at ORTEC, (615) 482-4411, before sending in an instrument for repair to obtain shipping instructions and so that the required Return Authorization Number can be assigned to the unit. This number should be written on the address label and on the package.

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A VERSATILE CONSTANT FRACTION 100 MHz DISCRIMINATOR

M.O. Bedwell and T.J. Paulus*

Introduction

A new constant fraction discriminator having excellent timing characteristics over a wide dynamic range of signals has been designed and tested. To achieve maximum timing performance, the most critical block of circuitry has been implemented using hybrid microcircuit technology. This block includes the leading edge arming discriminator, the constant fraction shaping circuitry and the zero-crossing pickoff. The basic constant fraction building element indicated above operates to a minimum threshold of -30 mV and can accept input signals to -10 V without overload. Amplitude-dependent time walk is less than ±150 ps for a 200:1 dynamic range of input signals (t_r = 1 ns). The count rate capability of this constant fraction hybrid exceeds 100 MHz.

A four-channel, 100 MHz constant fraction updating discriminator that uses the hybrid element has been developed and extensively tested. The primary design goal in this discriminator was the 100 MHz count rate capability with significantly improved timing performance over fast leading edge discriminators. A block diagram and the various functions of this instrument are described. Typical performance data and timing resolution data are presented.

Constant Fraction Discriminator Implementation

A functional representation of a constant fraction trigger is shown in Fig. 1. In the constant fraction method the input signal to the circuit is delayed and a fraction of the undelayed pulse is subtracted from it. A bipolar pulse is generated and its zero-crossing is detected and used to produce an output logic pulse.

Several circuit techniques have been used to perform the functions of deriving the constant fraction bipolar timing signal and of detecting its zero-crossing. Initial usage of the constant fraction method was reported by Gedcke and McDonald[1] in 1967. These first generation discriminators contained a pulse transformer to invert the delayed input signal. The delayed, inverted pulse and the resistively attenuated input signal were then current-summed in a limiter circuit and tunnel diode. The tunnel diode was enabled by an arming discriminator to detect the zero-crossing of the bipolar timing signal. A similar technique was employed and reported by Chase[2] in 1968 and again by Cho and Chase[3] in 1972. A variation on this technique was described in 1972 by Karlsson,[4] who used a bipolar common-base amplifier to accomplish the current sum of the delayed, inverted pulse and the resistively attenuated input signal. After further amplification of the bipolar signal using cascaded ECL line receivers, the leading edge enabling and zero-crossing functions were performed at an ECL NAND gate.

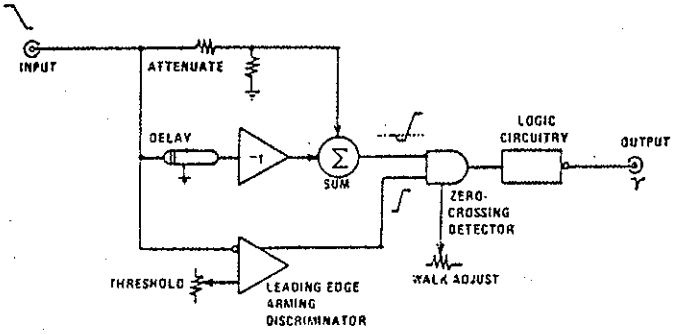

Fig. 1. Functional representation of a constant fraction trigger.

In 1975 Leskovar and Lo[5] published timing results using a discriminator that contained a pulse transformer to derive the difference between the attenuated and delayed input signals. The bipolar timing signal was then amplified and a tunnel diode was armed to detect the zero-crossing.

In the discriminator reported by Arbel et al,[6] in 1974, the input signal was first amplified and then split into attenuated and delayed components. The subtraction of the delayed signal from the attenuated signal was accomplished at the base-emitter junction of a transistor. After amplification of the bipolar timing signal, the zero-crossing of the timing pulse was detected with a snap-off diode.[7]

Maier and Sperr[8] reported on a discriminator using cascaded ECL differential line receivers to form the constant fraction bipolar signal. The delayed and attenuated input signals were applied to the two input terminals of the resulting differential amplifier. The leading edge enabling and zero-crossing functions were performed at an ECL NAND gate. Bedwell and Paulus and several other authors have reported similar implementations employing MECL II, MECL 10,000 and fast ECL comparator technologies in a variety of logic configurations.[9-16]

Figure 2 is a simplified block diagram of the hybridized constant fraction element used in the instrument reported in this paper. A differential transformer technique is used to passively form the constant fraction bipolar signal. Particular attention has been given to the design of the associated thick film resistive network to ensure proper impedance matching. This network sets a constant fraction attenuation factor of f = 0.2. The related 50Ω shaping delay must be provided externally. The passively derived bipolar timing signal is amplified by the fast differential constant fraction amplifier, CFA, and applied to the input of gate G1, which detects the zero-crossing. Walk adjustment is accomplished by varying the voltage applied to one input terminal of the CFA. Note that access for monitoring the bipolar timing signal is provided through buffer amplifier A1. The fast leading edge discriminator, LLED, provides the leading edge arming signal to the zero-crossing gate, G1. The various logic signals available from the hybrid are indicated in Fig. 2.

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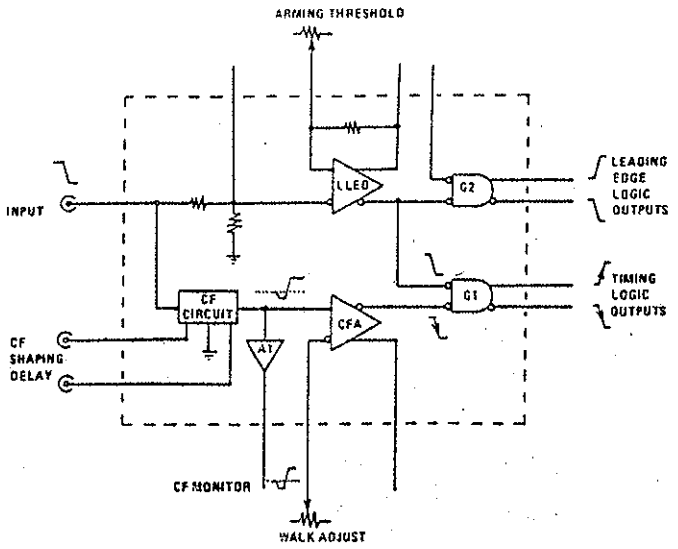

Figure 2. Simplified block diagram of the constant fraction hybrid.

The technique of passively forming the constant fraction bipolar signal has three primary advantages over most active techniques. First, the bipolar pulse is formed without the noise at zero-crossing that is normally introduced by active components. Second, the upper bandwidth limitation of the differential transformer in the pulse-forming network exceeds 350 MHz. Most active methods introduce slewing of the zero-crossing for signals with risetimes containing these frequency components. Third, the dynamic range limitation of the passive pulse shaping network far exceeds that of most active devices.

The passive constant fraction pulse shaping technique has one primary disadvantage compared to active methods. A low frequency limitation is imposed by the differential transformer. Thus, timing applications using this passive shaping circuitry should be limited to input signals with risetimes less than approximately 100 ns. Note, however, that this range of risetimes includes most applications with photomultiplier tubes and with fast solid state detectors.

A four-channel, 100 MHz timing discriminator that incorporates the constant fraction hybrid is described in the succeeding sections. Typical timing and performance data for this instrument are included.

Figure 3 is a simplified block diagram of one channel of the four-channel, 100 MHz constant fraction updating discriminator. The circuit operates as follows. A 0 V to -10 V amplitude input signal starts at time zero and is applied simultaneously to the constant fraction (CF) circuitry and to the leading edge discriminator (LLED) circuitry. The LLED has an adjustable threshold, ranging from -30 mV to -1 V, which determines the minimum input signal amplitude required to produce an output pulse from the instrument. If the input signal exceeds the LLED threshold, that comparator produces an output pulse which arms the zero-crossing gate, G1, at time t_{LE}. The passively formed constant fraction bipolar timing signal is amplified by the constant fraction amplifier, CFA, and crosses the logic threshold at the zero-crossing gate at time t_{CF}. The time t_{CF} is determined by the selection of the external constant fraction shaping delay, $t_{D(Ext)}$, subject to the risetimes and pulse shapes of the input signals.[16,17] A fixed internal delay of 0.6 ns to 0.7 ns must be added to $t_{D(Ext)}$ to obtain the total constant fraction shaping delay

$$t_{D(Tot)} \approx t_{D(Ext)} + 0.65 \text{ ns.}$$

The timing logic signal from gate G1 triggers a fast one-shot, comprised of an ECL type D master-slave flip-flop, FF1, and amplifier A2. This one-shot produces a reshaped logic pulse with a fixed 2 ns width for each signal from gate G1. The reshaped signal drives a hybridized, updating one-shot and output circuit, comprised of a capacitor and amplifiers A3 through A5. Each 2 ns wide signal from FF1 causes A3 to charge the updating capacitor to its maximum amplitude. At the end of the 2 ns interval, the updating capacitor begins to discharge through the series resistor and update width potentiometer toward its quiescent voltage level. Elements A4 and A5 amplify and shape the signal on the updating capacitor to a fast voltage output signal, capable of simultaneously driving three 50Ω loads with negative NIM standard fast logic pulses. The output width of the updating one-shot is continuously variable from less than 6 ns to greater than 150 ns. Each

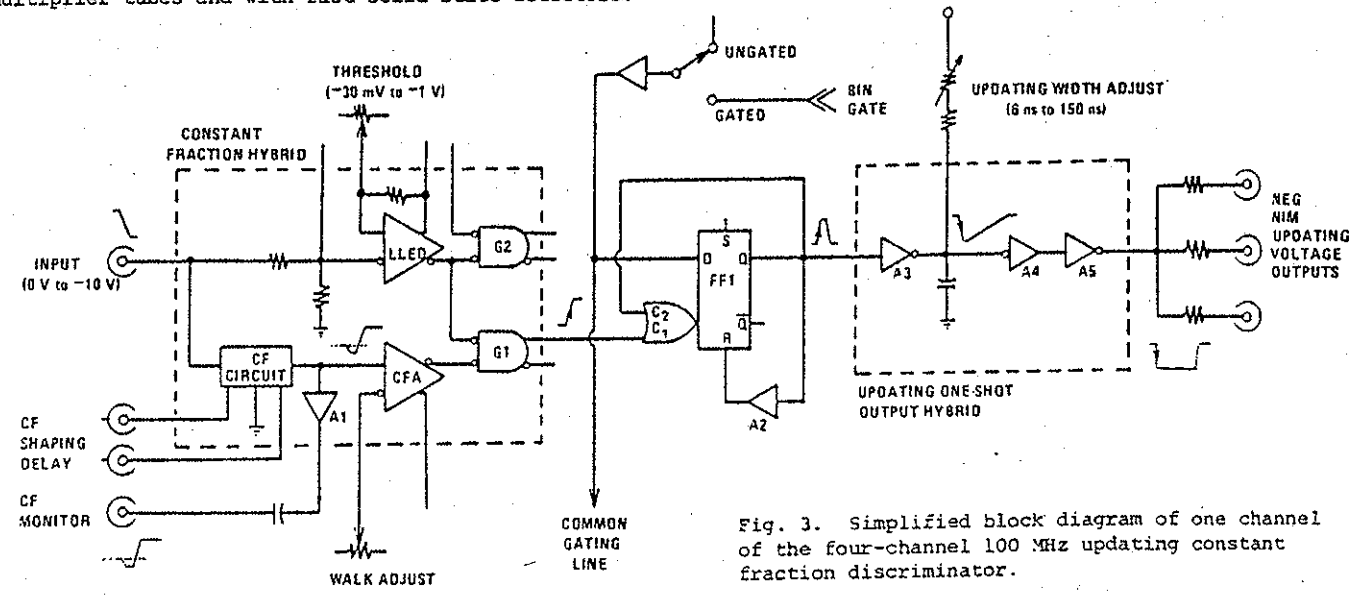

Fig. 3. Simplified block diagram of one channel of the four-channel 100 MHz updating constant fraction discriminator.

reshaped logic signal that occurs at the input of the updating hybrid during the width of an output pulse extends that output pulse by one full, preset updating width.

A common gating circuit can be used to simultaneously enable or inhibit the output responses of all four channels of the discriminator. The position of the Bin Gate switch determines whether gating signals from the bin are accepted or not. Gating control is established at the D input of the ECL type D master-slave flip-flop in each channel.

Experimental Results

The primary usage of the discriminator reported here is expected to be in fast timing or counting experiments with scintillators and photomultiplier tubes (PMTs). In these applications, the anode of the PMT is usually connected directly to the input of the constant fraction discriminator. The anode signals from fast PMTs may contain a wide range of amplitudes, but they usually have a relatively narrow range of risetimes and pulse widths. These signal conditions lend themselves to the use of the true constant fraction (TCF) timing technique.[17] In the TCF method, the constant fraction shaping delay, $t_{D(Tot)}$, is selected so that the zero-crossing of the bipolar timing signal occurs after the attenuated, undelayed portion of the constant fraction signal has reached its maximum amplitude. Thus, the zero-crossing occurs at the same fraction of the input pulse height, regardless of the amplitude of the input signal.[17]

Several four-channel, 100 MHz constant fraction discriminators have been built and tested. The following data represent typical results obtained with these units.

One figure of merit for a constant fraction discriminator is the effective time walk of the constant fraction zero-crossing as a function of input signal amplitude. The results of one time walk test are shown in Fig. 4. This data was obtained using a 10 ns wide input signal, with approximately 1 ns rise and fall times, and a 2.9 ns total constant fraction shaping delay. The discriminator threshold was set at -30 mV, and the walk data was obtained for a 200:1 dynamic range of input signals from -48 mV to -9.6 V. The range of input signal amplitudes and the shaping delay were chosen so that charge sensitivity would introduce minimal additional error in the time walk curve. The time walk shown in Fig. 4 ranged from +30 ps to -95 ps, around the zero walk reference selected at the 10:1 dynamic range point.

Figure 5(a) shows a photograph of the input signal shape used to measure the time walk of the constant fraction discriminator for signals near threshold. This signal is 3.1 ns wide; it has a 10% to 90% risetime of 1.8 ns and a 90% to 10% fall time of 2.0 ns.

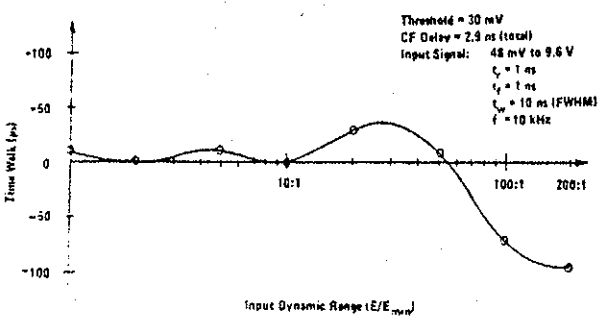

Fig. 4. Time walk of the constant fraction discriminator as a function of input signal dynamic range, for a wide signal significantly over threshold.

The signal shown in Fig. 5(a) is representative of a smoothly rounded, symmetrical signal from a very fast PMT. Figure 5(b) shows a photograph of the CF Monitor signal for the input signal in Fig. 5(a) and for a total constant fraction shaping delay, $t_{D(Tot)} \approx 1.5$ ns.

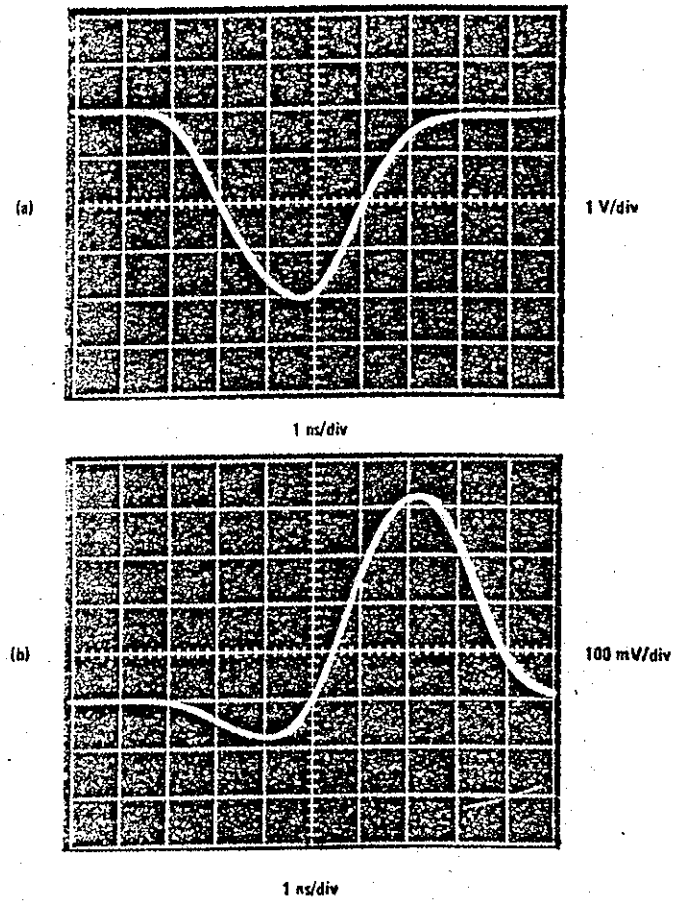

Fig. 5(a) Input signal shape for time walk measurements near threshold. (b) Constant fraction monitor signal for the input signal shown above (CF delay ≈ 1.5 ns total).

Figure 6 is a plot of the time walk of the constant fraction discriminator as a function of input signal amplitude near threshold. The discriminator was set to half-fire for a -40 mV smoothly rounded input signal, such as the pulse shown in Fig. 5(a). The zero walk reference was chosen for an input signal at 100 times threshold. Note that the total time walk shown in Fig. 6 is 480 ps and occurs within the first factor of 10 increase in signal amplitude over the discriminator threshold. This effective time walk can be attributed to charge sensitivity and to leading edge walk near threshold.

A similar time walk test near threshold was performed for a fast, tunnel diode leading edge discriminator.[18] Figure 7 is a plot of the time walk of the leading edge discriminator as a function of input signal amplitude over threshold. The discriminator was set to half-fire for a -45 mV smoothly rounded input signal, such as the pulse shown in Fig. 5(a). The zero walk reference was chosen for an input signal at 100 times threshold. The total time walk of the leading edge discriminator was 4.2 ns. Note that this figure for time walk near threshold is approximately an order of magnitude greater than the time walk for the constant fraction discriminator. The constant fraction unit should provide an even greater improvement in time walk near threshold for slower signals that are similarly shaped.

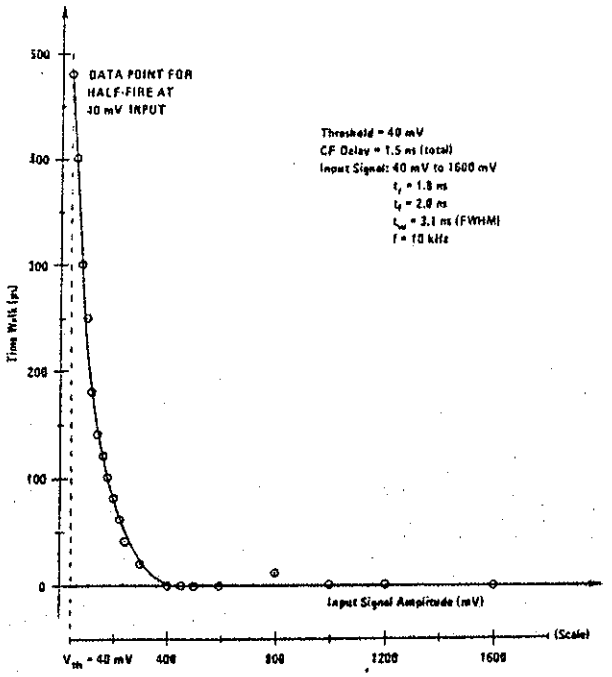

Fig. 6. Time walk of the constant fraction discriminator near threshold for the smoothly rounded signal shape shown in Fig. 5(a).

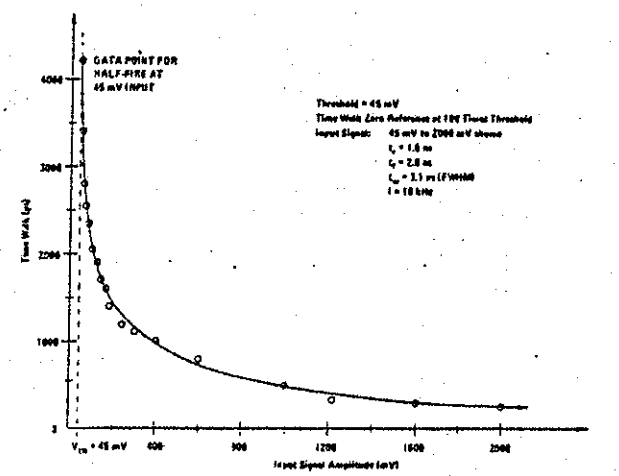

Fig. 7. Time walk of a fast, tunnel diode leading edge discriminator near threshold for the smoothly rounded signal shape shown in Fig. 5(a).

A measure of the charge sensitivity of the constant fraction discriminator can be obtained from Fig. 8. This plot represents the change in the effective threshold level for discriminator half-fire as a function of input pulse width. The data was obtained for a -30 mV discriminator threshold setting and for a total constant fraction shaping delay of 1.5 ns. Input signals were provided at a 10 kHz rate and had approximately 1 ns rise and fall times. The plot in Fig. 8 shows that the effective threshold level is relatively constant for pulse widths greater than 10 ns.

An indication of the pulse pair response capability of the constant fraction discriminator can be obtained from Fig. 9. This plot represents the apparent sensitivity of the discriminator to a second input signal, closely following the first input signal.

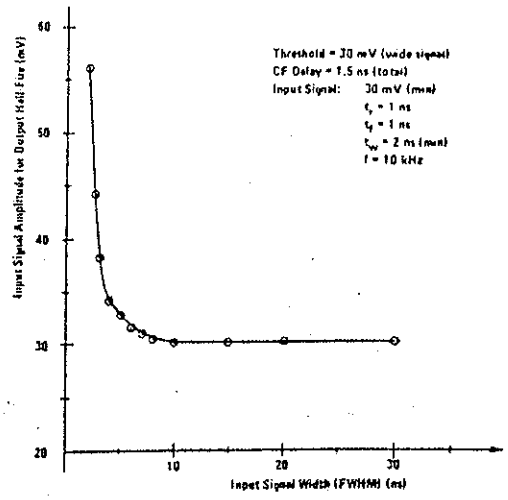

Fig. 8. Threshold sensitivity of the constant fraction discriminator as a function of input signal width.

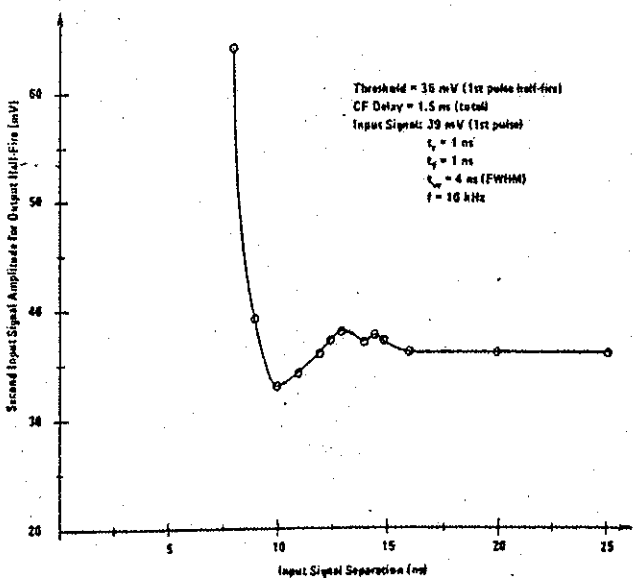

Fig. 9. Second pulse threshold sensitivity of the constant fraction discriminator as a function of input signal separation.

Both the first and second pulses were 4 ns wide (FWHM) and had 1 ns rise and fall times. This signal width approximates a 50% input duty cycle at the minimum expected separation of the leading edges of the input signals. The amplitude of the first pulse was set at 39 mV, or approximately 110% of threshold. For each data point, the second pulse amplitude was varied until the discriminator produced a half-fire for the second output pulse. The plot in Fig. 9 shows a characteristic perturbation for an input pulse leading edge separation of approximately 13 ns. This separation is equal to the propagation delay of the instrument for the selected total shaping delay $t_{D(Tot)} \approx 1.5$ ns. These discriminators typically respond to 4 ns wide input signals with leading edges separated by less than 9 ns.

In Fig. 10 is a set of photographs depicting the response of the constant fraction discriminator to a burst of five pulses less than 10 ns apart. Figure 10(a) shows the five input pulses, each 3 ns in width and 800 mV in amplitude. The (b) photograph in

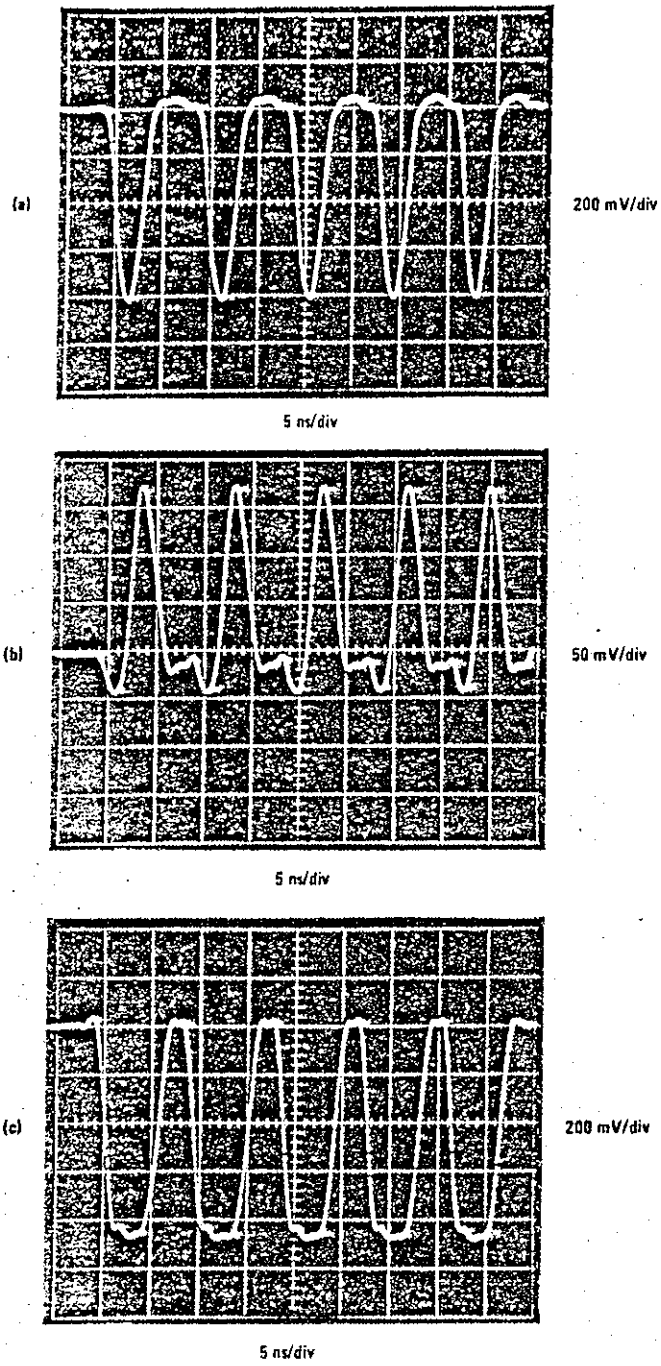

Fig. 10(a) Input signal burst of 5 pulses to the constant fraction discriminator. (b) Constant fraction zero-crossing monitor signal for the burst input. (c) Constant fraction discriminator output burst response. (CF delay ≈ 1.5 ns; threshold = 30 mV.)

the figure shows the burst response at the CF Monitor. Figure 10(c) depicts the discriminator output response.

Many timing experiments involve relatively low count rates and require long runs to accumulate sufficient data. Such experiments require exceptional temperature stability from the timing discriminators. Figure 11 shows plots of changes in propagation delay as a function of temperature for four channels of the 100 MHz discriminator, each set for a different updating output width. Note that the change in propagation delay for each channel is less than 10 ps/°C for

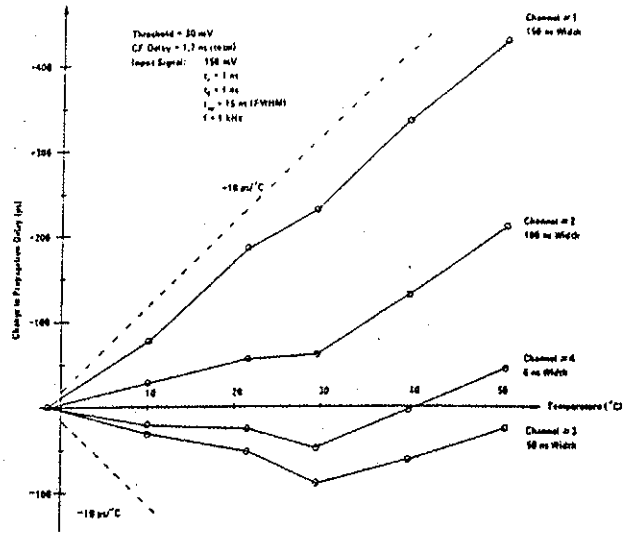

Fig. 11. Change in the propagation delay of the constant fraction discriminator as a function of temperature for four output width settings.

the range of temperatures from 0°C to 50°C. The updating output pulse widths are specified to change less than 0.2%/°C over the same range of temperatures.

The constant fraction discriminator described in this paper was also tested in a gamma-gamma timing coincidence experiment, using 1" x 1" KL236 plastic scintillators and PMTs. Figure 12(a) is a photograph of the anode signal from the RCA 8850 PMT used in the experiment. The constant fraction shaping delay for the discriminator used with this tube was selected using the criteria described earlier in this paper. Figure 12(b) and Figure 12(c) are photographs of the corresponding delayed CF Monitor signal, as seen on a sampling oscilloscope triggered by the discriminator output signal. The time spread in the zero-crossing region in these photographs is less than 100 ps. A typical gamma-gamma timing coincidence system is shown in Fig. 13. Timing resolution data was accumulated for this system using two adjacent channels of the 100 MHz constant fraction discriminator. The resulting timing resolution as a function of dynamic range is shown in Fig. 14. The FWHM timing resolution varies from 193 ps for a 1.1:1 dynamic range of signals to 333 ps for a 100:1 dynamic range of signals. The upper energy limit used in this experiment was 1.6 MeV, corresponding to anode pulses approximately 4 V in amplitude.

Conclusions

The four-channel constant fraction updating discriminator described in this paper has several important features. The discriminator uses a passive means for shaping the constant fraction signal. This technique results in excellent time walk characteristics. The instrument contains four discriminators and is capable of count rates in excess of 100 MHz. The intent in designing these features into the instrument is to extend the high resolution constant fraction timing technique to applications in high energy physics. The exceptional temperature stability of the unit also allows it to be used in long-term timing exerpiments.

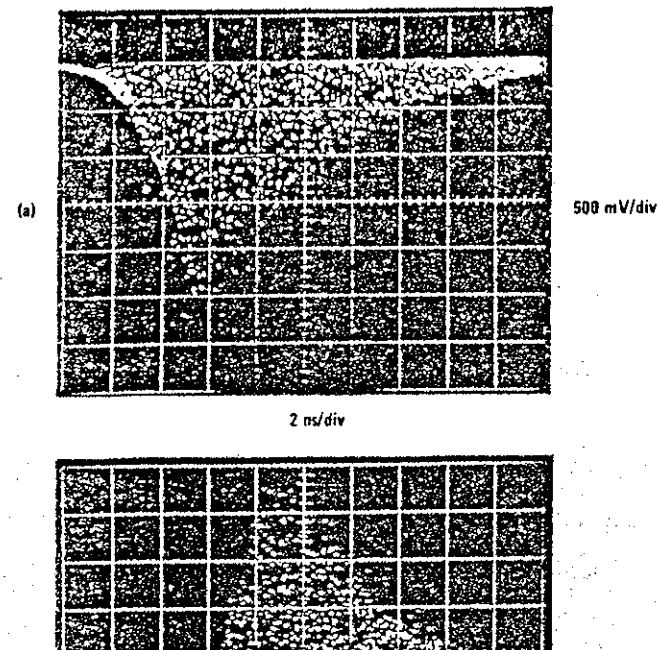

Fig. 12(a) RCA 8850 PMT anode signal with a 1" x 1" KL236 scintillator and ^{60}Co. (b) Constant fraction zero-crossing monitor signal, triggered by the discriminator output for the anode signal shown above. (c) Expanded view of the constant fraction zero-crossing monitor signal. (CF delay = 3 ns; threshold = 30 mV.)

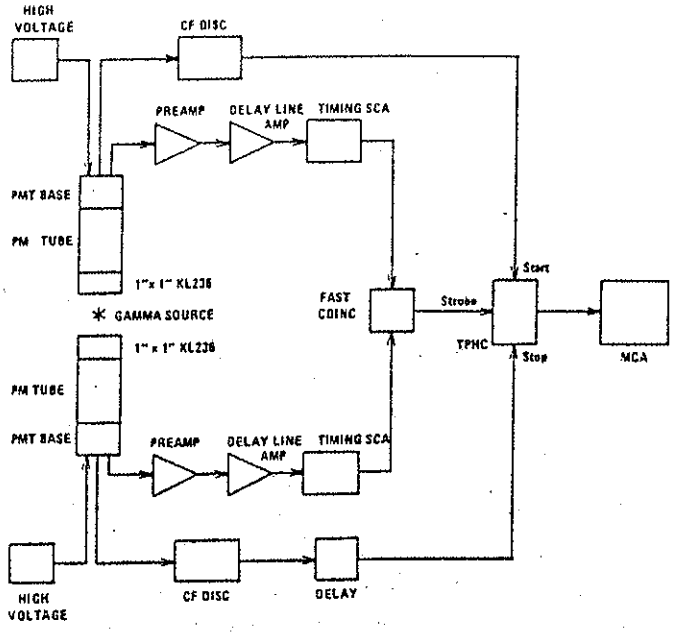

Fig. 13. Typical system for gamma-gamma coincidence measurements with scintillators and photomultiplier tubes.

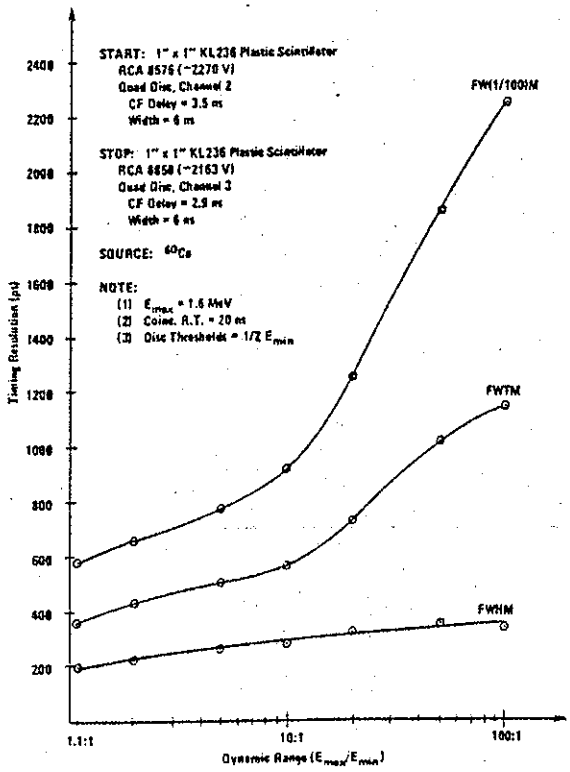

Fig. 14. Timing resolution as a function of dynamic range for two channels of the four-channel constant fraction discriminator operating in a fast-slow coincidence system.

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