EG&G ORTEC

AD811
CAMAC
Octal ADC

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CAMAC
Octal ADC

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"Rev 17" on rear panel

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No Manual Change

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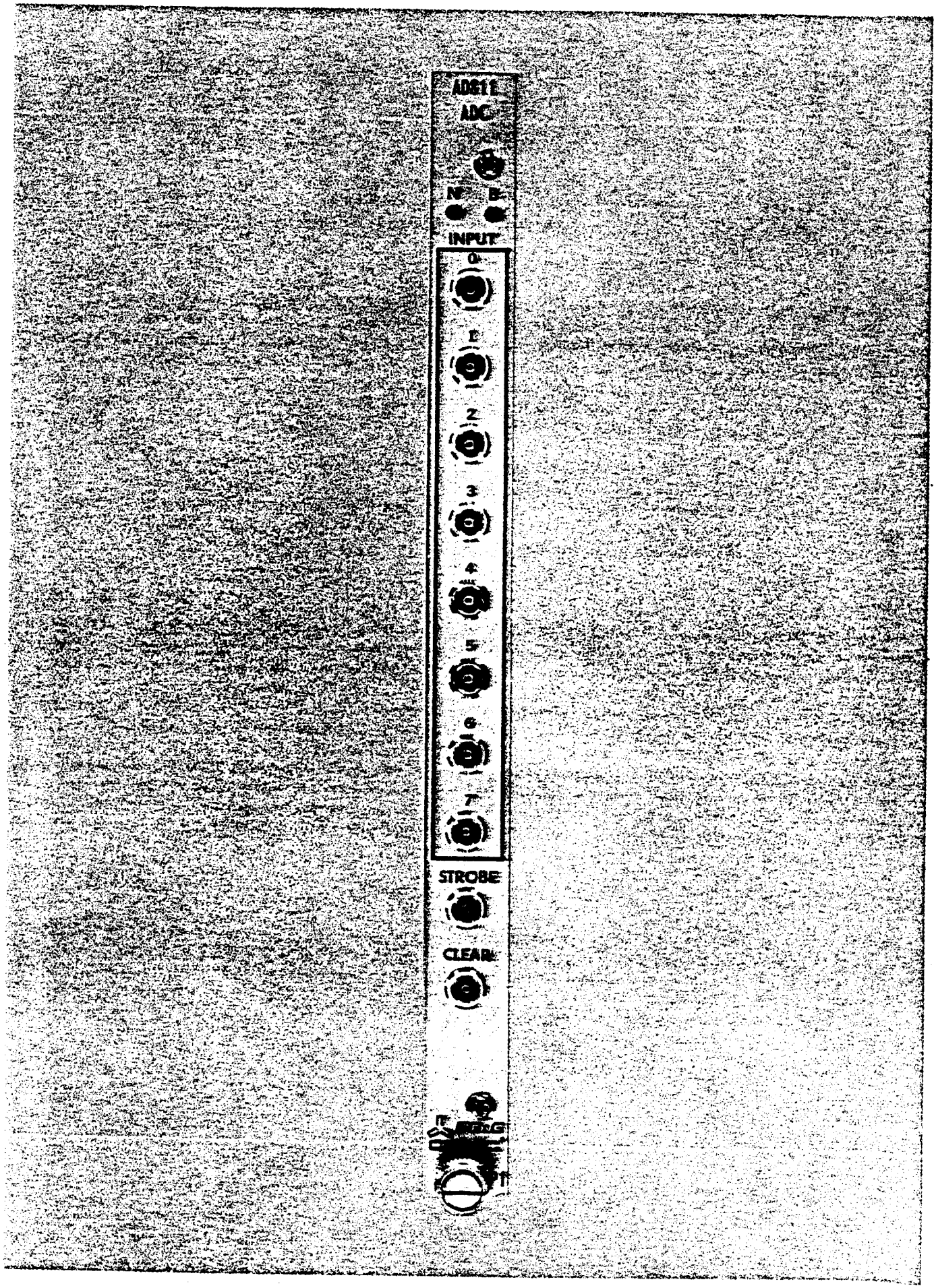
ADC11
ADC
INPUT
0
1
2
3
4
5
6
7
STROBE
CLEAR

AD811 CAMAC Octal ADC Manual

1. DESCRIPTION

The AD811 Octal ADC contains eight peak-measuring analog-to-digital converters packaged in a single-width CAMAC module. The instrument is designed to measure positive unipolar or bipolar signals from nuclear shaping amplifiers in the range of 0 to +2 V. However, the circuit is completely dc-coupled and can be used for sampling dc or slowly changing voltages, allowing a wide range of applications.

The AD811 provides 1 mV resolution with a range of 11 bits (2047 counts) and a 12th bit is included in each of the eight data registers for overflow detection. The input linear gates and peak detectors are normally closed and the unit must be triggered by an external strobe pulse to start a conversion.

The strobe input pulse starts an internal gate width circuit that enables all eight linear gates and their peak detectors. The duration of the gate width is adjustable from 50 through 350 ns with an internal control and can be set to overlap the peaks of the inputs for correct operation. The instrument has an excellent linearity and stability and is highly immune to crosstalk and power supply noise effects.

At the end of the gate interval, a conversion process starts and proceeds in parallel for all eight sections. The conversion lasts for approximately 80 μs, independent of the input signal amplitude. At any time during this 80 μs digitizing interval the conversion can be aborted by application of a signal to the front panel Clear input and the unit will be fully restored to its quiescent state within 0.5 μs and be ready to accept another strobe.

At the completion of a normal conversion a LAM service request is generated and all accumulated data are held until they are reset from the Dataway control circuits. The busy and/or LAM status can be controlled at the module level by CAMAC commands in accordance with recommended practice.

Automatic testing and calibration checking of the module is accomplished by issuing the CAMAC command F25. An internal reference voltage is supplied to all eight converters and triggers a conversion. The reference voltage is sufficient to ensure overflow of all eight scaler-registers and a comparison of their measurements serves as a calibration check. This tests the analog circuits and the digital registers fully. A LAM service request is generated at the end of the conversion interval.

Two front panel indicators are included to monitor the status of the module. An "N" indicator shows when the AD811 is being addressed and remains lighted for one full second to ensure that it can be observed by the operator. A "B" indicator shows when the module is in a blocked condition and cannot accept a strobe to start a conversion. The blocked condition can be generated by either the internal busy latch or by a Dataway inhibit signal.

2. SPECIFICATIONS

2.1. INPUTS

Input 0 to 7 One input per channel accepts positive unipolar or bipolar signals with >50 ns width in the positive lobe. Range 0 to >+2 V, peak measuring; protected to ±5 V dc or ±100 V transient; Z_{in} 1K, dc-coupled.

Strobe Accepts NIM-standard negative fast logic signal with >5 ns duration to initiate conversion. The leading edge must precede the peak of the data signal by at least 80 ns and the internal gate width must be adjusted to overlap the data signal peak. Protected to ±5 V dc; Z_{in} 50Ω, dc-coupled.

Clear Accepts NIM-standard negative fast logic signal with >5 ns duration to abort a conversion and reset the logic and the scaler-registers. Must occur within 80 μs after the trailing edge of the internally adjusted gate width for correct operation. Resets to ≤0.1% of full scale within 0.5 μs. Protected to ±5 V dc; Z_{in} 50Ω, dc-coupled.

2.2. OUTPUTS

Data 11 bits per section available on R1 to R11 Dataway lines.

Overflow 1 bit per section (latching) available on R12 Dataway line.

LAM Dataway LAM is set at the end of conversion; may be enabled/disabled and status-tested by CAMAC commands.

2.3. CONTROLS AND INDICATORS

Gate Width An internal potentiometer controls the width of the gating signal, common to all eight sections, from 50 to 350 ns. The strobe input leading edge should precede the data input peaks by at least 80 ns, and the gate width control should be set to overlap the peaks for correct operation.

Calibrate One internal potentiometer for each of the eight sections sets the calibration (slope) individually for its section.

Offset One internal potentiometer for each of the eight sections adjusts a pedestal to correct the zero intercept individually for its section.

Enable/Disable I An internal jumper-selectable Dataway Inhibit circuit.

B Indicator lights when unit is in a blocked condition.

N Indicator lights for 1 second when the unit is being addressed.

2.4. PERFORMANCE

Mod. 0 to 10V 4096
Range 0 to >+2 V, peak measuring, into 2047 channels plus overflow.
Mod. 2.5 mV
Resolution 1.0 mV referred to input.

Channel Width 1.0 mV/channel, 60% flat top profile.

Integral Nonlinearity ≤±0.05%, 1% to 100% of full scale.

Differential Nonlinearity ≤2%, 5% to 100% of full scale.

Conversion Time Fixed at 80 μs for all sections in parallel.

Crosstalk A 5 V signal with rise time ≥50 ns will not affect any adjacent section by more than one channel.

Temperature Coefficient ≤±0.025%/°C (0° to 50°C).

2.5. CAMAC CODES

F(0)·A(k) (k = 0 to 7) read selected register.

F(2)·A(k) (k = 0 to 6) read selected register.

F(2)·A(7) Read register 7; clear all registers, busy, and LAM.

F(8)·A(12) Test LAM; LAM = Q.

F(10)·A(12) Clear LAM.

F(11)·A(12) Clear all registers, busy, and LAM.

F(24)·A(12) Disable LAM.

F(25)·A(k) (k = 0 to 7) test all registers. Measures a reference voltage in all sections that generates an overflow.

F(26)·A(12) Enable LAM.

F(27)·A(12) Test busy; busy = Q.

C Clears all data registers, busy, and LAM status.

Z Clears all data registers, busy, and LAM status, and disables LAM.

I Inhibits operation of all sections (if accepted by jumper setting).

Q Returned for all F·A function codes except F(8)·A(12) and F(27)·A(12) where the Q response is conditional.

X Returned for all F·A function codes.

2.6. POWER REQUIRED

Maximum +6 V, 550 mA; −6 V, 250 mA; +24 V, 95 mA; −24 V, 8 mA.

3. OPERATION

3.1. INSPECTION AND INSTALLATION

After carefully unpacking the unit, thoroughly inspect it for evidence of damage in shipment. If it has been damaged, refer to the Warranty in the front of this manual for further instructions.

CAUTIONS

> Always ensure that CAMAC crate power is turned off before installing or removing any CAMAC module.
>
> Always ensure that all pins on the CAMAC Dataway connector on the rear panel are clean before installing any CAMAC module in its crate.
>
> Never use excessive force in installing or removing any CAMAC module.

3.2. SIGNAL CONNECTION AND APPLICATION OF POWER

Note: 50Ω coaxial signal leads with LEMO connectors (male) are required for front panel connections to this unit.

Connect a signal lead to each input that is to be used. These are marked Input 0 through Input 7 for the eight channels. Either pulses or dc levels can be furnished for measurements.

Connect a signal lead to the strobe input on the front panel. A signal is required through this input to initiate a measurement cycle.

The use of the clear input on the front panel is optional. If it is used, a signal through this connector after the effective gate interval will cancel the measurement and reset the logic and scalers to permit a new measurement to be initiated. The clear input is blocked after the 80 μs conversion period.

Turn on the CAMAC crate power. The unit should now be ready for operation.

3.3. SIGNAL CONNECTIONS

Table 3.1. summarizes the signal connections and their functions.

Table 3.1. Signal Connections.

Connector	Function
Input 0	Accepts signal level or pulses to +2 V for amplitude measurements in section 0.
Input 1	Accepts signal level or pulses to +2 V for amplitude measurements in section 1.

Table 3.1. (continued)

Connector	Function
Input 2	Accepts signal level or pulses to +2 V for amplitude measurements in section 2.
Input 3	Accepts signal level or pulses to +2 V for amplitude measurements in section 3.
Input 4	Accepts signal level or pulses to +2 V for amplitude measurements in section 4.
Input 5	Accepts signal level or pulses to +2 V for amplitude measurements in section 5.
Input 6	Accepts signal level or pulses to +2 V for amplitude measurements in section 6.
Input 7	Accepts signal level or pulses to +2 V for amplitude measurements in section 7.
Strobe	Accepts NIM-standard fast negative logic signal to initiate a measurement cycle in all sections.
Clear	Accepts NIM-standard fast negative logic signal to cancel the measurement and reset the unit within 500 ns; effective only after a gate interval is complete and before LAM is set.

4. FUNCTIONAL DESCRIPTION

Refer to Figs. 4.1 through 4.3 and schematics AD811-0101-S1 and AD811-0101-S2, included at the back of the manual. For identification of individual portions of multielement integrated circuits, an output terminal number can be used to specify a selected portion. For example, IC802(3) identifies the portion of IC802 that uses pin 3 for its output.

4.1. GENERAL FUNCTION

The intended function of the AD811 is to accept a strobe input pulse to generate a gate interval, to identify and stretch the peak amplitude of a signal input during the gate interval in each of its eight signal input circuits, and to then digitize the stretched peak amplitude in each section. Any or all of its eight sections, or channels, can be used as required by the experimental application. Any unused channel(s) can be disregarded and left with no connection.

When it receives a strobe input, the AD811 enables all eight input gates and permits each peak measuring circuit to stretch the peak amplitude of its input on a charge capacitor. At the trailing edge of the gate interval, adjusted internally in the range of 50 to 350 ns or extended by the duration of the strobe input signal, the charged capacitor is discharged with a constant current. During the discharge interval, clock pulses from a 26 MHz oscillator are gated to a scaler-register. The oscillator is common to all channels, while the clock gating intervals are unique to each channel.

When the measurement is complete, the oscillator is turned off and a LAM status indication is furnished to the CAMAC system to indicate that data are available from the scaler-registers for one or more of the eight channels. Once LAM has been set, the data and the LAM status will not be changed except by command from the CAMAC Dataway.

An upper limiter in the common control circuit determines the maximum amplitude that can be applied through any of the eight input signal circuits. It is set at about +2.25 V and cuts off any excess amplitude that may be furnished from the source that is being measured. The +2.25 V level is sufficient to ensure an overflow of the scaler when the measurement is made, and this is then indicated in the readout by a true signal from R12. The test program, using F25, applies the common upper limiter level to all eight sections and triggers a measurement of that level; this tests the entire counting capacity of all scalers (with overflow) and permits a comparison of the calibration adjustments in the individual sections since the same voltage is being measured in all sections.

An 80 μs timer enables the conversion interval. It operates at the trailing edge of the gate width signal and enables the normal rate rundown of the charge capacitor. A clock delay of about 400 ns is triggered at the leading edge of the 80 μs timer to permit the constant current discharge rate to stabilize; then the 26 MHz oscillator is enabled through the rest of the 80 μs timer interval. The 26 MHz oscillator pulses are fanned out to all eight sections.

A scaler gate in each section is enabled during the rundown of its charge capacitor and thus allows the peak input amplitude to be digitized in its scaler. The range and calibration are adjusted for a nominal +2 V equal to about 2000 counts in the scaler, or 1 mV/count. The slope and zero intercept for this relationship are both adjustable with potentiometers on the printed circuit for each section individually.

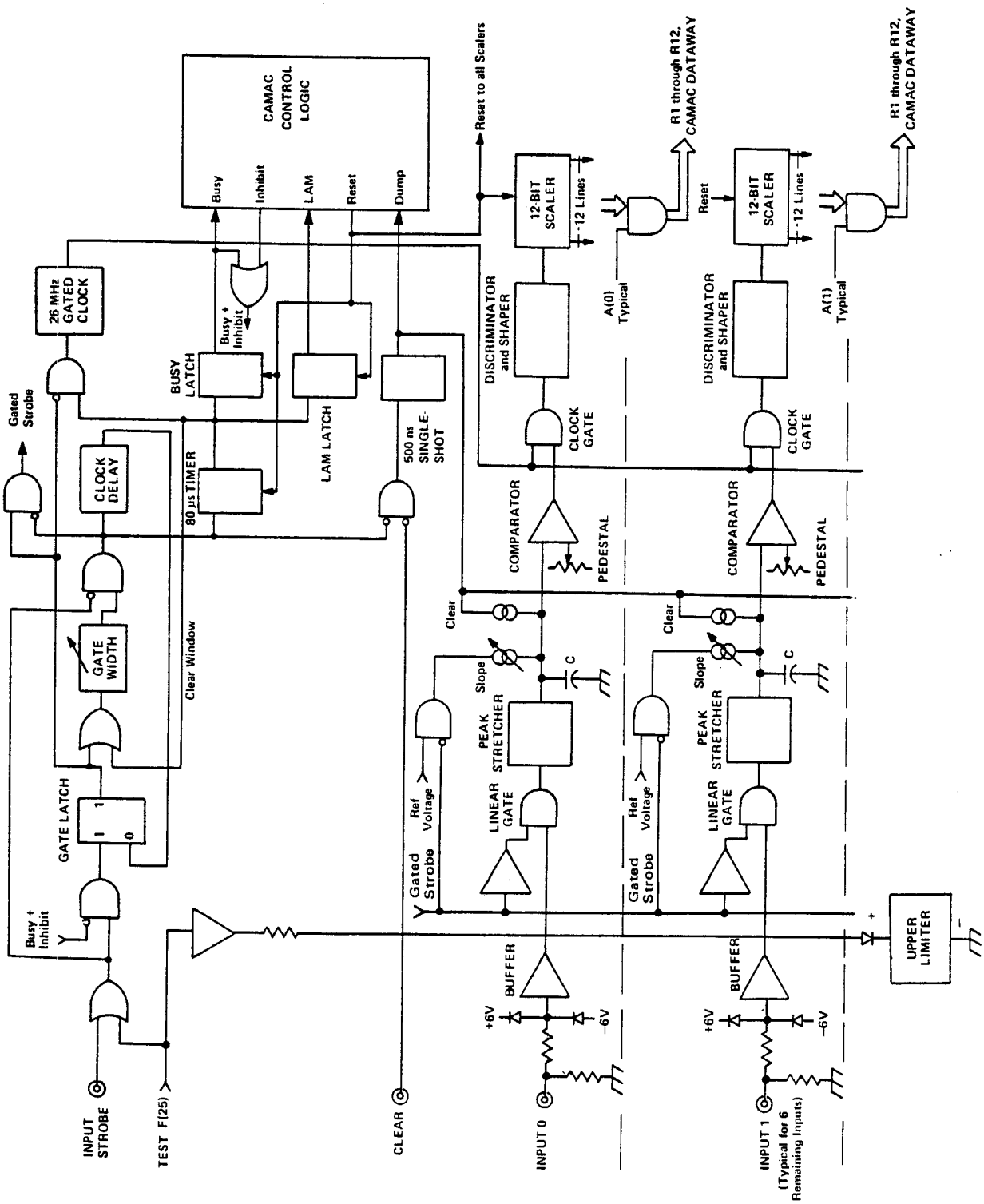

Fig. 4.1. Functional Block Diagram for AD811 Analog Section.

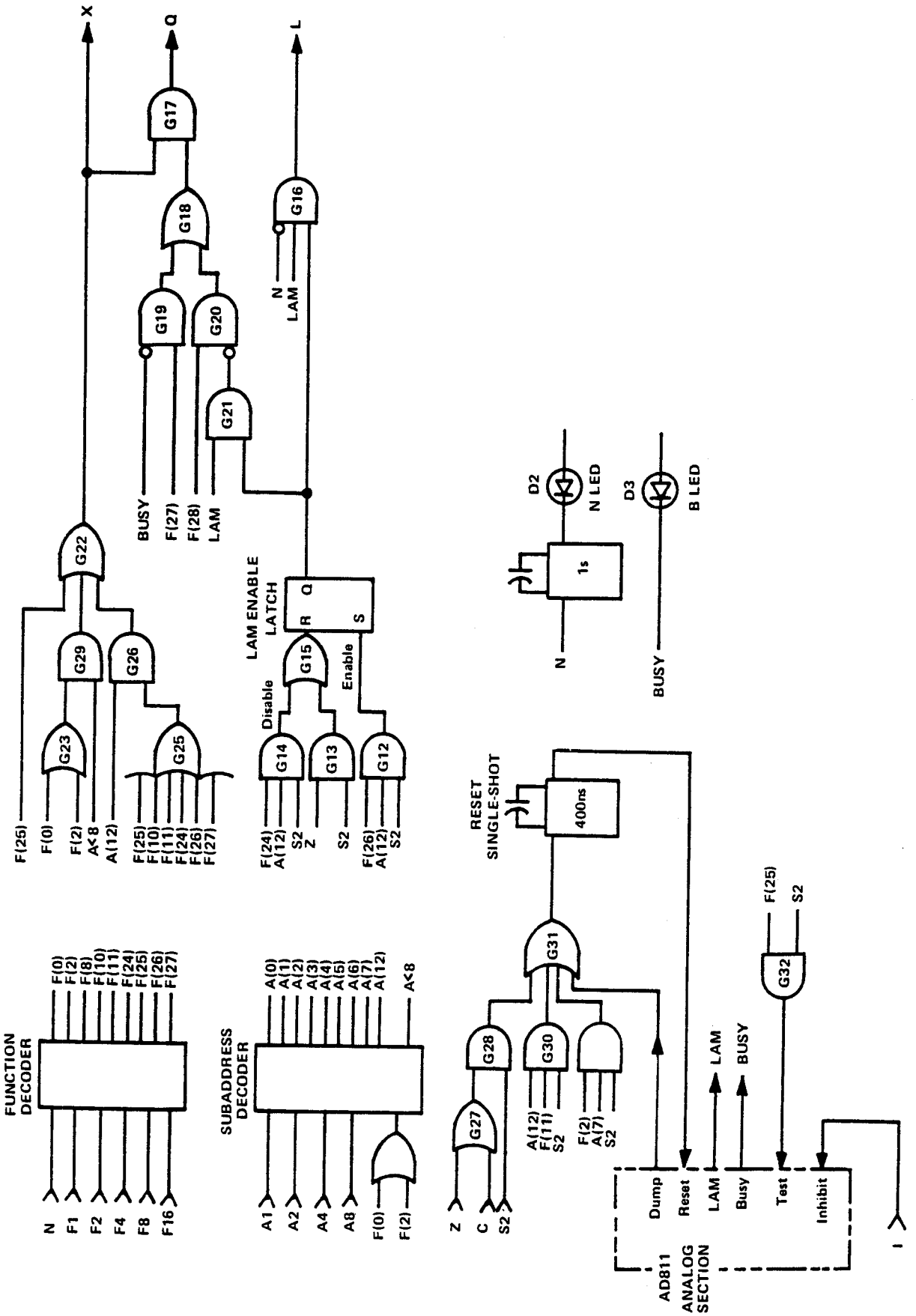

Fig. 4.2. Block Diagram, AD811 CAMAC Logic.

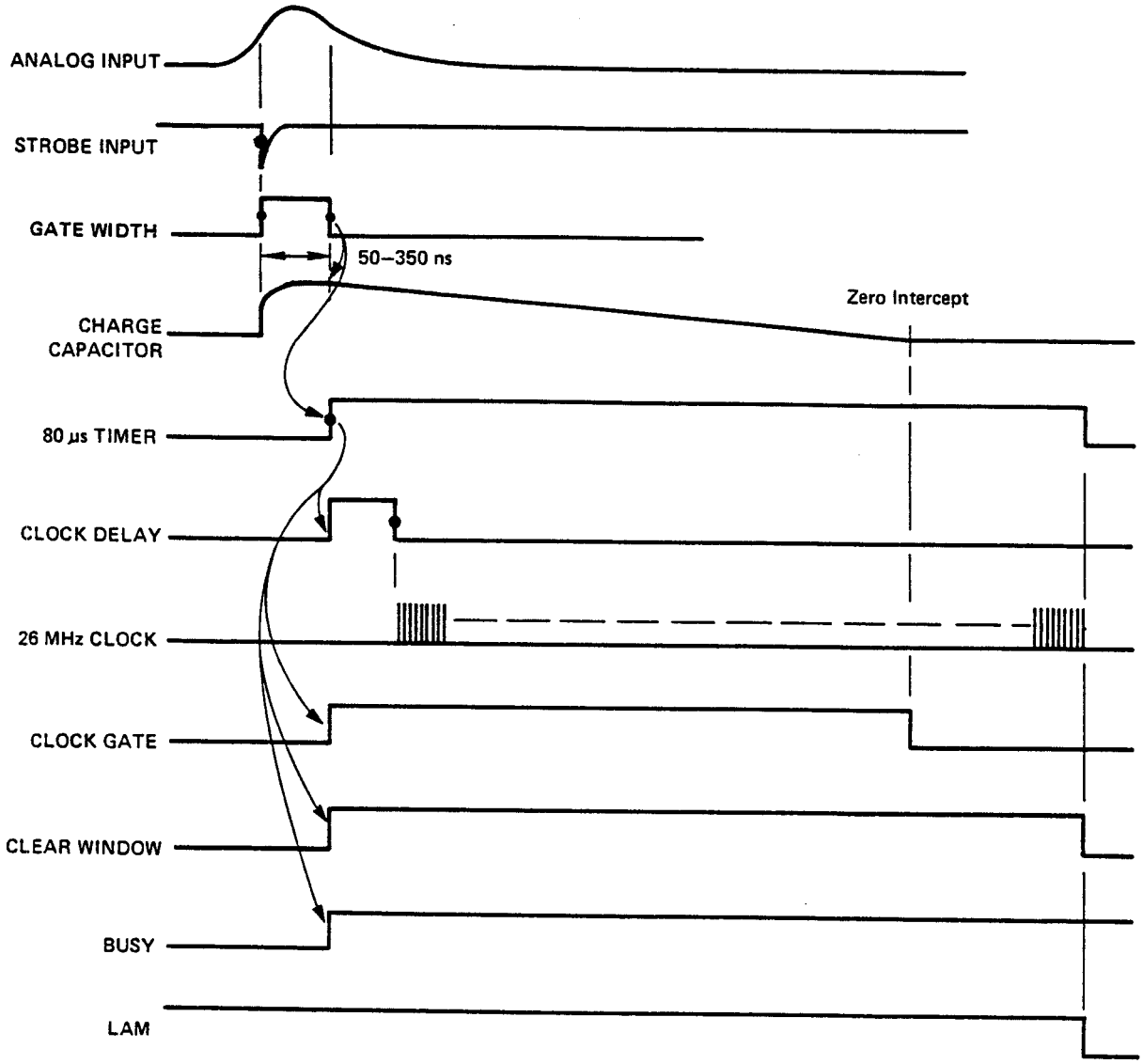

Fig. 4.3. AD811 Timing Diagram.

During the 80 μs timed conversion interval, the circuit that can accept a clear input signal is enabled. If a clear signal is furnished during this time window, the conversion is aborted, the scalers are reset, the charged capacitors are all run down at a fast discharge rate, and the logic is reset so that a new strobe can be accepted to start a measurement cycle. All of the clear functions take place within a 500 ns interval that starts at the leading edge of the clear input signal. A clear input cannot be accepted before or after this time window.

If the conversion is allowed to proceed to completion, indicated by timeout of the 80 μs timer, LAM is generated to indicate to the Dataway that data are available in one or more of the scalers. When LAM is set, no further operation is permitted in the AD811 until a reset is furnished from the CAMAC system.

A busy status is generated at the start of the conversion time and continues until CAMAC reset unless aborted by the clear input. Busy inhibits the signal inputs and the strobe input to prevent response to any additional information after conversion is initiated. Both the busy and the LAM status can be tested by the CAMAC system.

Either of two conditions generates a block condition and lights the B indicator on the front panel. These conditions are the presence of a busy status or an inhibit input from the Dataway I line. An internal jumper can be set to either accept or ignore the Dataway I line signal.

Most commands from the crate controller will include a signal on the Dataway N line to identify the location of the AD811 in the crate, a function code such as F(0) or F(24), a subaddress code such as A(0) or A(12), and an S2 strobe. The N( ), F( ), and A( ) portions are not required for I (inhibit), Z (initialize), or C (clear) codes.

Whenever the module is addressed by N(*k*) from the crate controller, where *k* is the crate station location (1 through 23), the front panel N LED lights and an L status is inhibited from generating an L output signal to the Dataway until the N is removed. While N is present, the function code decoder is enabled in this module only; this is the method that is used to select the module according to its station location number. The N signal triggers a 1 second monostable that lights the front panel indicator long enough to ensure that it can be monitored visually.

Any input command except Z or C generates an X response and, except for F(8)·A(12) or F(27)·A(12) it will also generate a Q response. For an F(8)·A(12) command, Q = the internal L status unless the LAM Enable latch is disabled. For an F(27)·A(12) command, Q = the internal busy status.

4.2. LOOK-AT-ME SIGNAL

A LAM enable latch, IC1F(10) and (13), must be enabled so that an internal L signal can be generated. The latch is enabled by code N( )·F(26)·A(12)·S(2) from the Dataway. It is disabled by Z·S(2) or by N( )·F(24)·A(12)·S(2).

If the latch has been set, a LAM status signal will be set 80 μs after the gate width interval unless a clear signal has been furnished during that 80 μs conversion time.

4.3. BUSY STATUS

A busy status is established at the start of the 80 μs conversion time. The busy condition inhibits the strobe input circuit from accepting any further signals to initiate a measurement until the module has been reset. At the end of the gate width interval, a signal through Q822 triggers IC2G(9) to set busy latch IC2H(6). The busy latch can be reset by either of two conditions; dump, due to a clear input signal within the conversion time, or a reset code from the Dataway. The condition of the busy latch can be tested by N( )·F(27)·A(12)·S(2) from the Dataway; at the test time, Q = busy or $\overline{Q}$ = not busy.

4.4. AMPLITUDE CONVERTERS

The circuit for each of the eight amplitude converters is outlined in schematic AD811-0101-S1, across the top of the drawing. The complete circuit is shown for the Input 0 channel, in which all components except for the output clock gate and the discriminator and shaper use reference designations in the 000 through 099 series. The equivalent components in each of the other sections use reference designators that reflect the section number, 1 through 7, as the most significant digit. The following discussion uses the reference designators shown for section 0, and each of the other sections operates identically.

Either pulses or a dc level can be furnished through the Input connector and through buffer Q001. Linear gate Q003 is normally conducting and shorts the input signal to ground. A gated strobe signal, furnished through the gate width interval, is furnished through Q813 to cut off Q003 and to gate the input signal into peak stretcher Q004 through Q007, but the signal is inhibited from rising above about +2.25 V by the level generated in Q819 and furnished through Q002.

Capacitor C002 is charged to the peak amplitude that is furnished through the input circuit during the gate interval. At the end of the gate width interval, when the 80 μs timer starts the 26 MHz clock, the capacitor is discharged through Q009, R037, and R017 to a reference level that is furnished through D813. A comparator, Q006 through Q013, senses the discharge interval and enables clock gate IC804(6) during the discharge time. The reference level for the comparator is furnished from R031.

During the time when IC804(6) is enabled, the clock pulses that are furnished from the 26 MHz oscillator through the clock fanout at IC804(3) are shaped by Q014 and counted in the 12 bit scaler for section 0.

Through the time interval during which storage capacitor C002 is being discharged and after the clock delay, the 26 MHz oscillator pulses are gated to the scaler. Since this interval is proportional to the peak amplitude that was stored on the capacitor, the number of counts in the scaler after the conversion is a digitized measurement of the amplitude.

If a clear input signal is furnished prior to the end of the 80 μs conversion time, a dump signal is generated that provides a quick discharge of C002 through Q008 and generates an internal reset in IC2G(6) that aborts the 80 μs timer, resets the busy latch, and resets the scaler circuits. The LAM latch, IC2H(9) is held in reset and does not respond to the reset of the 80 μs timer.

4.5. SCALER/REGISTER CIRCUITS

Each of the eight 12 bit scalers counts the burst of oscillator pulses that are furnished from the clock gate. For each channel that measures about 2 V or less, the number of clock pulses will not overflow the 11 bit valid scaler capacity. If the input voltage exceeds +2 V (actually +2.047 V if the calibration is accurate), the 11 bit capacity overflows and sets bit 12 to indicate that the measurement is not valid.

The scaler for section 0 includes IC5A, IC4A, and IC3B(9). The accumulated count is held in the scaler until a reset occurs. The 12 bit identifications are furnished to gates IC5B, IC4B, and IC3A. At N( )·F(0 + 2)·A(0)·S(2) the A0 strobe is furnished to the gates and the 12 bits are furnished through the Dataway R1 through R12 lines.

Each of the other seven scalers operates in exactly the same manner as that described for section 0. The equivalent components are indicated on schematic AD811-0101-S1, in the upper right portion of the drawing.

4.6. FUNCTION CODE DECODER

The function code decoder is IC2B. It is enabled by N( )·F(4) and can generate codes F(0), F(2), F(8), F(10), F(11), F(24), F(25), F(26), and F(27) from signals through the CAMAC F lines. These codes are all listed in Section 2, Specifications.

4.7. FUNCTION CODE F(0)

F(0) will be provided together with A(0) through A(7). The F(0) code commands read from the scaler/register that is designated by the A( ) subaddress code.

4.8. FUNCTION CODE F(2)

F(2) commands read only when it is furnished with A(0) through A(6), the same as for F(0) above. When F(2) is combined with A(7), it commands read of scaler/register 7 and then, at S2 time, clears all registers, busy, and LAM.

4.9. FUNCTION CODE F(8)

F(8) operates with A(12) to test the internal LAM status. The test is applied to the LAM status signal following the LAM enable latch function. It is derived from IC1G(4) and the Q output is equal to the LAM status at S2 time.

4.10. FUNCTION CODE F(10)

F(10) operates with A(12) to reset LAM latch IC2H(9) at S2 time. No other condition in the AD811 is affected by this code, and it is not operative during conversion because the LAM latch is not set until the end of the 80 μs conversion time.

4.11. FUNCTION CODE F(11)

F(11) operates with A(12) to provide a general reset at S2 time. Reset is furnished to all eight scaler/registers and to both the busy and LAM status latches.

4.12. FUNCTION CODE F(24)

F(24) operates with A(12) to selectively disable LAM enable latch IC1F(10) and (13). When this latch is disabled, it inhibits gating for the LAM status indication at the end of conversion, so the L output signal can neither be tested nor furnished through the Dataway N line.

4.13. FUNCTION CODE F(25)

F(25) operates with any subaddress, A0 through A7, at S2 time to test all eight channels simultaneously. The test command is furnished as a trigger through Q803 to the input buffers and the measurement cycle is initiated to digitize the (approximately) +2.25 V upper limiter level in all sections. The test level is sufficiently high to ensure that all sections will overflow and will thus check the response of all stages in each scaler as well as the conversion logic of each section.

4.14. FUNCTION CODE F(26)

An F(26)·A(12) code selectively enables LAM enable latch IC1F(10) and (13). After the latch has been enabled, it permits the LAM status to be both tested and furnished through Dataway L line.

4.15. FUNCTION CODE F(27)

F(27) operates with A(12) to test the status of busy latch IC2H(6). The Dataway Q signal is equal to the busy status at S2 time.

4.16. CODE Z·S2

Z·S2 is not dependent upon an N code and is the general signal to initialize all modules in the crate. In the AD811 it clears all eight scaler/registers to zero, clears the LAM and Busy status latches, and disables LAM enable latch IC1F(10) and (13). After this signal has been used, an N( )·F(26)·A(12)·S2 signal must be used to again enable the latch before any L signals can be tested or furnished.

4.17. CODE C·S2

C·S2 is not dependent upon an N code and is the general signal to clear all modules in the crate. In the AD811 it clears all eight scaler/registers to zero and clears the busy and LAM status latches. It does not affect the LAM enable latch.

4.18. SUPPLEMENTARY DATAWAY INFORMATION

The relative timing of signals in a Dataway operation is shown in Fig. 4.4 and Tables 4.1 through 4.4 are provided as an aid for using a CAMAC system. These tables show standard Dataway usage, connector pin assignments at both "normal" and "control" stations, and the function codes. The control station is always the highest numbered station location in the crate. In a 25 station crate, this is station 25 and stations 1 through 24 are all normal stations. Since a type A crate controller must occupy the control station and at least one adjacent normal station, the AD811 must be assigned a location within the group from 1 through 23. Its station location is its N( ) identification for selection of any code that includes an F( ) function code.

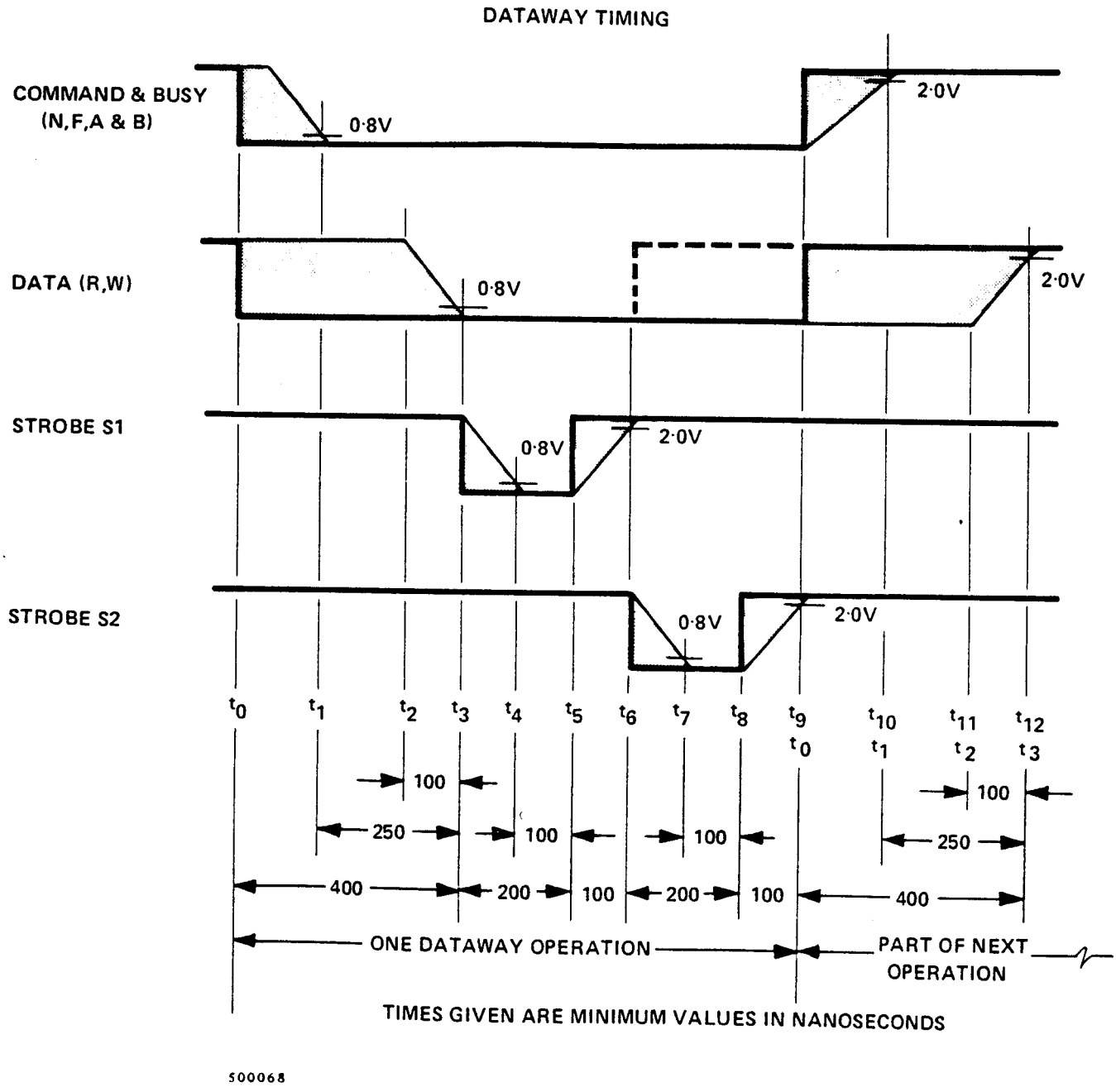

Fig. 4.4. Timing of a Dataway Operation (Fig. 9 of TID-25875).

Table 4.1. Standard Dataway Usage (Table 1 of TID-25875).

Title	Designation	Contacts	Use at Module
Command			
Station Number	N	1	Selects the module (Individual line from control station).
Sub-Address	A1,2,4,8	4	Selects a section of the module.
Function	F1,2,4,8,16	5	Defines the function to be performed in the module.
Timing			
Strobe 1	S1	1	Controls first phase of operation (Dataway signals must not change).
Strobe 2	S2	1	Controls second phase (Dataway signals may change).
Data			
Write	W1–W24	24	Bring information to the module.
Read	R1–R24	24	Take information from the module.
Status			
Look-at-Me	L	1	Indicates request for service (Individual line to control station).
Busy	3	1	Indicates that a Dataway operation is in progress.
Response	Q	1	Indicates status of feature selected by command.
Command Accepted	X	1	Indicates that module is able to perform action required by the command.
Common Controls			*Operate on all features connected to them, no command required.*
Initialise	Z	1	Sets module to a defined state. (Accompanied by S2 and B).
Inhibit	I	1	Disables features for duration of signal.
Clear	C	1	Clears registers. (Accompanied by S2 and B).
Non-Standard Connections			
Free bus-lines	P1,P2	2	For unspecified uses.
Patch contacts	P3–P5	3	For unspecified interconnections. No Dataway Lines.
Mandatory Power Lines			*The crate is wired for mandatory and additional lines.*
+24 V d.c.	+24	1	
+6 V d.c.	+6	1	
−6 V d.c.	−6	1	
−24 V d.c.	−24	1	
0 V	0	2	Power return.
Additional Power Lines			*Lines are reserved for the following power supplies*
+200 V d.c.	+200	1	Low current for indicators etc.
+12 V d.c.	+12	1	
−12 V d.c.	−12	1	
117 V a.c. (Live)	ACL	1	
117 V a.c. (Neutral)	ACN	1	
Clean Earth	E	1	Reference for circuits requiring clean earth.
Reserved	Y1,Y2	2	Reserved for future allocation.
TOTAL		86	

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Table 4.2. Pin Allocation at Normal Station Viewed from Front of Crate (Table II of TID-25875).

(Viewed from front of crate)

Bus-line	Free Bus-line	P1	B	Busy	Bus-line
Bus-line	Free Bus-line	P2	F16	Function	Bus-line
Individual patch contact		P3	F8	Function	Bus-line
Individual patch contact		P4	F4	Function	Bus-line
Individual patch contact		P5	F2	Function	Bus-line
Bus-line	Command Accepted	X	F1	Function	Bus-line
Bus-line	Inhibit	I	A8	Sub-address	Bus-line
Bus-line	Clear	C	A4	Sub-address	Bus-line
Individual line	Station Number	N	A2	Sub-address	Bus-line
Individual line	Look-at-Me	L	A1	Sub-address	Bus-line
Bus-line	Strobe 1	S1	Z	Initialise	Bus-line
Bus-line	Strobe 2	S2	Q	Response	Bus-line
		W24	W23		
		W22	W21		
		W20	W19		
		W18	W17		
24 Write Bus-lines		W16	W15		
		W14	W13		
W1 = least significant bit		W12	W11		
W24 = most significant bit		W10	W9		
		W8	W7		
		W6	W5		
		W4	W3		
		W2	W1		
		R24	R23		
		R22	R21		
		R20	R19		
		R18	R17		
24 Read Bus-lines		R16	R15		
		R14	R13		
R1 = least significant bit		R12	R11		
R24 = most significant bit		R10	R9		
		R8	R7		
		R6	R5		
		R4	R3		
		R2	R1		
	−12V d.c.	−12	−24	−24V d.c.	
	+200V d.c.	+200	−6	−6V d.c.	
Power	117V a.c. Live	ACL	ACN	117V a.c. Neutral	Power
Bus-lines	Reserved	Y1	E	Clean Earth	Bus-lines
	+12V d.c.	+12	+24	+24V d.c.	
	Reserved	Y2	+6	+6V d.c.	
	0V (Power Return)	0	0	0V (Power Return)	

The assignment of contacts at the Dataway connector and their connections to bus-lines, individual lines and patch contacts must be as shown in Table II for normal stations and Table III for the control station. The control station must be to the right of all normal stations.

Table 4.3. Pin Allocation at Control Station Viewed from Front of Crate (Table III of TID-25875).

(Viewed from front of crate)

Individual patch contact		P1	B	Busy	Bus-line
Individual patch contact		P2	F16	Function	Bus-line
Individual patch contact		P3	F8	Function	Bus-line
Individual patch contact		P4	F4	Function	Bus-line
Individual patch contact		P5	F2	Function	Bus-line
Bus-line	Command Accepted	X	F1	Function	Bus-line
Bus-line	Inhibit	I	A8	Sub-address	Bus-line
Bus-line	Clear	C	A4	Sub-address	Bus-line
Individual patch contact		P6	A2	Sub-address	Bus-line
Individual patch contact		P7	A1	Sub-address	Bus-line
Bus-line	Strobe 1	S1	Z	Initialise	Bus-line
Bus-line	Strobe 2	S2	Q	Response	Bus-line
		L24	N24		
		L23	N23		
		L22	N22		
		L21	N21		
		L20	N20		
		L19	N19		
		L18	N18		
		L17	N17		
		L16	N16		
		L15	N15		
		L14	N14		
24 individual Look-at-Me lines		L13	N13	*24 individual Station Number lines*	
L1 from Station 1, etc.		L12	N12	N1 to Station 1, etc.	
		L11	N11		
		L10	N10		
		L9	N9		
		L8	N8		
		L7	N7		
		L6	N6		
		L5	N5		
		L4	N4		
		L3	N3		
		L2	N2		
		L1	N1		
	−12V d.c.	−12	−24	−24V d.c.	
	+200V d.c.	+200	−6	−6V d.c.	
Power	117V a.c. Live	ACL	ACN	117V a.c. Neutral	Power
Bus-lines	Reserved	Y1	E	Clean Earth	Bus-lines
	+12V d.c.	+12	+24	+24V d.c.	
	Reserved	Y2	+6	+6V d.c.	
	0V (Power Return)	0	0	0V (Power Return)	

Table 4.4. The Function Codes (Table IV of TID-25875).

No.	Function	F16	F8	F4	F2	F1	No.
0	Read Group 1 Register	0	0	0	0	0	0
1	Read Group 2 Register	0	0	0	0	1	1
2	Read and Clear Group 1 Register	0	0	0	1	0	2
3	Read Complement of Group 1 Register	0	0	0	1	1	3
	Functions which use the R lines						
4	Non-standard	0	0	1	0	0	4
5	Reserved	0	0	1	0	1	5
6	Non-standard	0	0	1	1	0	6
7	Reserved	0	0	1	1	1	7
	Additional functions which use the R lines						
8	Test Look at Me	0	1	0	0	0	8
9	Clear Group 1 Register	0	1	0	0	1	9
10	Clear Look at Me	0	1	0	1	0	10
11	Clear Group 2 Register	0	1	0	1	1	11
12	Non-standard	0	1	1	0	0	12
13	Reserved	0	1	1	0	1	13
14	Non-standard	0	1	1	1	0	14
15	Reserved	0	1	1	1	1	15
	Additional Functions						
	These functions do not use the R or W lines						
16	Overwrite Group 1 Register	1	0	0	0	0	16
17	Overwrite Group 2 Register	1	0	0	0	1	17
18	Selective Overwrite Group 1 Register	1	0	0	1	0	18
19	Selective Overwrite Group 2 Register	1	0	0	1	1	19
	Functions which use the W lines						
20	Non-standard	1	0	1	0	0	20
21	Reserved	1	0	1	0	1	21
22	Non-standard	1	0	1	1	0	22
23	Reserved	1	0	1	1	1	23
	Additional functions which use the W lines						
24	Disable	1	1	0	0	0	24
25	Increment Preselected Registers	1	1	0	0	1	25
26	Enable	1	1	0	1	0	26
27	Test Status	1	1	0	1	1	27
28	Non-standard	1	1	1	0	0	28
29	Reserved	1	1	1	0	1	29
30	Non-standard	1	1	1	1	0	30
31	Reserved	1	1	1	1	1	31
	Additional Functions						
	These functions do not use the R or W lines						

5. MAINTENANCE AND CALIBRATION

5.1. CAUTIONS

Certain solvents may possibly damage the printed-circuit board or other components. If uncertain as to the compatibility of a specific solvent and any of the components, consult EG&G ORTEC before using it.

Always ensure that CAMAC crate power is turned off before installing or removing any CAMAC module.

Always ensure that all pins on the CAMAC Dataway connector on the rear of the unit are clean before installing any CAMAC module in its crate.

Always heat-sink the leads to diodes, transistors, and IC's whenever soldering or unsoldering them.

Never use excessive force in installing or removing any CAMAC module.

Handle all printed-circuit boards with care.

Do not clean solder-clogged printed-circuit board holes by heating and then pushing a wire through them. This procedure can damage the board by lifting the land. Heat the hole as little as possible and then use a solder puller to remove excess solder.

5.2. PREVENTIVE MAINTENANCE

The only preventive maintenance required involves giving reasonable attention to mechanical details. Keep the signal connectors clean, and periodically remove the cover plates to inspect the interior of the module for excessive dust accumulation. Clean as often as required by local conditions (normally about once every 12 months).

5.3. CORRECTIVE MAINTENANCE

Corrective maintenance will generally be restricted to replacing defective components, such as resistors, capacitors, diodes, transistors, and IC's, to replacing missing hardware, and to tightening loose hardware. In tightening screws, nuts, etc., *do not* use excessive force.

When replacing components on a printed-circuit board, be sure that the board is not damaged by excessive heating. When unsoldering leads, grip the lead to be unsoldered with a tool that also acts as a heat sink. Heat the solder joint as little as possible while maintaining a steady pull on the component lead to assure prompt removal of the lead. Use a solder puller to remove excess solder from the board. *Do not* redrill holes in the printed-circuit board. When the integrity of a plated-through hole is in doubt, solder the component lead on both sides of the board.

5.4. TEST POINTS AND VOLTAGES

Digital circuits operate in only the on state or the off state. Therefore, with the exception of certain circuit points in networks consisting of resistors, capacitors, diodes, and transistors that are external to integrated circuits, the voltages will normally be either logic level. The voltage read at any point depends on the function of the IC, transistor, or other component and on its input.

The voltages listed in Table 5.1 are typical values that were measured in the portions of the AD811 circuits that differ from the normal digital type and therefore have significant levels that are different from the supply level. These voltages are to be considered as typical, rather than absolute, and are furnished to aid in troubleshooting suspected circuits where a malfunction occurs.

The conditions used for the measurements included: measurements were made with a DVM with an 11 MΩ input impedance; the proper power supply voltage levels were furnished at the module connector; and the module had received a strobe input that was followed by a Z·S2. The test points are listed for components that are included in section 0 and these are typical for the equivalent test points in each of the other seven sections.

Table 5.1. Typical Voltage Measurements.

Test Point	Voltage	Test Point	Voltage	Test Point	Voltage
Q002E	−0.6	D801K	+5.0	IC801(8)	−5.2
Q004(A)E	−1.25	Q803B	−5.2	Q821E	−0.04
Q004(A)C	+5.3	Q803C	−5.9	IC801(9)	−0.7
Q007E	−3.28	Q819E	+3.0	IC801(13)	−1.8
Q007B	−2.6	Q813E	−1.63	Q805E	−0.48
Q009E	−5.9	Q814E	−0.88	Q805C	−0.75
Q009B	−5.2	D810A	−11.7	IC801(2)	−1.7
C002	−2.4	D811K	−5.3	IC801(4)	−2.4
Q004(B)E	−0.6	Q815E	−0.3	IC801(5)	−0.7
Q004(B)B	−0.03	Q815B	0	Q810B	−1.8
Q004(B)C	+9.9	Q816B	0	Q811E	−1.7
Q011E	+10.7	Q817E	−6.0	Q811B	−1.0
Q011B	+10.6	Q817B	−6.0	Q811C	−0.8
Q012B	+9.96	D814A	+6.0	Q812B	−0.7
Q013B	+0.7	Q818C	+5.0	IC802(1)	+2.5
Q013C	0	Q804B	−0.2	IC802(3)	+1.9
IC804(6)	+5.0	IC801(7)	−0.57	IC802(6)	+3.8
Q801E	+0.3	D806K	+4.0	IC803(3)	+1.6
Q801B	0	IC801(10)	−0.73	IC804(3)	+1.6
Q802B	−0.45	IC801(11)	−0.7		
D801A	+2.47	IC801(14)	−0.7		

5.5. STROBE GATE WIDTH ADJUSTMENT

The strobe gate width circuit, Q805 and Q821, is a monostable that has a recovery time adjustable in the limits of about 50 through 350 ns. Its recovery time is adjusted by R829, which is located at the bottom near the center of the printed circuit. In each application, it must be set to extend the gate interval from the leading edge of the strobe input signal until a peak is present to be measured in each of the eight active sections.

Since the time when the input peak of a pulse through the linear input circuit will occur is a function of the shaping times in the preamplifier and amplifier, a good method that can be used to adjust the strobe gate width is as follows:

1. Connect the preamplifier-amplifier circuit leading to one of the signal input connections on the AD811. Select the shaping time constants that will be used in the amplifier and adjust its gain for normal operation.

2. Furnish the output of a precision pulse generator into the test input of the preamplifier and adjust its amplitude such that the amplifier output amplitude is less than +2 V.

3. Use the leading edge of the pulse from the pulse generator as a strobe input to the AD811.

4. Measure the input signal with the AD811 under various settings of the gate width control. Select a control setting that shows no change of measurement for a minor change of the control setting. The minimum setting that reflects this quality is one that provides a gate width approximately equal to the time to the peak of the amplifier output signal.

5.6. CONVERSION CALIBRATION

The slope and zero intercept for the distribution of input voltage versus measured counts are adjustable for each section individually. The pedestal, or zero intercept, is adjusted with R*k*31, where *k* is the section number, 0 through 7. The slope is adjusted with R*k*17. On the printed circuit, these controls are located in vertical rows of eight potentiometers, with the zero intercept controls near the front panel and the slope controls about 3 inches toward the rear of the printed circuit; section 0 is across the top of the printed circuit and sections 1 through 7 are aligned horizontally below section 0.

Use the following procedure to calibrate each of the eight sections in the AD811:

1. Apply a precise dc voltage level at the input. Use a level near +2 V.

2. Furnish a strobe input and measure the dc level; it should be at or near 1 count per millivolt of the input (2000 counts for +2 V).

3. Adjust the slope control as necessary to measure the input correctly.

4. Reduce the input dc voltage level to about +0.5 V.

5. Furnish a strobe and measure this level; it should be at or near 1 count per millivolt of the input (500 counts for +0.5 V).

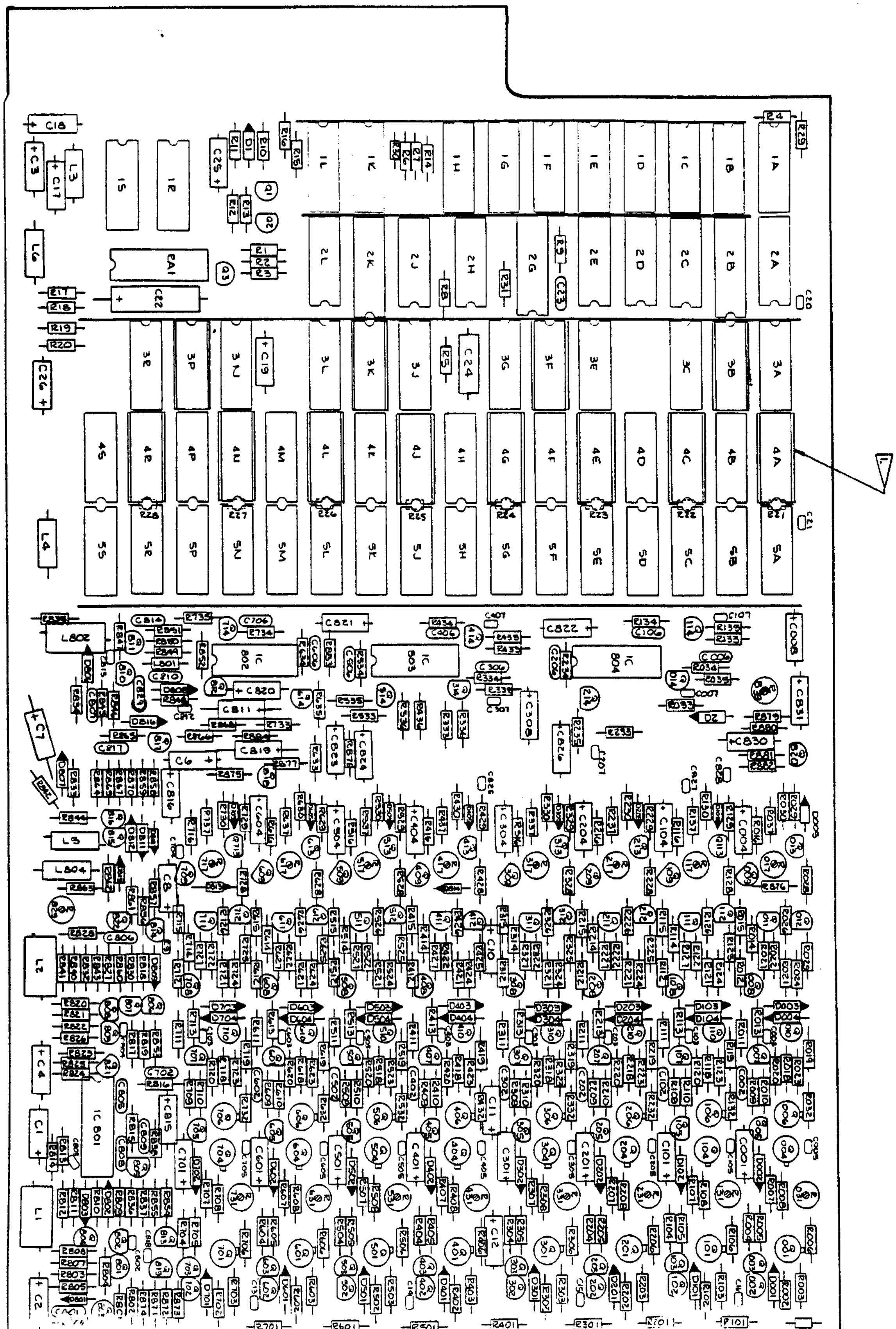
6. Adjust the zero intercept as necessary to measure the input correctly.

7. Repeat steps 1 through 6 until both voltage levels are measured accurately.

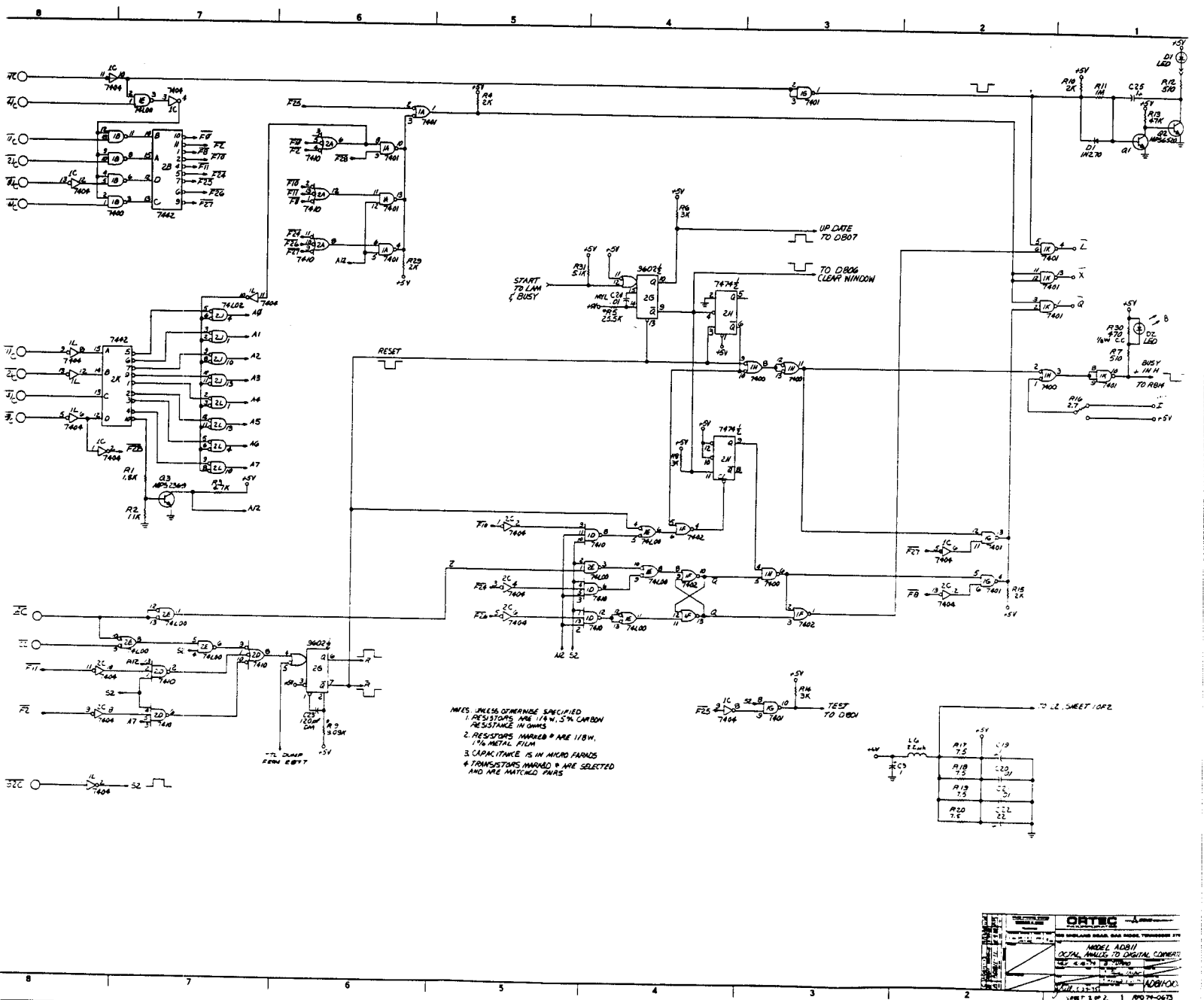
5.7. REFERENCE VOLTAGE ADJUSTMENT

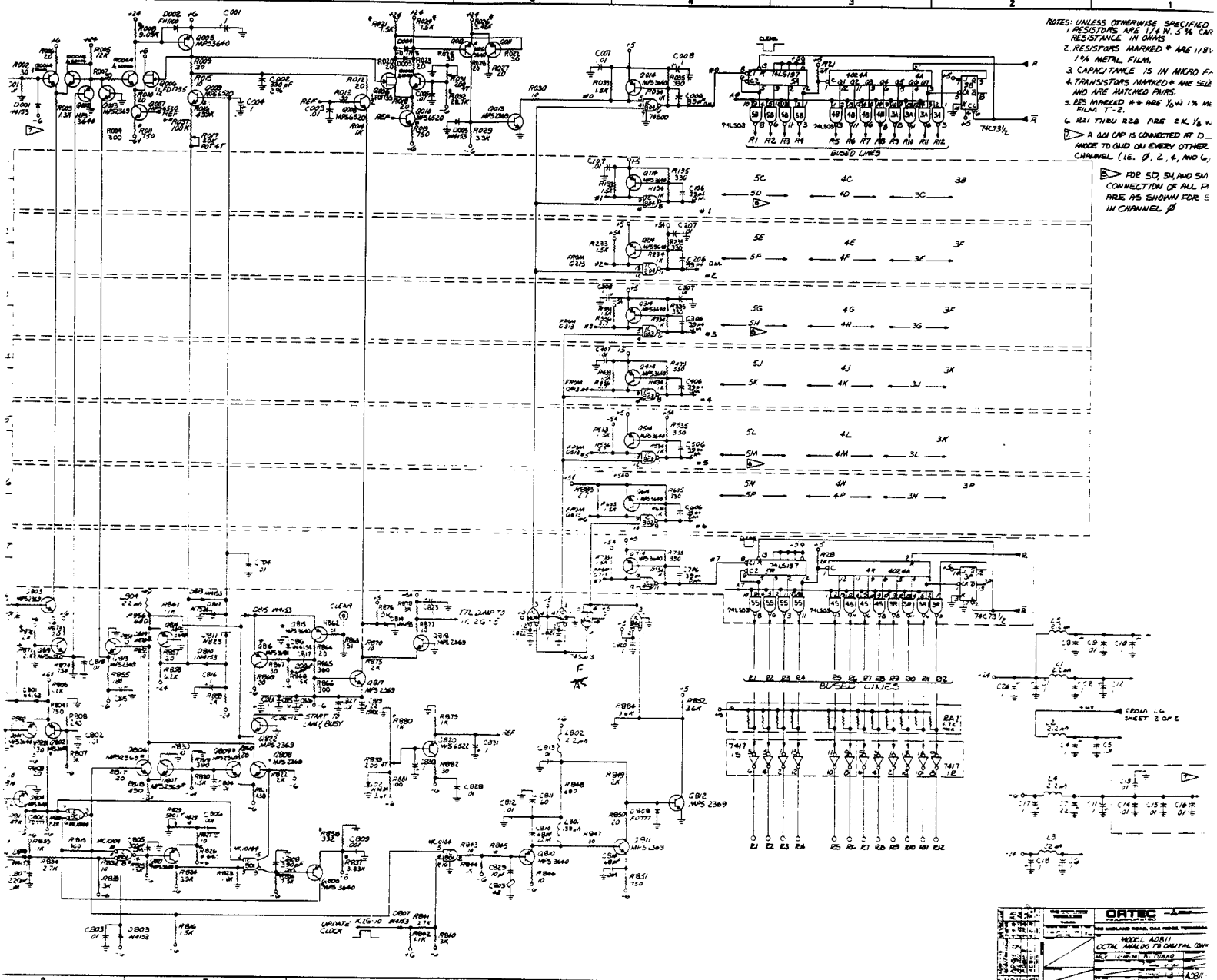
If, during the conversion calibration procedure, the zero intercept control range is not adequate in one or more sections, the reference level that is furnished from R839 may require a minor adjustment. The normal adjustment of R839 is such that the reference level that is furnished from Q820E to all eight comparators is −2.6 V. The range of the control is from about −2.3 to −2.9 V. R820 is located near the top center of the printed circuit.

Any adjustment of R839 requires that all eight sections of the AD811 must be recalibrated according to the procedure in Section 5.6.



AD811-0201 (L)


RESET
UP DATE TO DB07
START TO LAM & BUSY
TO DB06 CLEAR WINDOW
BUSY + IN H
TO RB14
TEST TO DB01
TO L2, SHEET 1 OF 2
NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTORS ARE 1/4 W, 5% CARBON RESISTANCE IN OHMS
2. RESISTORS MARKED * ARE 1/8 W, 1% METAL FILM
3. CAPACITANCE IS IN MICRO FARADS
4. TRANSISTORS MARKED * ARE SELECTED AND ARE MATCHED PAIRS
MODEL ADB11
OCTAL ANALOG TO DIGITAL CONVERTER
ADB11-00
SHEET 1 OF 2
APD 74-0673


NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTORS ARE 1/4 W. 5 % CAR
RESISTANCE IN OHMS
2. RESISTORS MARKED * ARE 1/8
1% METAL FILM.
3. CAPACITANCE IS IN MIKRO F
4. TRANSISTORS MARKED * ARE SEL
AND ARE MATCHED PAIRS.
5. RES MARKED ** ARE 1/8 W 1% ME
FILM T-2.
6. R21 THRU R28 ARE 2K. 1/2 W.
A .001 CAP IS CONNECTED AT D
ANODE TO GND ON EVERY OTHER
CHANNEL (I.E. Ø, 2, 4, AND 6)
FOR 5D, 5H, AND 5M
CONNECTION OF ALL P
ARE AS SHOWN FOR 5
IN CHANNEL Ø
BUSED LINES
BUSED LINES
FROM LG SHEET 2 OF 2
TTL LOAD *3
UPDATE K26-10 CLOCK
ORTEC
MODEL AD811
OCTAL ANALOG TO DIGITAL CONV
AD811
SHEET 1 OF 2