PerkinElmer instruments.
ORTEC Products

AD413A
CAMAC Quad 8k ADC

- Multiplexed, 4-input, 8064-channel ADC with CAMAC and fast FERAbus TM readout for multi-parameter experiments
- 6-µs conversion time per active input, and 100 ns/word FERAbus readout
- FERAbus readout can skip ADCs with no information in 3 ns
- CAMAC control of: FERAbus/CAMAC readout, zero and overflow suppression, master gate, individual gates, singles/coincidence modes, and each lower-level discriminator
- Differential inputs suppress ground-loop noise

The ORTEC Model AD413A CAMAC Quad 8k ADC is a multiplexed, four-input, 13-bit analog-to-digital converter (ADC) with CAMAC and fast FERAbus readout. It is a very productive solution for high-multiplicity multiparameter experiments because it has a conversion time of 6 µs per active input, and a 100-ns-per-word FERAbus readout with the ability to skip ADCs with zero information in 3 ns. This 8064-channel ADC can be used with Ge detectors, silicon charged-particle detectors, scintillation detectors, proportional counters, and ionization chambers.

Each of the four analog inputs has its own peak amplitude stretcher, and accepts pulses in the linear range from 0 to +10 V. The stretchers are multiplexed on a first-come, first-served basis to a 13-bit, successive-approximation ADC with sliding scale linearization. If two or more inputs receive coincident pulses, the pulse amplitudes are stored in their respective stretchers, so that the ADC can successively convert each input. The dc-coupled analog inputs accept unipolar and bipolar pulses from standard spectroscopy amplifiers with shaping times from 0.25 to 20 µs. Differential inputs are incorporated to suppress ground-loop noise when connected to systems with multiple power supplies and grounds.

Each analog input has its own gate input (GATE 1, 2, 3, 4) to suppress analysis of unrelated events when the master gate in the FERA (Fast Encoding and Readout ADC) ECL CONTROL bus is used to synchronize coincident events. The master gate is also available as a TTL input on a LEMO connector, for use in the coincidence mode with CAMAC readout. CAMAC commands permit enabling and disabling the module's response to any gate input. This is useful when selecting the coincidence mode or the singles mode for the Model AD413A under CAMAC control. Four LEMO connectors on the rear panel accept the pile-up rejector logic signals from the four spectroscopy amplifiers supplying the associated analog input pulses.

Additional modes selectable by CAMAC command are: CAMAC or FERAbus readout, zero suppression or no zero suppression during readout, overflow suppression, singles or coincidence analysis, and random access versus sequential access during CAMAC readout. Each analog input has its own lower-level discriminator, separately adjustable by CAMAC command over the range from 0 to 512 mV with 2 mV/bit resolution.

The Model AD413A is compatible with the standard LeCroy FERA control and data output busses. This system can provide very fast readout of the ADCs with non-zero events in a CAMAC crate full of ADCs. For both data acquisition and readout, the control bus synchronizes all ADCs with the experiment's master trigger. This permits identification of all the ADC outputs from the same event and their subsequent assimilation into a common block of data. To the standard FERAbus features, ORTEC has added the ability to select the singles or coincidence analysis mode for any Model AD413A. This feature allows checking the functionality of a detector via the singles spectrum at any time during an experiment.

Normally, all the ADCs in the crate are connected to a LeCroy Model 4301 FERA Driver for control and readout (Fig. 1). The FERA Driver, in turn, delivers the data to either a LeCroy Model 4302 Dual Port Fast Memory in CAMAC, or a CES Model HSM8170 High Speed Memory in VMEbus. Both memories operate in the list mode to assemble the block of coincident events for further processing by an event builder.

To facilitate making the interconnection between the FERAbus Modules, the C-ECLBUS Cable Kit is recommended as a separately ordered accessory. This kit contains the cables and connectors needed for a crate full of FERAbus Modules.

PERFORMANCE

ADC ANALOG INPUTS Four inputs, each with its own peak amplitude stretcher, accept analog input pulses in the range from 0 to + 1 0 V. The stretchers are multiplexed to a single, successive-approximation ADC with sliding scale linearization.

RESOLUTION 8,064 channels (1.25 mV/channel).

CONVERSION TIME 6 µs per active channel input (5 µs for conversion plus 1 µs settling time for the multiplexer).

INTEGRAL NONLINEARITY <±0.025% over the top 99% of the dynamic range.

DIFFERENTIAL NONLINEARITY <±1% over the top 99% of the dynamic range.

TEMPERATURE SENSITIVITY 0 to 50°C.
Gain <50 ppm/°C.
Zero Offset <50 ppm of full scale per °C.

LOWER-LEVEL DISCRIMINATOR RANGE CAMAC controlled from 0 to 512 mV (2 mV/bit).

UPPER-LEVEL DISCRIMINATOR Common to all channels and factory set to approximately +10.2 V.

CAMAC CONTROL OF READOUT MODES Selection of: CAMAC or FERAbus (ECL bus) readout, sequential readout of all ADCs or suppression of ADCs with zeros (zero-suppression mode), overflow-suppression option, singles or coincidence modes, random access or sequential CAMAC readout.

READOUT TIME
Zero-Suppressed Readout Mode Two to five words at 100 ns per word for FERAbus readout, or at 1 µs per word for CAMAC readout.
Sequential Readout Mode 0.8 µs for initialization plus four words at 100 ns per word for FERAbus readout, or at 1 µs per word for CAMAC readout.

CONTROLS AND INDICATORS

CONVERT 1, 2, 3, 4 Four front-panel red LEDs, one for each channel. Each LED blinks once for each pulse that is accepted for conversion.

PD Two front-panel red LEDs, one for the ECL CONTROL connector, and one for the ECL DATA OUTPUT connector. Turned on when the ECL pull-down resistors or termination resistors are installed for the respective connector.

STRETCHER ZERO OFFSET A 12-turn potentiometer mounted on each of the stretcher printed circuit boards permits adjustment of the stretcher dc offset so that zero pulse amplitude is digitized into channel zero. Maximum input offset compensation is ±20 mV.

INPUTS

IN 1, 2, 3, 4 Four separate front-panel BNC connectors accept analog pulses for pulse amplitude digitization in the linear range from 0 to +10 V. Each input has its own peak amplitude stretcher multiplexed to the common ADC. Inputs accept positive unipolar pulses, positive gated integrator pulses, or bipolar pulses, with the positive lobe leading. Pulse shapes can be semi-Gaussian or triangular, with shaping time constants from 0.25 to 20 µs, or delay-line-shaped with widths >0.25 µs. Maximum input is ±12 V. No internal delay. Center conductor input impedance is 2000 Ω to ground, dc-coupled. The floating BNC connector shield is used with a differential input amplifier to suppress common-mode input noise caused by ground loops. The common-mode rejection ratio is nominally 99:1 with a zero-impedance source, and nominally 22:1 with a 93-Ω signal source.

CAMAC COMMANDS

Z Initializes module. Clears the module, sets all bits of control registers 1 and 2 to zero, and sets all LLD registers to 36 (72 mV).

C Performs the same function as the CLR input on the ECL CONTROL bus.

I Inhibits subsequent conversions when present. Conversions and readouts already in progress are not affected. Used to start and stop data acquisition.

X Generated by the module for all valid functions.

Q Generated by the module if the function can be executed.

L LAM is set (if CAMAC readout is enabled, and if LAM is enabled) after the end of conversion, if there are data to be read. See CONTROL REGISTER FORMAT.

F(0)·A(0) Read Control Register 1.

F(0)·A(1) Read Control Register 2.

F(1)·A(0) Read Channel 1 lower-level discriminator setting.

F(1)·A(1) Read Channel 2 lower-level discriminator setting.

F(1)·A(2) Read Channel 3 lower-level discriminator setting.

F(1)·A(3) Read Channel 4 lower-level discriminator setting.

F(2)·A(0–3) Read ADC conversions. When the Random Access mode is selected, A = 0, 1, 2, or 3 selects the ADC to be read (ADC 1, 2, 3, or 4, respectively). When the Sequential CAMAC readout mode is selected, the value given for A is ignored, and the command is issued four times to read the four ADCs in sequence. See B14 of Control Register 1. If zero-suppression is active in the Sequential CAMAC readout mode, the command is issued two to five times until Q = 0. Q = 1 if valid data is available.

F(8)·A(0) Test LAM. Q = 1 if LAM is present.

F(9)·A(0) Clear Module. Performs the same function as the C command, except only for the single module being addressed through CAMAC.

F(10)·A(0) Test and clear LAM. Q = 1 if LAM was set.

F(16)·A(0) Write into Control Register 1.

F(16)·A(1) Write into Control Register 2.

GATE 1, 2, 3, 4 Four front-panel LEMO connectors provide separate gating for each analog input. Inputs are compatible with TTL logic levels. A low logic level (0 to +0.8 V) prevents analysis of the analog signal at the associated IN connector; a high logic level (+2 to +5 V) permits analysis of the analog signal. With no input connected, the GATE input remains at the high logic level. The GATE signal must be at the desired logic level prior to the peak amplitude of the analog pulse, and must extend ≥0.5 µs beyond peak detection. Input impedance is 1000 Ω. Response to each GATE connector can be enabled/disabled by CAMAC commands.

GATE Front-panel LEMO connector accepts the master gate signal for coincidence mode operation with CAMAC readout. See ECL GATE for function. A low TTL logic level (0 to +0.8 V) prevents analysis, and a high TTL logic level (+2 to +5 V) permits analysis. With no input connected, the GATE input remains at the low logic level. Input impedance is 1000 Ω.

PUR 1, 2, 3, 4 Four rear-panel LEMO connectors accept the pile-up rejector logic signals from the four spectroscopy amplifiers supplying the associated analog input pulses. The inputs are compatible with TTL logic levels. A high logic level (+2 to +5 V) causes rejection of the analog signal; a low logic level (0 to +0.8 V) permits analysis of the analog signal. The circuit defaults to a low logic level if no input is connected. The PUR signal must be at the desired logic level prior to the peak amplitude of the analog pulse, and must extend ≥0.5 µs beyond peak detection. Input impedance is 1000 Ω. Can be used as veto inputs.

ECL INPUTS/OUTPUTS

The fast FERAbus readout utilizes the front-panel ECL CONTROL bus and the ECL DATA OUTPUT bus.

ECL LOGIC LEVELS Nominal differential ECL logic levels (into 100 Ω differential load) are:

	Left (+) Pin	**Right (–) Pin**
Logic 0	–1.8 V	–0.9 V
Logic 1	–0.9 V	–1.8 V

F(17)·A(0) Write Channel 1 lower-level discriminator value.

F(17)·A(1) Write Channel 2 lower-level discriminator value.

F(17)·A(2) Write Channel 3 lower-level discriminator value.

F(17)·A(3) Write Channel 4 lower-level discriminator value.

CONTROL REGISTER 1 FORMAT

Bit and Function

B1 to B8 Virtual Station Number. Index Source for readout with zero suppression. (Lower eight bits of header word.)

B9 Zero-suppression enable. When B9 = 0, ADCs with zeros for data are skipped during readout.

B10 ECL port enable. When B10= 0 , ECL port readout is enabled. When B10 = 1, CAMAC readout is enabled.

B11 Not used.

B12 Not used.

B13 Coincidence/Singles selection for all 4 inputs. When B13 = 0, the coincidence mode is selected. When B13 = 1, the singles mode is selected. When in the singles mode, the zero-suppression mode must be selected for all ADCs in the same FERAbus readout loop.

B14 CAMAC random access enable. When B14 = 1 and B10 = 1 and B9 = 1, random access CAMAC readout is enabled.

B15 CAMAC LAM enable. When B15 = 1, LAM is enabled.

B16 Overflow-suppression enable. When B16 = 0, overflows are converted to zeros in the ADC output data. Readout will be suppressed only if the zero-suppression mode is selected.

CONTROL REGISTER 2 FORMAT

Bit and Function

B1 Enable GATE 1 (B1 = 0). When B1 = 1, the GATE 1 input is ignored and all analog pulses in channel 1 are converted, unless gated by the master GATE in the ECL CONTROL bus, or by PUR 1.

B2 Enable GATE 2 (B2 = 0). Function similar to B1.

ECL DATA OUTPUT Front-panel 17- by 2-pin connector (AMP 1-103326-7) provides the digitized ADC outputs for connection to the FERA data readout bus. Differential ECL outputs are employed, with bit 1 assigned to the two pins in row 1, and bit 16 occupying the two pins in row 16. Row 17 is not connected. See READOUT FORMAT. Interconnection between ADC modules and the FERA Driver (LeCroy 4301) requires construction of a 34-conductor ribbon cable (3M part number 3365/34) with 17- by 2-pin headers (3M 3414-6006 or AMP 499498-9) spaced to match the configuration of modules (Fig. 1). Only one module on the ECL DATA OUTPUT bus should have the pull-down resistors installed (See PD LED and Fig. 1).

ECL CONTROL BUS Front-panel 8- by 2-pin connector accommodates the control bus for synchronizing data acquisition among multiple ADCs, and for ECL readout. A row of two pins is assigned to each differential ECL input or output. Interconnection between ADC modules and the FERA Driver (LeCroy 4301) requires construction of a 16-conductor ribbon cable (3M part number 3365/16) with 8- by 2-pin headers (3M 3452-6006 or AMP 499497-3) spaced to match the configuration of modules (Fig. 1). Only one module on the ECL CONTROL bus should have the pull-down and termination resistors installed (See PD LED and Fig. 1). The logic signals in the ECL CONTROL bus are listed below. Except where noted otherwise, the inputs to the AD413A are provided from the LeCroy 4301 FERA Driver connected to the bus.

N/C No connection.

WST The Write Strobe output indicates when each output word is valid on the ECL DATA OUTPUT connector. WST is released 15 ns after the Write Acknowledge (WAK) is received.

REQ The Request output indicates that the module has completed its conversions, and is ready to take control of the ECL DATA OUTPUT bus for readout. REQ can be asserted only if FERAbus readout is enabled.

B3 Enable GATE 3 (B3 = 0). Function similar to B1.

B4 Enable GATE 4 (B4 = 0). Function similar to B1.

B5 Enable master GATE (B5 = 0) for the coincidence mode. When B5 = 1, the master GATE signal in the ECL CONTROL bus is ignored, and all analog pulses are converted, unless gated by GATE 1, 2, 3, or 4, or by PUR 1, 2, 3, or 4. B5 = 1 is used with the singles mode.

READOUT FORMAT

The readout format of the Model AD413A is identical in both the CAMAC and the FERAbus ECL readout modes.

WITHOUT ZERO-SUPPRESSION

B16	B15	B14	B13 . . . . . B1
0	0	0	CHANNEL 1 DATA
0	0	0	CHANNEL 2 DATA
0	0	0	CHANNEL 3 DATA
0	0	0	CHANNEL 4 DATA

WITH ZERO-SUPPRESSION

When zero-suppression is enabled and valid data are received, two to five data words are output. The first is always a Header word:

B16	B15	B14	B13 . . .B12	B11	B10	B9	B8 . .B1
1	0	0	WRDCNT	0	0	0	VSN

Followed by 1 to 4 data records, each with the following format:

B16	B15 . . . B14	B13 . . . . B1
0	SUBADDR	DATA

DEFINITIONS

WRDCNT The word count is a value from 0 to 3 that defines the number of data records that follow in the readout. A value of 0 indicates that four data records follow.

VSN The Virtual Station Number (0–255) identifies the module number during zero-suppressed readout. VSN is set via CAMAC command in the lower 8 bits of Control Register 1.

CLR The Clear input clears stored data and conversions in progress for all ADCs connected to the ECL CONTROL bus. It is required in the coincidence mode at the end of readout to simultaneously release all ADCs for the next conversion. CLR is not required in the singles mode. The differential ECL input impedance is 100 Ω. Minimum width, 5 ns. Clear can also be initiated from the CAMAC interface. If clear is asserted during ADC conversion, up to 5 µs are required to clear the module.

GATE The GATE input simultaneously provides the master gate signal to all ADCs connected to the ECL CONTROL bus for coincidence mode operation. This ECL GATE input is OR'ed with the TTL master GATE input from the LEMO connector. The logic 1 state enables acceptance of the analog input signal for conversion, and forces all ADCs to wait for a common clear (CLR) after analyzing coincident events. With no signal connected, the GATE input remains in the logic 0 state. The GATE signal must arrive before the peak amplitude on the analog input signal, and extend ≥0.5 µs beyond peak amplitude detection. With termination resistors installed, the differential ECL input impedance is 100 Ω. Response to the GATE input can be enabled/ disabled by CAMAC commands.

WAK The Write Acknowledge input signal indicates through the readout controller (LeCroy 4301) that the associated memory has read the current word and that the next word may be sent. The differential ECL input impedance is 100 Ω. WAK minimum width is 30 ns.

GND Connected to ground.

N/C No connection.

REN The Readout Enable input is a front-panel, 1- by 2-pin connector. It accepts the PASS output from a previous module, or the REO output from the LeCroy 4301, to enable readout of the Model AD413A. The ECL differential input impedance is 100 Ω. Interconnection requires construction of a 100-Ω, twisted-pair cable with a 2-pin socket and housing (AMP 1-87756-8 and AMP 5-87456-3) on each end.

SUBADDR The Subaddress (0–3) indicates with which of the four input channels the data is associated. NOTE: the data records are in no particular order in zero-suppression mode. Therefore, the subaddress should always be used to determine which channels are delivering data.

SUBADDR = 0	Channel 1 data
SUBADDR = 1	Channel 2 data
SUBADDR = 2	Channel 3 data
SUBADDR = 3	Channel 4 data

DATA Thirteen bits of ADC conversion data. DATA over 8064 indicates overflow.

ORDERING INFORMATION

To order, specify:

Model	Description
AD413A	CAMAC Quad 8k ADC
C-ECLBUS	Cable Kit for the ECLBUS

PASS The PASS output is provided on a front-panel, 1- by 2-pin connector. It indicates completion of the module's readout cycle on the ECL bus. The PASS output is normally connected to the REN input on the next module to enable readout of the next module (Fig. 1). In the zero-suppression mode, the Model AD413A generates the PASS signal typically within 3 ns of receiving the REN signal if the Model AD413A has no data to read out. The PASS signal from the last Model AD413A in the readout loop is used to generate the CLR signal via the external master trigger logic for the experiment and/or the LeCroy 4301.

ELECTRICAL AND MECHANICAL

POWER REQUIRED The Model AD413A derives its power from a CAMAC crate supplying ±24 V and ±6 V. The power required is +24 V at 380 mA, +6 V at 2 A, –6 V at 1.2 A, and –24 V at 430 mA.

WEIGHT
Net 1.1 kg (2.5 lb).
Shipping 2.0 kg (4.5 lb).

DIMENSIONS CAMAC-standard double-width module 3.42 X 22.15 cm (1.35 X 8.72 in.) front panel per IEEE/583-1982 (Reaff 1988).

OPTIONAL ACCESSORIES

The C-ECLBUS Cable Kit is recommended as an accessory to facilitate the FERAbus interconnections. Each kit contains:

Qty	Description
1	16-conductor ribbon cable with 23 headers installed at 7.6-cm intervals for the ECL Control Bus.
1	34-conductor ribbon cable with 23 headers installed at 7.6-cm intervals for the ECL Data Bus.
1	51-cm long twisted pair cable with 2-pin sockets and headers on each end for the PASS to CLI connection.
23	15-cm long twisted pair cables with 2-pin sockets and headers on each end for the REO to REN, and the PASS to REN connections.

The ribbon cables will serve an entire crate full of FERAbus modules, and can be cut to handle smaller groups of modules.

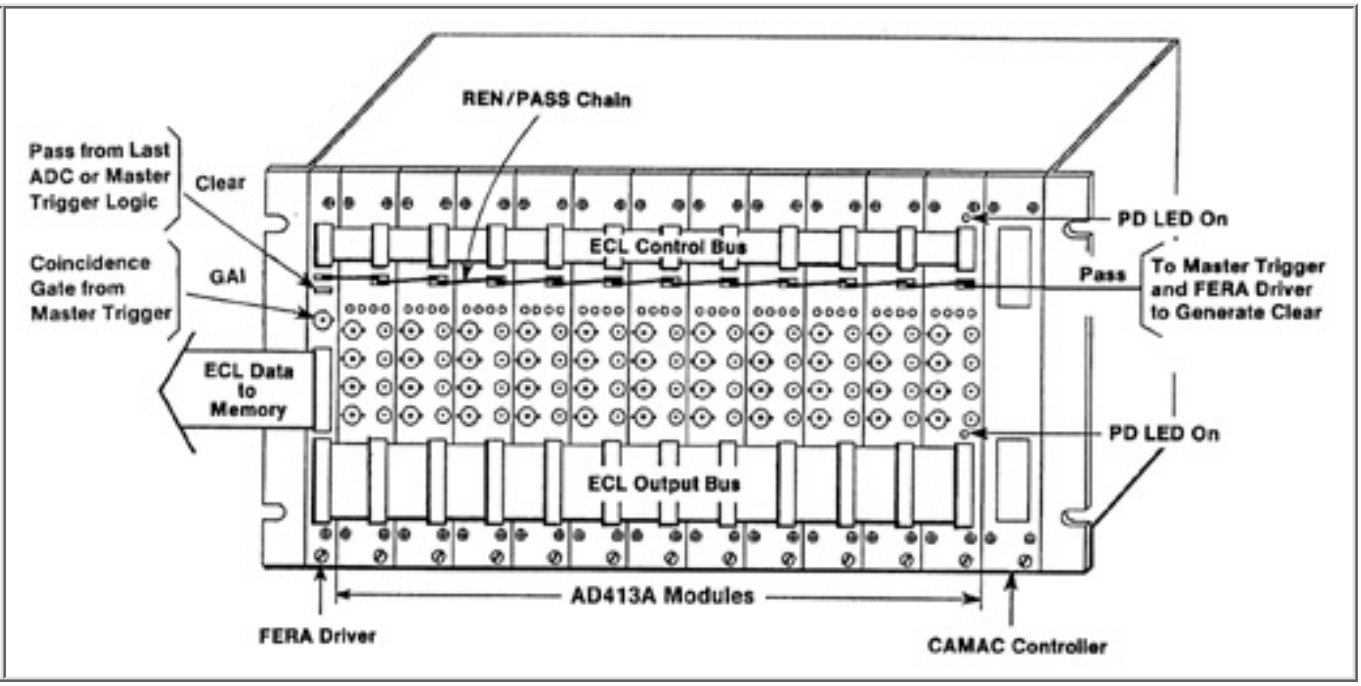

Fig. 1. Interconnection of Multiple AD413As and LeCroy 4301 FERA Driver for FERAbus Readout.