C 124 COINCIDENCE LATCH

OPERATING AND SERVICE MANUAL

1. DESCRIPTION

The C124 Coincidence Buffer is a 24-binary-bit wide, two fold, coincidence module, in a CAMAC-standard double-width module. The inputs are NIM-standard negative fast logic signals, and the output of the 24 latches is on the CAMAC dataway and on a rear panel connector. The rear panel outputs are MECL. When the module inputs are in coincidence with the external strobe, the 24 latches are set. The bits are gated onto the 24 CAMAC Dataway R lines upon receipt of the proper command from the crate controller. The output of the latches is available immediately at the rear panel. The strobe is a bridging type of input. The bridging inputs of the Strobe signal allow the signal to be reused.

The Strobe signal circuit automatically latches on the trailing edge of the first Strobe signal in order to block any subsequent Strobe signals from activating the Strobe signal circuit until the latches have been reset. The data and strobe latches are reset by the Dataway S2-line Strobe signal and any one of function code F(2), function code F(9), and the Dataway C- and Z-line signals (but not function code F(0)) or by a NIM-standard negative fast logic Reset signal fed from an external source through the front panel Reset connector on this module. The reset input is also of the bridging type.

2. SPECIFICATIONS

2.1 DATA INPUTS

In 0 - In 23 LEMO connectors, front panel.

Circuit Characteristics: 50Ω terminated, with <10% reflections for inputs having a 1-nsec rise time; dc-coupled.

Typical Input: NIM-standard fast logic signals $\geq$2 nsec in width, measured at the half-peak-height point on pulses of -600 mV peak amplitude.

Maximum Input: +1.5 V and -3 V.

2.2 CONTROL INPUTS

Front Panel

Strobe (2) LEMO connectors.

Circuit Characteristics: Bridging type, with <20% reflections in a 50Ω system, if Strobe signal line or lines are terminated or reused in their characteristic impedances; input impedance 2 kΩ; dc-coupled.

Input: Same as Data.

Reset: circuit and inputs same as Strobe.

Front panel Reset input signal performs same function as Dataway C- and Z-line signals.

Rear Panel

Dataway Lines

C and Z: Each will reset the Data and Strobe latches on the leading edge of the Dataway S2-line Strobe signal.

S2: Strobe signal provides timing for resetting of Data and Strobe signal latches.

CAMAC Function Codes

F(0) Read Register.

F(2) Read and clear register.

F(9) Clear register.

F(25) Set all latches.

2.3 OUTPUTS (Rear Panel)

Dataway R1-R24 Lines: Data outputs; LSB = R1, MSB = R24.

Dataway Q Line: Signal generated by the C124 in response to a valid subaddress (A(0) only), function code, and N-line signal.

Data - rear panel connector (2DB52P).

Outputs are MECL.

The connector is wired to take twisted pair cable.

3. OPERATION

3.1 INSPECTION AND INSTALLATION

After carefully unpacking the unit, thoroughly inspect it for evidence of damage in shipment. If it has been damaged, refer to the Warranty section for further instructions.

CAUTION

Always ensure that CAMAC crate power is turned off before installing or removing any CAMAC module.

Always ensure that all pins on the CAMAC Dataway connector on the rear of the unit are clear before installing any CAMAC module in its crate.

Never use excessive force in installing or removing any CAMAC module.

After observing the above precautions, install the module in its assigned crate at its assigned numbered station in accordance with prior programming of the computer.

3.2 SIGNAL CONNECTION AND APPLICATION OF POWER

NOTE

50Ω coaxial signal leads terminated in LEMO connectors (male) are required for front panel connections to this unit.

Connect signal leads from the source of the Data signals to the front panel Data signal input connectors (labeled 0 - 23). Connector 0 carries the lease significant bit (LSB), and connector 23 carries the most significant bit (MSB).

Connect a signal lead from the Strobe signal source to the Strobe signal input connector. If the Strobe signal is to be reused, connect a signal lead from the unused front panel Strobe signal connector to the Strobe signal input on the other item of equipment to be strobed. In any case, ensure that each Strobe signal line is terminated in its characteristic impedance either at the unused front panel Strobe signal connector or at the end of each Strobe signal line.

If it is desired to use an externally supplied NIM-standard fast logic Reset signal, connect a signal lead from the source of such a signal to the front panel Reset connector. Terminate the reset line in its characteristic impedance.

Turn CAMAC crate power on. The unit should now be ready for performance testing, as described in Section 5.5.

4. FUNCTIONAL DESCRIPTION

Throughout this discussion, refer to Fig. 4.1, to the logic drawing and schematic, Drawing 306913 and to Table 4.1. Logic elements will in general be identified by the IC number, followed by a hyphen, followed by the output terminal number. When the logic element is a type D or type JK flip-flop or other element having both Q and $\overline{Q}$ outputs, the Q output terminal number will be utilized for such logic element identification. When the logic element is a multiple-bit counter or register or other element having several outputs, the output terminal number of the most significant bit will be utilized for such logic element identification. When there is no ambiguity, the logic element will be identified by the IC number alone.

4.1 GENERAL FUNCTION

In order for any CAMAC module to perform its intended function, it must first be commanded to do so by the crate controller. The intended functions of the C124 are twofold in nature, as follows: (1) the acceptance of NIM-standard fast logic signals (up to and including 24 binary bits), and (2) the delivery of the latch states to the 24 Dataway R lines and to the rear panel connector and the clearing of the Data signal latches and Strobe signal latches at the completion of a CAMAC Dataway operation so that the module is clear and can handle its next data collection and transfer operation. The proper command from the crate controller for the performance of these functions is a combination of the Dataway N-line signal for the module, the correct function code on the Dataway F lines for the performance of the desired function, and a valid subaddress for this module on the Dataway A lines. Subaddress A(0) is the only valid subaddress for the C124.

The C124 has NIM-standard binary data words presented at its 24 front panel Data signal input connectors. When strobed from an external Strobe signal

source, it latches the 24 internal latches to the state of the 24 data inputs and puts the state of the 24 latches on the rear panel connector. A minimum of 1.6 nsec overlap of the input "true" signal and the Strobe signal is required for an input to be latched as true, otherwise the latch is set to false. When commanded to do so by the crate controller, it gates these data bits onto the 24 Dataway R lines. When cleared by F(2) or F(9), it is ready to accept the next data word.

4.2 INHIBIT CIRCUITRY

The Inhibit Circuitry, which consists of IC's 7A-8, 7A-6, and 7B-10 is intended to disable the Function Code Decoding Circuitry if the Dataway N-line signal for this module is absent or an invalid function code or invalid subaddress for this module is sent by the crate controller. The inputs to the Inhibit Circuitry are the Dataway A1, A2, A4, A8, F4, and (through IC 5B-12, which acts as an inverter) N lines. The absence of the Dataway N-line signal, or any of the above signals, will cause the Inhibit Circuitry to inhibit or disable the Function Code Decoding Circuitry.

4.3 DATA ACCEPTANCE AND STROBING

Nim-standard negative fast logic signals are accepted by the front panel Data signal inputs (numbered 0 - 23). Data words consisting of as many as 24 binary bits can be accepted by this module. The signal presented to Data signal input connector 1 is the least significant bit (LSB), and the signal presented to Data signal input connector 24 is the most significant bit (MSB).

Since all 24 Data latches are identical, only Data latch 1 will be specifically discussed in this section. The data bits are handled in each of the other 23 Data latches in precisely the same manner as in Data latch 1.

In the quiescent state, Q1 is on. This produces a high-level signal at terminal 13 of IC 1A. If the signal presented to Data signal input connector 1 is a binary 1 (i.e., -800 mV), the negative signal level (through Q1) produces a low-level signal at terminal 13 of IC 1A.

Now, consider what happens when the Strobe Circuit is strobed by a NIM-standard negative fast logic Strobe signal. In the quiescent state, Q13 is on, and a similar set of conditions exists to that in Data latch 1. There is a high-level signal at terminal 7 of IC 1D and at terminal 9 of IC 1D.

The negative-going Strobe signal (through Q13) produces a low-level signal at terminal 1 of IC 1D and at terminal 9 of IC 1D and at the output of each of these two OR gates. The CAMAC dataway inhibit line blocks the strobe signal through Q27.

The low-level signal which appeared at IC 1A-12 in Data latch 1 during the interval when the Strobe signal was present strobed the data bit through IC 1A-12. If the data bit was a binary 1, it produced a high-level signal at IC 1A-15 and at the output of IC 2B-13, which latched IC 2B-13 in that state through its terminal 15. This produced a high-level signal at IC 3A-14 and 4A-13. The strobe signal should precede the data input by 2 nsec.

This presents the data in the latches to the CAMAC dataway multiplexers and to the rear connector. Typical delay between strobe input and output on rear connector is 10 nsec.

4.4 FUNCTION CODE F (0)

When the Dataway N-line signal for this module, function code F(0), and subaddress A(0) are received by the module, the Function Code Decoding Circuitry sends a Gate signal to the Gate Generator, which responds by sending a Gate signal to all 24 Output Gates and to the Response Generator. The Output Gates deliver all 24 data bits to the 24 Dataway R lines. The Response Generator generates the Dataway Q-line Response signal.

4.5 FUNCTION CODE F(2)

When the Dataway N-line signal for this module, function code F(2), and subaddress A(0) are received by the module, precisely the same events occur as in the case of function code F(0), except that the Function Code Decoding Circuitry does not send a Disable signal to the Data Latch Reset Generator. When the Dataway S2-line Strobe signal is received by the module, the low-level output signal from IC 5B-4 in the Data Latch Reset Generator drives 6A-6 low. This resets both the F(25) latch (IC's 5C-8

and 5C-11) and the data latches through 5B-6, Q28 and Q27. When the reset signal is on, Q27 turns on and pulls the input to data latch false. This resets the latch.

4.6 FUNCTION CODE F(9)

F(9) works just as F(2) with the exception that the read lines are not altered.

4.7 FUNCTION CODE F(25)

Function code F(25) (and N) will set the latch (IC's 5C-8, 5C-11), at S2. F(25) is inverted by 5B-2 and strobed into the latch by S2 at gate 5C-6. This does not latch the data points. The outputs of the F(25) latch are wire ored to the MECL output drivers and appear both on the rear connector and on the CAMAC dataway (when so addressed).

4.8 DATAWAY C- AND Z-LINE SIGNALS

Either of the Dataway C-line Clear and Z-line Initialize signals causes the Function Code Decoding Circuitry to send the Enable signal to each of the Data Latch Reset Generator and the Strobe Input Inhibit Latch Reset Generator so that the Dataway S2-line Strobe signal can remove all Data signal latches and both Strobe signal input block latches, just as in the case of function codes F(2) and F(9).

4.9 FRONT PANEL RESET SIGNAL

The front panel reset signal is fed into Q29. This turns Q27 on, which pulls the diode on the latch circuit and pulls the latch input (2A-10) false which resets the latch. This does not reset the F(25) latch.

4.10 TIMING

A better understanding of the relative timing of the various signals may be gained from a study of Fig. 4.2, which has been excerpted from Specification EUR-4100e.

4.11 SUPPLEMENTARY DATAWAY INFORMATION

Tables 4.2, 4.3, 4.4, and 4.5 have been excerpted from Specification EUR 4100e and are included to serve as an aid in the use of a CAMAC system. These tables respectively present standard Dataway usage, Dataway connector pin assignments at a "normal" station, Dataway connector pin assignments at the Control Station, and the standard function codes.

The Control Station is Station 25 in the crate. The "normal" stations are Station 1 through 24. Since every crate controller must occupy Station 25 and at least one "normal" station (usually Station 24), the C124 will be assigned a location somewhere from Station 1 through Station 23.

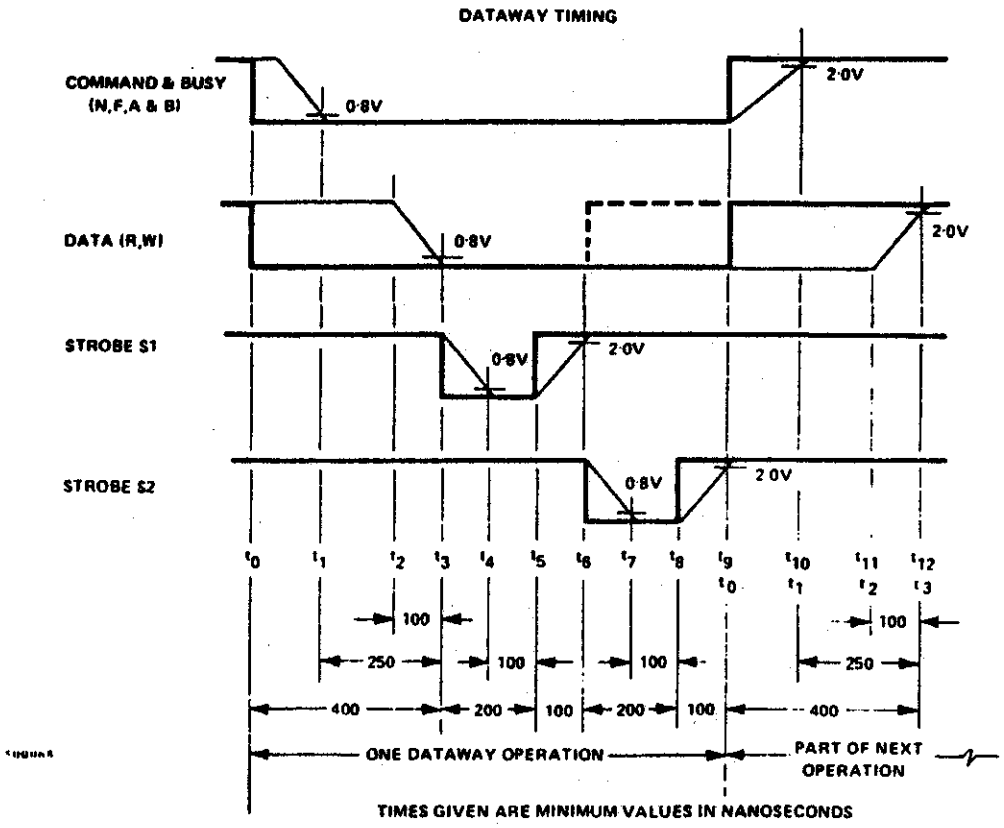

Fig. 4.2. Timing of a Dataway Operation (Fig. 9 of EUR 4100e).

Table 4.2. Standard Dataway Usage (Table I of EUR 4100e).

Title	Designation	Pins	Use at a Module
Command			
Station Number	N	1	Selects the module (Individual line from control station).
Sub-Address	A1, 2, 4, 8.	4	Selects a section of the module.
Function	F1, 2, 4, 8, 16.	5	Defines the function to be performed in the module.
Timing			
Strobe 1.	S1	1	Controls first phase of operation (Dataway signals must not change).
Strobe 2.	S2	1	Controls second phase (Dataway signals may change).
Data			
Write	W1 - W24	24	Bring information to the module.
Read	R1 - R24	24	Take information from the module.
Status			
Look-at-Me	L	1	Indicates request for service (Individual line to control station).
Response	Q	1	Indicates status of feature selected by command.
Busy	B	1	Indicates that a Dataway Operation is in progress.
Common Controls			Operate on all features connected to them, no command required.
Initialise	Z	1	Sets module to a defined state. (Accompanied by S2 and B)
Inhibit	I	1	Disables features for duration of signal.
Clear	C	1	Clears registers. (Accompanied by S2 and B)
Reserved			
Reserved Bus	X	1	Reserved for future allocation.
Private Wiring			
Patch Points	P1 - P5	5	Free for unspecified interconnections. No Dataway lines.
Mandatory Power Lines			The Crate is Wired for Mandatory and Additional Lines
+24V D.C.	+24	1	
+6V D.C.	+6	1	
-6V D.C.	-6	1	
-24V D.C.	-24	1	
0V	0	2	Power return.
Additional Power Lines			Lines are Reserved for the Following Power Supplies
+200V D.C.	+200	1	Low current for indicators etc.
+12V D.C.	+12	1	
-12V D.C.	-12	1	
117V A.C. (Live)	ACL	1	
117V A.C. (Neutral)	ACN	1	
Clean Earth	E	1	Reference for circuits requiring clean earth.
Reserved	Y1, Y2	2	Reserved for future allocation.
TOTAL		86	

Table 4.3. Pin Allocation at Normal Station Viewed from Front of Crate (Table II of EUR 4100e).

Individual Patch Point	P1	B	Busy – Bus Line
" " "	P2	F16	Function " "
" " "	P3	F8	" " "
" " "	P4	F4	" " "
" " "	P5	F2	" " "
Bus Line – Reserved	X	F1	" " "
" " with Patch Point – Inhibit	I	A8	Sub-Address " "
" " " " " – Clear	C	A4	" " "
Individual Lines – Station Number	N	A2	" " "
with Patch Points – Look-at-Me	L	A1	" " "
Bus Line – Strobe 1	S1	Z	Initialise " "
Bus Line – Strobe 2	S2	Q	Response " "
	W24	W23	
	W22	W21	
	W20	W19	
	W18	W17	
	W16	W15	
24 Write Bus Lines	W14	W13	
	W12	W11	
W1 = least significant bit	W10	W9	
W24 = most significant bit	W8	W7	
	W6	W5	
	W4	W3	
	W2	W1	
	R24	R23	
	R22	R21	
	R20	R19	
	R18	R17	
	R16	R15	
24 Read Bus Lines	R14	R13	
	R12	R11	
R1 = least significant bit	R10	R9	
R24 = most significant bit	R8	R7	
	R6	R5	
	R4	R3	
	R2	R1	
Reserved for -12 volts D.C.	-12	-24	-24 volts D.C.
Reserved for +200 volts D.C.	+200	-6	-6 volts D.C.
Reserved 117 volts A.C. Live	ACL	ACN	Reserved for 117 volts A.C. Neutral
Reserved	Y1	E	Reserved for Clean Earth
Reserved for + 12 volts D.C.	+12	+24	+24 volts D.C.
Reserved	Y2	+6	+6 volts D.C.
0 volts (Power return)	0	0	0 volts (Power Return)

Table 4.4. Pin Allocation at Control Station Viewed from Front of Crate (Table III of EUR 4100e).

Individual Patch Point	P1	B	Busy – Bus Line
" " "	P2	F16	Function – " "
" " "	P3	F8	" – " "
" " "	P4	F4	" – " "
" " "	P5	F2	" – " "
Bus Line – Reserved	X	F1	" – " "
" " with Patch Point – Inhibit	I	A8	Sub-address – " "
" " " " " – Clear	C	A4	" – " "
Individual Patch Point	P6	A2	" – " "
" " "	P7	A1	" – " "
Bus Line – Strobe 1	S1	Z	Initialise – " "
Bus Line – Strobe 2	S2	Q	Response – " "
	L24	N24	
	L23	N23	
	L22	N22	
	L21	N21	
	L20	N20	
	L19	N19	
	L18	N18	
	L17	N17	
	L16	N16	
	L15	N15	
	L14	N14	
24 Individual Look-at-Me Lines	L13	N13	24 Individual Station Lines
	L12	N12	
	L11	N11	
	L10	N10	
	L9	N9	
	L8	N8	
	L7	N7	
	L6	N6	
	L5	N5	
	L4	N4	
	L3	N3	
	L2	N2	
	L1	N1	
Reserved for -12 volts D.C.	-12	-24	-24 volts D.C.
Reserved for +200 volts D.C.	+200	-6	-6 volts D.C.
Reserved for 117 volts A.C. Live	ACL	ACN	Reserved for 117 volts A.C. Neutral
Reserved	Y1	E	Reserved for Clean Earth
Reserved for +12 volts D.C.	+12	+24	+24 volts D.C.
Reserved	Y2	+6	+6 volts D.C.
0 volts (Power Return)	0	0	0 volts (Power Return)

Table 4.5. The Function Codes (Table IV of EUR 4100e).

No.	Function		F 16	F 8	F 4	F 2	F 1	No.
0	Read Group 1 Register	Functions which use the R lines	0	0	0	0	0	0
1	Read Group 2 Register		0	0	0	0	1	1
2	Read and Clear Group 1 Register		0	0	0	1	0	2
3	Read Complement of Group 1 Register		0	0	0	1	1	3
4	Non-standard	Additional functions which use the R lines	0	0	1	0	0	4
5	Reserved		0	0	1	0	1	5
6	Non-standard		0	0	1	1	0	6
7	Reserved		0	0	1	1	1	7
8	Test Look at Me	These functions do not use the R or W lines	0	1	0	0	0	8
9	Clear Group 1 Register		0	1	0	0	1	9
10	Clear Look at Me		0	1	0	1	0	10
11	Clear Group 2 Register		0	1	0	1	1	11
12	Non-standard	Additional Functions	0	1	1	0	0	12
13	Reserved		0	1	1	0	1	13
14	Non-standard		0	1	1	1	0	14
15	Reserved		0	1	1	1	1	15
16	Overwrite Group 1 Register	Functions which use the W lines	1	0	0	0	0	16
17	Overwrite Group 2 Register		1	0	0	0	1	17
18	Selective Overwrite Group 1 Register		1	0	0	1	0	18
19	Selective Overwrite Group 2 Register		1	0	0	1	1	19
20	Non-standard	Additional functions which use the W lines	1	0	1	0	0	20
21	Reserved		1	0	1	0	1	21
22	Non-standard		1	0	1	1	0	22
23	Reserved		1	0	1	1	1	23
24	Disable	These functions do not use the R or W lines	1	1	0	0	0	24
25	Increment Preselected Registers		1	1	0	0	1	25
26	Enable		1	1	0	1	0	26
27	Test Status		1	1	0	1	1	27
28	Non-standard	Additional Functions	1	1	1	0	0	28
29	Reserved		1	1	1	0	1	29
30	Non-standard		1	1	1	1	0	30
31	Reserved		1	1	1	1	1	31

5. MAINTENANCE*

5.1 WARNINGS AND CAUTIONS

When any maintenance is done on this module, it is strongly advised that the following WARNINGS and CAUTIONS be observed.

WARNING

When any solvent is used to clean any part of this module, it should be remembered that petroleum-base solvents as a class are generally flammable and that chlorinated solvents as a class are generally toxic and narcotic. Solvents should be used only in open, well-ventilated areas. Petroleum-base solvents should not be used near or in the presence of open flames, and no smoking should be allowed during their use. Along with removing other oils and greases, most solvents will also remove natural skin oils, and high-quality rubber gloves should be worn while using solvents.

CAUTION

Certain solvents may possibly damage the printed-circuit board or other components. If uncertain as to the compatibility of a certain solvent and any of the components, consult EG&G (NID) before using it.

*No calibration of this unit is required.

Always ensure that CAMAC crate power is turned off before installing or removing any CAMAC module.

Always ensure that all pins on the CAMAC Dataway connector on the rear of the unit are clean before installing any CAMAC module in its crate.

Always heat-sink the leads to diodes, transistors, and IC's whenever soldering or unsoldering them.

Never use excessive force in installing or removing any CAMAC module.

Do not clean solder-clogged printed-circuit boards by heating and then pushing a wire through them. This procedure can damage the board by lifting the land.

5.2 PREVENTIVE MAINTENANCE

The only preventive maintenance required involves giving reasonable attention to mechanical details. Keep the signal connectors clean, and periodically remove the cover plates to inspect the interior of the module for excessive dust accumulation. Clean as often as required by local conditions (normally about once every 12 months).

5.3 CORRECTIVE MAINTENANCE

Corrective maintenance will generally be restricted to replacing defective components, such as resistors, capacitors, diodes, transistors, and IC's, replacing missing hardware, and to tightening loose hardware. In tightening screws, nuts, etc., DO NOT use excessive force.

When replacing components on a printed-circuit board, be sure that the board is not damaged by excessive heating. When unsoldering leads, grip the lead to be unsoldered with a tool that also acts as a heat sink. Heat the solder joint as little as possible while maintaining a pull on the component lead to assure prompt removal of the lead. Use a solder puller to remove excess solder from the board. DO NOT redrill holes in the printed-circuit board. When the integrity of a plated-through hole is in doubt, solder the component lead on both sides of the board.

5.4 TEST POINTS AND VOLTAGES

The nominal values of supply voltages +V, -V, and -V' in this module are as follows:

+V = +5.00 V dc

-V = -5.25 V dc

-V' = -6.00 V dc

Digital modules, unlike analog modules, operate in only the on state or the off state. Therefore, with the exceptions of the transistor circuitry in the 24 Data Converters, the Strobe Circuit , the Reset Buffer, the Data Latch Reset Generator, and the Strobe Input Block Latch Reset Generator, all voltages will be either zero volts or one of the supply voltages listed above. The voltage at any point depends on the function of the transistor or integrated circuit and its input.

5.5 PERFORMANCE TESTING

The following test procedure is considered sufficient to determine whether the C124 is in operating condition.

CORRECT READING OF INPUT DATA WORD

1. With the Module installed in a CAMAC crate, connect a source of NIM-standard negative fast logic signals that is capable of generating any desired 24-binary-bit data word in parallel form to the 24 front panel Data signal input connectors.

2. Connect a source of NIM-standard negative fast logic Strobe signals that can be manually triggered to one of the front panel Strobe signal input connectors.

3. Connect a 50Ω termination to the unused front panel Strobe signal input connector.

4. Connect a source of NIM-standard negative fast logic Reset signals that can be manually triggered to the front panel Reset connector.

5. With CAMAC crate power applied to the module, send any desired 24-binary-bit data word to the module and strobe it through to the inputs of the 24 Output Gates.

6. Send $N_{(module)} \cdot F(0) \cdot A(0)$.

7. Verify that the data word read in Step 6 was the same data word as that sent to the module in Step 5 and that the Dataway Q-line Response signal was generated.

8. In order to verify that the Data signal latches remained set, repeat Steps 6 and 7.

9. In order to verify that the Strobe signal input inhibit latches were reset, send the binary complement of the data word sent in Step 5 to the module and strobe it through to the inputs to the 24 Output Gates.

10. Send $N_{(module)} \cdot F(0) \cdot A(0)$.

11. Verify that a data word consisting of all binary 1's was read in Step 10 and that the Dataway Q-line Response signal was generated.

12. Verify that the signals are at the rear connector.

CORRECT READING AND CLEARING OF INPUT DATA WORD

1. With the data word that was read in Step 10 of the previous section still latched at the inputs to the Output Gates, send $N_{(module)} \cdot F(2) \cdot A(0)$.

2. Verify that a data word consisting of all binary 1's was read in Step 1 and that the Dataway Q-line Response signal was generated.

3. Send $N_{(module)} \cdot F(0) \cdot A(0)$.

4. Verify that a data word consisting of all binary 0's was read in Step 3 and that the Dataway Q-line Response signal was generated.

5. Verify that the signals on the rear connector have been reset.

CLEARING OF INPUT DATA WORD

1. Send any desired 24-binary-bit data word other than those previously used to the module and strobe it through to the inputs to the 24 Output Gates.

2. Send $N_{(module)} \cdot F(9) \cdot A(0)$.

3. Verify that no data word was read in Step 2 and that no Dataway Q-line Response signal was generated.

4. Send $N_{(module)} \cdot F(0) \cdot A(0)$.

5. Verify that a data word consisting of all binary 0's was read in Step 4 and that the Dataway Q-line Response signal was generated.

6. Send any desired 24-binary-bit data word other than those previously used to the module and strobe it through to the inputs to the 24 Output Gates.

7. Send $N_{(module)} \cdot F(0) \cdot A(0)$.

8. Verify that the data word read in Step 7 was the same as that sent to the module in Step 6.

REACTION TO DATAWAY C- AND Z-LINE SIGNALS

1. There should now be a 24-binary-bit data word latched at the inputs to the 24 Output Gates. Send the Dataway C-line Clear signal.

2. Verify that the Dataway Q-line Response signal was not generated.

3. Send $N_{(module)} \cdot F(0) \cdot A(0)$.

4. Verify that a data word consisting of all binary 0's was read in Step 3 and that the Dataway Q-line Response signal was generated.

5. Send any desired 24-binary-bit data word other than those previously used to the module and strobe it through to the inputs of the 24 Output Gates.

6. Send the Dataway C-line Clear signal.

7. Verify that the Dataway Q-line Response signal was not generated.

8. Send the binary complement of the data word sent in Step 5 to the module and strobe it through to the inputs of the 24 Output Gates.

9. Send $N_{(module)} \cdot F(0) \cdot A(0)$.

10. Verify that the data word read in Step 9 is the binary complement of that sent to the module in Step 5 and that the Dataway Q-line Response signal was generated.

11. Verify that the rear panel signals are reset.

12. Repeat Steps 1 through 11, except send the Dataway Z-line Initialize signal, rather than the Dataway C-line Clear signal, in Steps 1 and 6.

13. Clear the module by sending the Dataway Z-line Initialize signal.

RESPONSE TO NIM-STANDARD NEGATIVE FAST LOGIC RESET SIGNAL

1. Send any desired 24-binary-bit data word other than those previously used to the module and strobe it through to the inputs to the 24 Output Gates.

2. Send $N_{(module)} \cdot F(0) \cdot A(0)$.

3. Verify that the data word read in Step 2 is the same as that sent to the module in Step 1 and that the Dataway Q-line Response signal was generated.

4. Repeat Steps 1 through 11 of the section concerning RESPONSE TO DATAWAY C- AND Z-LINE SIGNALS, except send the NIM-standard negative fast logic Reset signal, rather than the Dataway C-line Clear signal, in Steps 1 and 6 of that section.

5. Clear the module by sending the NIM-standard negative fast logic Reset signal.

REACTION OF INHIBIT CIRCUITRY

1. Send any desired 24-binary-bit data word other than those already used to the moduel and strobe it through to the inputs to the 24 Output, gates.

2. Send $F(0) \cdot A(0)$. (wrong station number or N = 0).

3. Verify that a data word consisting of all binary 0's was read in Step 2 and that the Dataway Q-line Response signal was not generated.

4. Clear the module by sending the Dataway C-line Clear signal.

5. Repeat Steps 1 through 4 six (6) times, sending successively in Step 3 $N_{(module)} \cdot F(4) \cdot A(0)$, $N_{(module)} \cdot F(16) \cdot A(0)$, $N_{(module)} \cdot F(16) \cdot A(0)$, $N_{(module)} \cdot F(0) \cdot A(1)$, $N_{(module)} \cdot F(0) \cdot A(2)$, $N_{(module)} \cdot F(0) \cdot A(4)$, and $N_{(module)} \cdot F(0) \cdot A(8)$.

6. REPLACEABLE PARTS

This section contains information needed for ordering spare and/or replacement parts. Table 6.1 lists the parts by their reference designator numbers as shown on the schematic diagram and indicates the description of the part and the part number.

6.1 ORDERING INFORMATION

All written inquiries concerning spare and/or replacement parts and all orders for same should be addressed to the Customer Service Department at 100 Midland Road, Oak Ridge, Tennessee 37830. The Manager of Customer Services can be reached by telephone at (615) 482-4411. All written and verbal inquiries concerning spare and/or replacement parts and all orders for same should include the model and serial numbers of the instrument involved. The minimum order that can be accepted for spare and/or replacement parts is $25.00.

6.2 ORDERING INFORMATION FOR PARTS NOT LISTED

In order to facilitate ordering of parts, the following information should be submitted to the Customer Service Department:

1. The instrument model number,
2. the instrument serial number,
3. a description of the part,
4. information as to the function and location of the part.

C 124 Strobed Coincidence

Rear Connector Pin Assignments

Pin #	Assgnmnt.	Pin #	Assgnmnt.
1	24-	26	12-
2	24	27	12
3	23-	28	7-
4	23	29	7
5	22-	30	6-
6	22	31	6
7	21-	32	5-
8	21	33	5
9	1-	34	nc
10	1	35	nc
11	2-	36	19
12	2	37	19
13	3-	38	17-
14	3	39	17
15	4-	40	15-
16	4	41	15
17	nc	42	13-
18	20-	43	13
19	20	44	11-
20	18-	45	11
21	18	46	10-
22	16-	47	10
23	16	48	9-
24	14-	49	9
25	14	50	8-
		51	8
		52	nc