6/16/94

Model CCF8200
CAMAC Octal
Constant-Fraction Discriminator
Operating and Service Manual

Printed in U.S.A.

EG&G ORTEC Part Number 740320
Manual Revision B

3962 0.5C 1189

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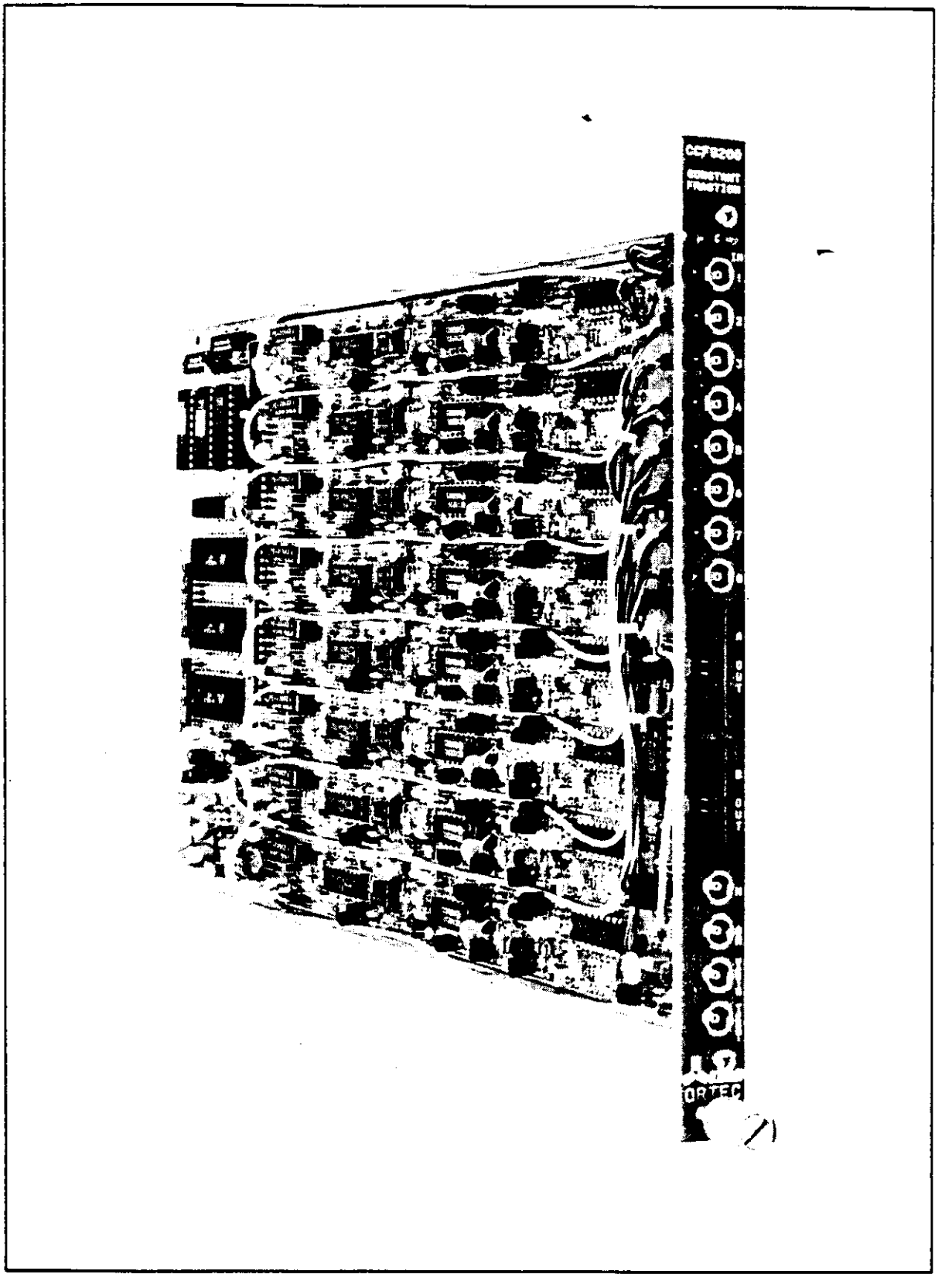
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EG&G ORTEC MODEL CCF8200 CAMAC OCTAL CONSTANT-FRACTION DISCRIMINATOR

1. DESCRIPTION

Packaged in a single-width CAMAC module, the EG&G ORTEC Model CCF8200 Octal Constant-Fraction Discriminator incorporates eight identical channels of constant-fraction timing discriminators, with computer control of input thresholds and output pulse widths. It is a particularly efficient solution for obtaining good time resolution with germanium, silicon, or scintillation detectors in multi-detector experiments involving wide energy ranges. Use of the constant-fraction technique eliminates the severe time shift experienced with simple, leading-edge timing discriminators when the signal amplitude varies over a wide range. In addition, the Model CCF8200 selects the optimum trigger point for minimum time resolution on pulses of all amplitudes.

Several features of the Model CCF8200 offer convenience for multiple-detector experiments. Manual adjustments are eliminated by an automatic walk adjusting circuit, and by computer control of the input thresholds and output pulse widths. An OR output produces a negative fast-NIM logic pulse whenever one or more inputs are triggered. For determination of the multiplicity of the event, the "M" output produces a negative pulse with an amplitude proportional to the number of "B" outputs that are active simultaneously. A VETO input can be used to inhibit outputs on all channels. To test the entire function of each channel, the front-panel test input can be used, or an internally generated test pulse can be triggered by a CAMAC command. A CAMAC programmable output mask permits selection of which channels will be active.

The nuisance of the bulky, external, shaping delay cables normally required with constant-fraction discriminators is eliminated by a compact, internally selectable delay. Each plug-in delay block provides five different delay settings. To cover the requirements of constant-fraction shaping with a variety of detector types, optional plug-in delays are available to cover the range from 1 to 50 ns.

Each channel has an "A" and a "B" output. The leading edge of each output transition precisely defines the arrival time of the input pulse. Complementary ECL outputs are used, with two pins assigned to each output. The "A" outputs from all channels share the 2- by 8-pin "A" connector, and have a common width that is selectable by CAMAC command from 20 to 200 ns. All the "B" outputs are contained in the 2- by 8-pin "B" connector, with their own common width controlled from 20 to 200 ns by a CAMAC command. On both sets of outputs, the width is set with an 8-bit resolution. Figure 1 shows the relationship between the CAMAC command setting and the output pulse width. A red LED beside each input indicates when that channel is responding to an input pulse.

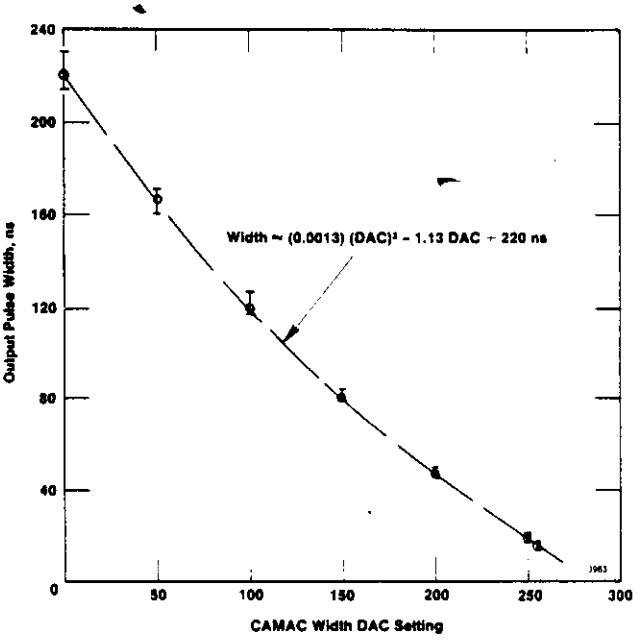

Fig. 1. Output Width Setting vs CAMAC Width DAC Setting.

The input on each channel accepts fast linear signals from the detector in the range of 0 to −5 V. Each input has an associated noise discriminator threshold that is independently adjustable over the range of −25 to −1100 mV, with 8-bit resolution, via a CAMAC command. Figure 2 illustrates the relationship between the CAMAC command setting and the threshold voltage. All CAMAC settings in the module can be read back for verification.

For timing with scintillation detectors and silicon charged particle detectors, the Model CCF8200 is utilized in the conventional, constant-fraction timing mode.[1] The timing fraction of the Model CCF8200 is set at the factory to f = 0.4. Consequently, the internal delay is selected to match the time taken by the detector signal to rise from 40% to 100% of its maximum amplitude. For most scintillation detectors, the 0 to −5 V fast, linear signal from the photomultiplier tube anode can be accepted directly by the 50-Ω input on the Model CCF8200. In the rare cases where the signal amplitude is too small, a fast amplifier may be needed between the anode output and the Model CCF8200 input. With silicon charged- particle detectors a fast amplifier is usually required between the detector

preamplifier output and the Model CCF8200 input. In both cases, the rise time of the amplifier must be fast enough to not degrade the rise time of the detector signal.

With germanium detectors, the Model CCF8200 is used in the amplitude and rise time compensated (ARC) timing mode,[1] in order to minimize the time resolution degradation caused by the variations in the charge collection time of the detector. The internal shaping delay is chosen to optimize the time resolution on the particular detector being used, and is generally in the range from 20 to 50 ns. A timing filter amplifier, such as the EG&G ORTEC Model 863, 474, or 579, is required between the detector preamplifier output and the Model CCF8200 input. Best results are typically obtained with the minimum integration time constant and the maximum differentiation time constant on the timing filter amplifier.

[1] *Principles and Applications of Timing*, Application Note AN-42. EG&G ORTEC, Oak Ridge, Tennessee.

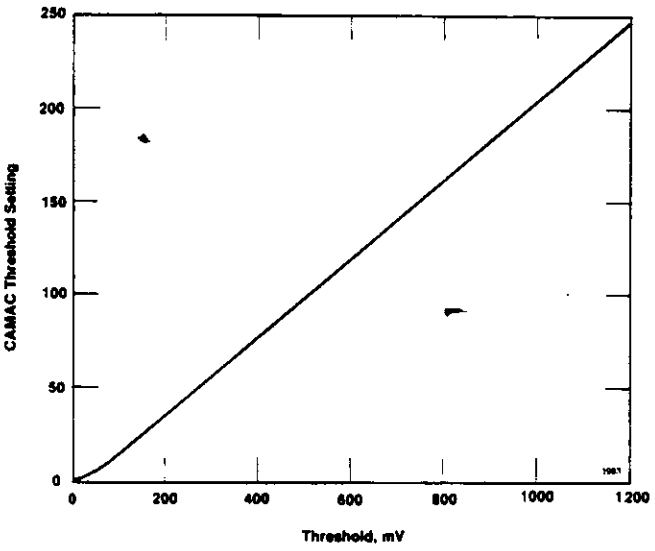

Fig. 2. Threshold Voltage vs CAMAC Threshold DAC Setting.

2. SPECIFICATIONS*

The Model CCF8200 contains 8 duplicate channels with identical functions. Unless otherwise stated, the specifications apply to each channel.

2.1. PERFORMANCE

WALK Typically <±250 ps from −50 mV to −5 V. Measured with an input pulse with a 10-ns width, and 1-ns rise time; a 4-ns delay; and the threshold set at nominally −30 mV (CAMAC setting of 4).

CONSTANT FRACTION RATIO f = 0.4

PULSE-PAIR RESOLUTION <50 ns.

INPUT/OUTPUT RATE >20 MHz.

TRANSMISSION DELAY
"A" Outputs Typically 15 ns.
"B" Outputs Typically 27 ns.

OPERATING TEMPERATURE RANGE 0 to 50°C.

THRESHOLD TEMPERATURE SENSITIVITY
<0.1 mV/°C. Threshold reference is derived from the −24 V supply.

* Specifications subject to change without notice.

2.2. INDICATORS

N Front-panel, green LED indicates when the module has been addressed by the CAMAC bus.

Q Front-panel, yellow LED turns on when the CAMAC command has been accepted by the module.

IN1, IN2, ..., IN8 LEDs Red, front-panel LED flashes when an "A" output has been generated for that channel. (One LED per channel).

2.3. CONTROLS

SHAPING DELAY Internal PCB jumper (1 per channel) selects the proper shaping delay from one of five standard values (2, 4, 6, 8, or 10 ns). Other delay ranges are available as accessories.

THRESHOLD CONTROL Independently variable for each channel via CAMAC command. A plot of threshold voltage vs CAMAC setting is shown in Figure 2. "A" and "B" outputs are generated only for linear input pulses which exceed the threshold setting.

Range Nominally from −25 to −1100 mV.
Resolution 8 bits.

WIDTH ADJUSTMENTS ("A" and "B") All eight "A" output widths have one common control, and all eight "B" output widths have a separate common control. Output pulse widths are set via CAMAC command. A plot of nominal output pulse width vs CAMAC setting is shown in Fig. 1. The "B" outputs are triggered by the leading edges of the "A" outputs, and are also subject to the blocking time set by the "A" output width.
Range Nominally <20 ns to >200 ns.
Resolution 8 bits.

INHIBIT MASK CAMAC command allows blocking of both "A" and "B" outputs for selected channels.

CAMAC TEST CAMAC command generates a single test pulse on the inputs of all eight channels.

CAMAC Function Codes

F(0)*A(0)...A(7)	Read Threshold (1 through 8)
F(1)*A(0)	Read "A" Output Width
F(1)*A(1)	Read "B" Output Width
F(1)*A(2)	Read Inhibit Mask
F(16)*A(0)...A(7)	Write Threshold (1 through 8)
F(17)*A(0)	Write "A" Output Width
F(17)*A(1)	Write "B" Output Width
F(17)*A(2)	Write Inhibit Mask
F(25)*A(0)	Generate Test Signal (on all enabled channels)
F(9)	Clear Module

2.4. INPUTS

IN1, IN2, ..., IN8 Front-panel LEMO connector for each channel accepts the fast linear signal from a detector for constant fraction timing. Linear range from 0 to −5 V. Input impedance 50 Ω, dc-coupled. Input protected with diode clamps to ground and −6 V.

VETO Front-panel LEMO connector accepts negative Fast-NIM signal. Active-low signal (nominally −800 mV) disables all "B" outputs. Input impedance, 50 Ω. Leading edge of the VETO input must occur no later than 8 ns after the leading edge of the linear input signal, and it must overlap the trailing edge of the linear input signal for proper operation.

TEST Front-panel LEMO connector accepts negative Fast-NIM signal. Active-low signal (nominally −800 mV) triggers all enabled channels and produces an output that indicates functionality of the entire discriminator circuit, regardless of threshold setting. Input impedance, 50 Ω.

CAMAC TEST INPUT CAMAC function code F(25)*A(0) generates a single test pulse that triggers all enabled channels and produces an output that indicates functionality of the entire discriminator circuit regardless of the threshold setting.

2.5. OUTPUTS

"A" OUT 2- by 8-pin front-panel connector provides a pair of complementary ECL output logic pulses for each of the 8 channels, starting with the channel 1 output on the top pair of pins. The leading edge of the output transition defines the time of arrival of the input pulse. All "A" outputs have a common blocking width adjustable from <20 ns to >200 ns via CAMAC command.
Rise Time Typically 2 ns.
Fall Time Typically 2 ns.
Amplitude Swing Left pin: nominally from −1.8 V (quiescent state) to −0.9 V; right pin: nominally from −0.9 V (quiescent state) to −1.8 V.
Line Impedance 112 Ω.

"B" OUT 2- by 8-pin front-panel connector provides a pair of complementary ECL output logic pulses for each of the 8 channels, starting with the channel 1 output on the top pair of pins. The leading edge of the output transition defines the time of arrival of the input pulse. All "B" outputs have a common blocking width adjustable from <20 ns to >200 ns via CAMAC command. The "B" outputs are triggered by the leading edges of the "A" outputs, and are also subject to the blocking period set for the "A" outputs.
Rise Time Typically 2 ns.
Fall Time Typically 2 ns.
Amplitude Swing Left pin: nominally from −1.8 V (quiescent state) to −0.9 V; right pin: nominally from −0.8 V (quiescent state) to −1.8 V.
Line Impedance 112 Ω.

MULTIPLICITY OUTPUT (M) Front-panel LEMO connector provides an output pulse whose amplitude is proportional to the number of "B" outputs active at any given instant. A composite waveform showing the M output for 0 to 8 "B" outputs in shown in Fig. 3.

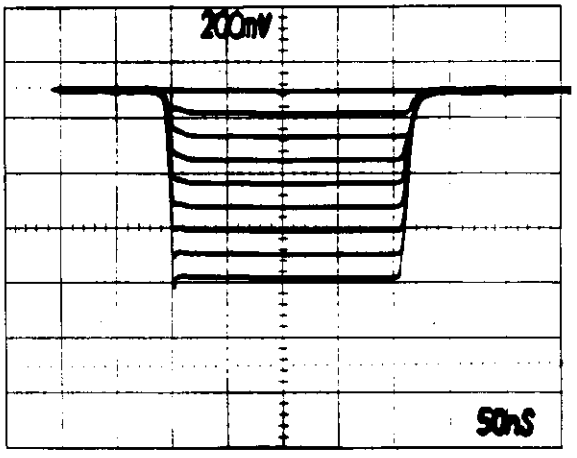

Fig. 3. Multiplicity Output for 0 to 8 "B" Outputs.

Amplitude Range Nominally −90 mV per channel fired (0 to −720 mV). Proper operation requires a 50-Ω termination on the M output.
Rise Time <7 ns.
Fall Time <7 ns.

OR OUTPUT (OR) Front-panel LEMO connector provides OR logic of all "B" outputs. Negative Fast-NIM signal.
Amplitude Nominally 0 mV (quiescent state) to −800 mV (active).
Rise Time <3 ns.
Fall Time <3 ns.

2.6. ELECTRICAL AND MECHANICAL

POWER REQUIRED The Model CCF8200 derives its power from a standard CAMAC crate and power supply. Required dc voltages and currents are: +24 V at 175 mA, +6 V at 1.1 A, −6 V at 2.4 A, −24 V at 60 mA.

WEIGHT
Net 0.5 kg (1.1 lb).
Shipping 1.4 kg (3.1 lb).

DIMENSIONS Standard CAMAC single-width module, 1.6 × 22.1 cm (0.63 × 8.7 in.) front panel.

2.7. ACCESSORIES

Four different plug-in delay options are available, to suit the type of detector being used. Each of the eight channels requires a separate plug-in. The Model CCF8200 comes from the factory with eight of the CFD-DELAY-10ns options installed. For constant-fraction timing with scintillators and silicon detectors, order the optional delay that matches most closely the time for the input pulse to rise from 40% to 100% of its maximum amplitude. For amplitude and rise-time compensated (ARC) timing with Ge detectors order the CFD-DELAY-50ns option.

CFD-DELAY-5ns Delay plug-in for 1, 2, 3, 4, or 5-ns delay settings.

CFD-DELAY-10ns (Standard) Delay plug-in for 2, 4, 6, 8, or 10-ns settings.

CFD-DELAY-30ns Delay plug-in for 6, 12, 18, 24, or 30-ns settings.

CFD-DELAY-50ns Delay plug-in for 10, 20, 30, 40, or 50-ns settings.

3. INSTALLATION

3.1. GENERAL

The Model CCF8200 power requirements must be furnished from a CAMAC standard bin and power supply. The bin and power supply in which the Model CCF8200 will normally be operated is designed for relay rack mounting. If the equipment is rack mounted, be sure that there is adequate ventilation to prevent any localized heating in the Model CCF8200. The temperature of equipment mounted in racks can easily exceed the maximum limit of 50°C unless precautions are taken.

3.2. CONNECTION TO POWER

Prior to inserting the Model CCF8200 into the CAMAC bin, turn off the CAMAC power supply. The power supply can be turned on after all modules are installed into the bin. To be sure of proper operation, check the dc voltage levels of the power supply after all modules have been installed in the bin.

3.3. INPUT CONNECTIONS

Each discriminator channel includes an input connector on the front panel that is terminated internally in 50-Ω. Connect the source of negative input signals to this connector through a 50-Ω coaxial cable and a mating LEMO connector. Any of the eight channels can be provided with an input signal and will operate independently from all other channels.

3.4. TIMING OUTPUT CONNECTIONS

Two ECL outputs are available for each channel, "A" output and "B" output. Both outputs operate in the blocking mode and do not update. Output signals are available on 2 × 8 front-panel ECL connectors. The amplitude swing is nominally −0.9 to −1.8 V with a line impedance of nominally 112 Ω. These ECL signals can be converted to Fast-NIM signals using the EG&G ORTEC Model EC1600 16-Channel ECL/NIM/ECL Converter.

All eight "A" output widths are controlled by a common DAC, and all eight "B" output widths are controlled by a separate common DAC. Both are under CAMAC control and can range in width from <20 ns to >200 ns.

3.5. LOGIC OUTPUT CONNECTIONS

There are two special function logic outputs available on the Model CCF8200. The Multiplicity Output "M" is available at a front-panel LEMO connector and provides a pulse signal whose amplitude is proportional to the number of "B" outputs active at any given instant. The amplitude range is nominally −90 mV per active "B" output or −720 mV when outputs from all eight channels are active. For proper operation, the "M" output must be terminated in 50 Ω.

The logic OR output is available at a front-panel LEMO connector and provides OR logic for all "B" outputs. The OR output is Fast-NIM.

3.6. CF SHAPING DELAY SELECTION

The selection of the CF Shaping Delay is accomplished using an internal PCB jumper to select one of five values (2, 4, 6, 8, or 10 ns). Other delay ranges are available as Accessories. The jumpers are located toward the rear of the module near where the input signal cables connect to the PC board. The jumper position nearest the word "max" is the longest delay setting.

The primary usage of the Model CCF8200 is expected to be in fast timing or counting experiments with scintillators and photomultiplier tubes (PMTs) and Silicon Surface Barrier Detectors. In these applications, the CF Shaping Delay is selected equal to the time required for the input signal to rise from 40% of its maximum amplitude to 100% of its maximum amplitude. However, selection of the CF Shaping Delay for best timing performance with a given detector system is usually accomplished experimentally.

The CCF8200 can be used with germanium detectors for amplitude and rise-time compensated (ARC) timing. The detector preamplifier signal is amplified by a Timing Filter Amplifier (e.g., EG&G ORTEC Model 863, 474, or 579) before being supplied to the Model CCF8200 input. Typically, the amplifier control should be set for minimum rise time and maximum fall time of the output pulse. The delay in the Model CCF8200 should be in the range of 20 to 40 ns. For further details on optimum settings, consult the EG&G ORTEC Application Note AN-42, *Principles and Applications of Timing Spectroscopy*.

3.7. WALK SETTING

The Model CCF8200 Walk Adjustment is factory set to provide optimum performance over a 100:1 dynamic range of input signals with fast rise times (see 2.1. Performance Specifications). Under most operational conditions, the internal walk adjustment (potentiometer R30) on the circuit board will not need adjustment.

4. OPERATING INSTRUCTIONS

4.1. GENERAL

The actual timing performance of a timing system depends on many variables. The type of detector and the energy range of interest are two important system variables that are independent of the electronics. In general, detectors having fast rise time signals and higher energies give the best timing performance.

4.2. THRESHOLD ADJUSTMENT

The Model CCF8200 threshold is under CAMAC control. Using the CAMAC command F(16)*A(0)...A(7), the threshold of each channel can be independently set over the nominal range of −25 to −1100 mV with 8-bit resolution. The threshold of any channel can be read using the CAMAC command F(0)A(0)...A(7).

A plot of threshold voltage vs CAMAC THRESHOLD setting is shown in Fig. 1. For threshold settings >100 mV, the threshold in mV can be approximated by the formula:

$$\text{Threshold} \sim 4.8(\text{CAMAC THRESHOLD}) + 24\ \text{mV} . \quad (1)$$

For Threshold settings <100 mV, the threshold in mV can be approximated by the formula:

$$\text{Threshold} \sim 5.3(\text{CAMAC THRESHOLD}) + 9\ \text{mV} . \quad (2)$$

Equations (1) and (2) are generally accurate to ±5 mV or ±5%, whichever is larger.

When a given threshold is required, the CAMAC THRESHOLD setting can be estimated by Equations (3) or (4). For threshold settings >100 mV,

$$\text{CAMAC THRESHOLD} \sim 0.21\ (\text{Threshold in mV}) - 5 . \quad (3)$$

For threshold settings <100 mV,

$$\text{CAMAC THRESHOLD} \sim 0.19\,(\text{Threshold in mV}) - 1.7\ . \quad (4)$$

Although it is possible to set the Model CCF8200 Threshold DAC to 0, this will result in an unstable condition with the threshold operating in the noise. The minimum usable threshold is nominally −25 mV, which corresponds to CAMAC DAC setting of 3.

4.3. OUTPUT WIDTH ADJUSTMENT

The Model CCF8200 output width is under CAMAC control. The "A" output width is set using the CAMAC command F(17)*A(0), and the "B" output width is set using the CAMAC command F(17)*(A1). The setting for the "A" output width can be read using the CAMAC command F(1)*A(0) and the setting for the "B" output width can be read using the CAMAC command F(1)*A(1).

All eight "A" outputs have a common control and all eight "B" outputs have a separate common control. The range of both outputs is from <20 ns to >200 ns with 8-bit resolution. A plot of output width vs CAMAC DAC setting is shown in Fig. 2. The output width can be approximated by the formula:

$$\text{Width} \sim 0.0013(\text{DAC})^2 - 1.13(\text{DAC}) + 220\ \text{ns}\ . \quad (5)$$

Equation (5) is generally accurate to ± 3ns or ±5%, whichever is larger.

When a given output width is required, the CAMAC DAC setting can be estimated by Equation (6) as:

$$\text{Width DAC Setting} \sim 0.0027(\text{Width})^2 - 1.86(\text{Width}) + 284 \quad (6)$$

4.4. INHIBIT MASK

The Model CCF8200 can turn off selected channels via CAMAC command using the Inhibit Mask. This feature allows computer controlled reconfiguration of an experiment without hardware changes.

The CAMAC command F(17)*A(0) will write the Inhibit Mask. Both "A" and "B" outputs are controlled by the Inhibit Mask. The CAMAC command F(1)*A(2) is used to read the Inhibit Mask.

The specific mask setting is determined by the data sent with the F(17)*A(0) command. If all eight bits are set to "1", all eight channels are inhibited. If the data is 01001101, channels 1, 3, 4, and 7 are inhibited.

4.5. VETO INPUT

The Model CCF8200 has a front-panel LEMO connector that can accept a negative Fast-NIM VETO input signal. An active-low signal (nominally −800 mV) disables all "B" output signals but does not affect any of the "A" output signals. For proper operation, the leading edge of the VETO input must occur no later than 8 ns after the leading edge of the input signal and it must overlap the trailing edge of the input signal.

4.6. TEST INPUT

The Model CCF8200 has two methods for testing the functionality of the unit. A front-panel LEMO connector accepts negative Fast-NIM signals. The active-low signal triggers all enabled channels and produces an output that indicates functionality of the entire discriminator circuit regardless of threshold setting. Both "A" and "B" outputs as well as the front-panel event LED will be present for each enabled channel.

The Model CCF8200 also will accept the CAMAC command F(25)*A(0) that generates a single test input signal that triggers all enabled channels regardless of threshold setting. Both "A" and "B" outputs as well as the front-panel event LED will be present for each enabled channel.

5. THEORY OF OPERATION

5.1. GENERAL

A complete schematic of the EG&G ORTEC Model CCF8200 CAMAC Octal Constant-Fraction Discriminator, Drawing Number 755070 (2 sheets), is included at the back of this manual. Also included is a component assembly drawing, Drawing Number 755350. On this documentation, note that corresponding components in each channel have the same reference designator. Components within a given channel have a prefix designator for that channel. Thus 1R1 corresponds to resistor R1 in Channel 1, while 8R1 corresponds to the same resistor in Channel 8. Components common to all channels, such as the CAMAC controller, OR and Multiplicity Outputs, have three-digit component designations without a prefix. For example, resistor R101 is part of the Test Input Circuit common to all eight channels.

5.2. DIGITAL CIRCUITRY

Most of the common circuits for the Model CCF8200 are shown on sheet 1 of 2 of the schematic. DC power is taken from the CAMAC crate and filtered. V_{CC} for the TTL devices is derived from +6 V with diode D110 dropping the voltage to +5 V. The ±15 V supplies for the op amps are derived from ±24 V using three terminal regulators U120 and U121. A stable $+5V_{REF}$ and $-5V_{REF}$ are formed by U118 and U119 and their associated circuitry.

Three PALs, U104, U105 and U106, contain the internal state machine of the CCF8200. These PALs convert the various CAMAC commands into the required internal signals for the CCF8200. Three 8-bit DACs, U107, U108 and U109, convert the digital information into analog signals. Op amps U115, U116 and U117 convert the DAC current outputs to voltage outputs and drive the individual channels. The CAMAC Read and Write buses are buffered from the CCF8200 by U102 and U103.

The width of the "A" outputs are set by the voltage on the T1 bus, which is set by U117(1). The width of the "B" outputs are set by the voltage on the T2 bus, which is set by U117(14). Both these voltages are under CAMAC control.

5.3. TIMING CIRCUITRY

The timing circuitry of the Model CCF8200 is shown on sheet 2 of the schematic. The negative input signal is applied to the Input connector. Diodes D1 and D2 and resistor R1 provide input protection against overload signals.

The input signal is split into two parts at the junction of D1 and D2. Resistors R2 and R3 attenuate the input signal and connected to the "+" input of U1A. The full amplitude signal is delayed by the lumped constant delay line DL1 and connected to the "–" input of U1A. The constant-fraction signal is formed internal to U1A and appears as a negative-going ECL signal at U1A(2). The constant-fraction logic output is available for viewing at Test Point TP2.

The full amplitude input signal is also connected to the "–" input of U1B which operates as a leading edge discriminator. The output at U1B(15) is "wire-ANDed" with the constant-fraction output at U1A(2) to produce the constant-fraction timing output.

The threshold control voltage derived in the digital circuitry is connected to U1B(9) after filtering by C3 and R11. Resistor R14 provides hystereses to prevent multi-pulsing near threshold.

The Model CCF8200 employes a gated walk circuit to reduce time shift as a function of varying input signal rates. The gating element is U2 whose output is disabled when the leading edge discriminator, U1B, changes state. Transistors Q1 and Q2 translate the ECL signal to that required by U2. Resistor R30, a PCB potentiomenter, provides walk adjustment.

The constant-fraction timing output signal at U1(2,15) is negative-going. The pulse transformer T1 inverts this signal and clocks the fast flip-flop U3B.

The "A" output signal is derived from the U3B(14) output, buffered by the line driver U4B. The width of the "A" output is set by the circuitry associated with Q4 through Q7. When U3B is clocked, a negative-going ramp begins at Q5E. When this ramp signal crosses the T1 bus voltage at Q7B, Q6-Q7 switch and generate the reset pulse at U3B(12). Changing the width of the "A" output requires changing the voltage of the T1 bus, which is derived in the Digital Circuitry under CAMAC control.
The output of U3B, and hence both the "A" outputs and the "B" outputs, can be blocked at U3B(10) by the Inhibit Mask signal from the Digital Circuitry.

The front-panel event LED is triggered by the signal at U3B(15). The line driver U4C and associated circuitry form a one-shot of nominally 20 ms duration to drive the event LED. This is an updating one-shot.

The signal U3B(15) is also used to clock the fast flip-flop U3A. The "B" output signal is derived from U3A(2) buffered by the line driver U4A. The width of the "B"

output is set by the circuitry associated with Q8 through Q11 and is similar to the circuity used to set the "A" output pulse width. When U3A is triggered, a negative-going ramp begins at Q9E. When this ramp signal crosses the T2 bus voltage at Q11B, Q10-Q11 switch and generate the reset pulse at U3A(4). Changing the width of the "B" output requires changing the voltage of the T2 bus which is derived in the Digital Circuitry under CAMAC control.

The Multiplicity Output is derived from the "B" output signal at U3A(3). Resistor R59 from each channel connect at R116, which is a low impedance point due to Q106E. The summed signals are level shifted by Q106-Q107 and available at the front-panel LEMO "M" output. For proper operation, the "M" output must be terminated in 50-Ω.

The OR Logic Output is also derived from the "B" output signal at U3A(2). U101 serves as an eight-input OR gate and transistors Q104-105 shift the ECL output from U101 to a fast-NIM signal.

5.3. TEST INPUT CIRCUITRY

The Model CCF8200 has provisions for two forms of test input. The front-panel LEMO connector accepts Fast-NIM signals. Transistors Q101 through Q103 convert this input into a positive-going pulse at Q101C. This positive pulse turns on diodes D3 and D4 causing both U1A and U1B to change state and form a timing signal output at U1(2,15). This signal will produce both "A" and "B" outputs and light the front-panel event LED provided that the channel is not blocked by the Inhibit Mask at U3B(10).

The CAMAC test signal operates in a similar manner except that it is a positive signal and is applied to Q103B. All other functions are the same as for the Fast-NIM Test input.

6. MAINTENANCE

6.1. CALIBRATION

There are only two adjustments internal to the Model CCF8200. Each channel has a Walk Adjustment, R30, which can be optimized for a given timing application. This potentiometer is factory set with a 10-ns-wide input signal having a 1-ns rise and fall time. With the Threshold set to nominally −30 mV, the input signal is varied from −50 mV to −5 V using a precision attenuator (Hewlett-Packard Model HP8496B with <±10 ps time walk). R30 is adjusted to minimize the time shift of the CCF8200 output.

The second internal adjustment in the CCF8200 is R117, which controls the amplitude and pulse shape of the Multiplicity Output. This potentiometer should not need field adjustment.

6.2. TYPICAL DC VOLTAGES

All voltages listed on the schematic drawing are measured with respect to ground with the Threshold and Width set to minimum.

6.3. FACTORY SERVICE

This instrument can be returned to the EG&G ORTEC factory for service and repair at a nominal cost. The EG&G ORTEC standard procedure for repair ensures the same quality control and checkout that are used for a new instrument. Always contact Customer Services at EG&G ORTEC before sending an instrument for repair to obtain shipping instructions and so the required Return Authorization Number can be assigned to the unit. This number should be written on the address label and on the package.