

Technical Data

S424B Quad Scaler

September 1972

- 24-bit Scaler
- Data inputs protected against ± 50 -V fast transients ($\leq 1 \mu\text{sec/sec}$)
- Data inputs from dc to 150 MHz
- 2-connector bridging Inhibit input circuit
- Inhibit signal does not increment Scaler
- LAM generated on overflow
- Overflow or Carry output available
- LED monitors module Inhibit

The S424B is a 24-bit CAMAC Quad Scaler consisting of 4 scalers packaged in a shielded single-width module built per USAEC TID-25875 specifications. The **inputs are protected** against **fast transients** up to ± 50 V and against dc levels up to ± 3.5 V dc. The input circuits respond to signals of at least 3-nsec duration. The S424B has a typical **operating speed of 150 MHz**, with continuous operation at 125 MHz guaranteed.

A front panel locking toggle switch has two positions for selecting the source of the Inhibit signal: In the Both position either the front panel or the CAMAC Dataway I-line Inhibit signal will perform the inhibit function; in the Front position the CAMAC Dataway I-line Inhibit signal is disabled. **Two-connector high-impedance bridging Inhibit input circuit** on the front panel allows the Inhibit signal to be reused.

The input signal is differentiated to allow proper counting of slow (to dc) pulses. **The Inhibit signal will not increment the Scaler** if the data input is true and the Inhibit signal is pulsed on and off.

The S424B has many options for overflow detection. The user may select, by means of internal switches, one option from group 1 and one option from group 2:

1. If **LAM** is to be used for **overflow detection**, the LAM status bit may be connected to:

- a. the overflow of the 23rd bit, or
- b. the overflow of the 24th bit.

2. If the **24th bit** of the Scaler is to be used for overflow detection, the 24th bit **is latched on setting or is buffered** and made available for external use. The 24th bit:

- a. will set when the 23rd bit carries, and will remain set regardless of the number of 23-bit carries, or
- b. will toggle normally, and is available (buffered TTL) on the rear of the printed-circuit board.

The LAM status bits are read by F(1):A(12). If enabled by F(26):A(12), this bit will cause a LAM when set.

S424B
QUAD
SCALER

INHIBIT



SPECIFICATIONS

INPUTS

DATA INPUTS

In 0-In 3 LEMO connectors, 50Ω terminated with <10% reflection; dc-coupled. Protected against ±50-V fast transients; to maximum of ±3.5 V dc. Minimum input: 3 nsec; 2 nsec typical measured at the half-height point on a -600-mV peak-amplitude pulse. Input pair resolution typically 6 nsec, and module will correctly count a burst with ≥7-nsec leading-edge to leading-edge spacing. Typical maximum continuous operating rate, 150 MHz; guaranteed continuous operation, 125 MHz. Threshold, -350 mV ± 50 mV.

CONTROL INPUT

Inhibit High-impedance dc-coupled bridging type, with reflections <20% (unused connector terminated in 50Ω); LEMO connector. Threshold, -350 mV ± 50 mV. Protection, +1.5 V to -4 V. Minimum input: <5 nsec measured at the half-height point on a -600-mV peak-amplitude pulse. A single pulse of a 150-MHz burst can be inhibited. Timing: Inhibit pulse should precede data input pulse by ~5 nsec.

CONTROLS AND INDICATORS

INHIBIT SWITCH Front panel 2-position locking toggle switch selects source of Inhibit signal:

Both Either the front panel Inhibit signal or the CAMAC Databay I-line Inhibit signal will inhibit the counting processes of all 4 scalers.

Front The CAMAC Databay I-line Inhibit signal is disabled, but the front panel Inhibit signal is left enabled; only the front panel Inhibit signal will inhibit the counting processes of all 4 scalers.

RESET Push-button switch to reset all 4 scalers, but not LAM status bits or LAM mask.

INHIBIT LED Monitors Inhibit status of Scaler; if LED is illuminated, Scaler cannot count.

N LED Illuminated when module is addressed.

CAMAC CODES

F(0)-A(k) Read Scaler specified by subaddress; k = 0, 1, 2, 3.

F(1)-A(12) Read LAM status register; may be the 25th bit if proper options are selected.

F(2)-A(k) Read and clear Scaler and LAM status bit specified by subaddress; k = 0, 1, 2, 3.

F(8)-A(12) Test LAM.

F(9)-A(k) Clear register and LAM status bit specified by subaddress; k = 0, 1, 2, 3.

F(10)-A(k) Clear LAM status bit specified by subaddress; k = 0, 1, 2, 3.

F(24)-A(12) Disable LAM.

F(25) Increment all scalers.

F(26)-A(12) Enable LAM.

C and Z Clear and initialize resets all sections to zero on leading edge of S2 and disables LAM. Reset time, 300 nsec.

I Databay Inhibit line inhibits all scalers from counting when front panel switch is in Both position.

Q Q = 1 is sent for all above function codes except F(8) with proper N and A. For F(8) and proper N and A, Q = LAM status bit.

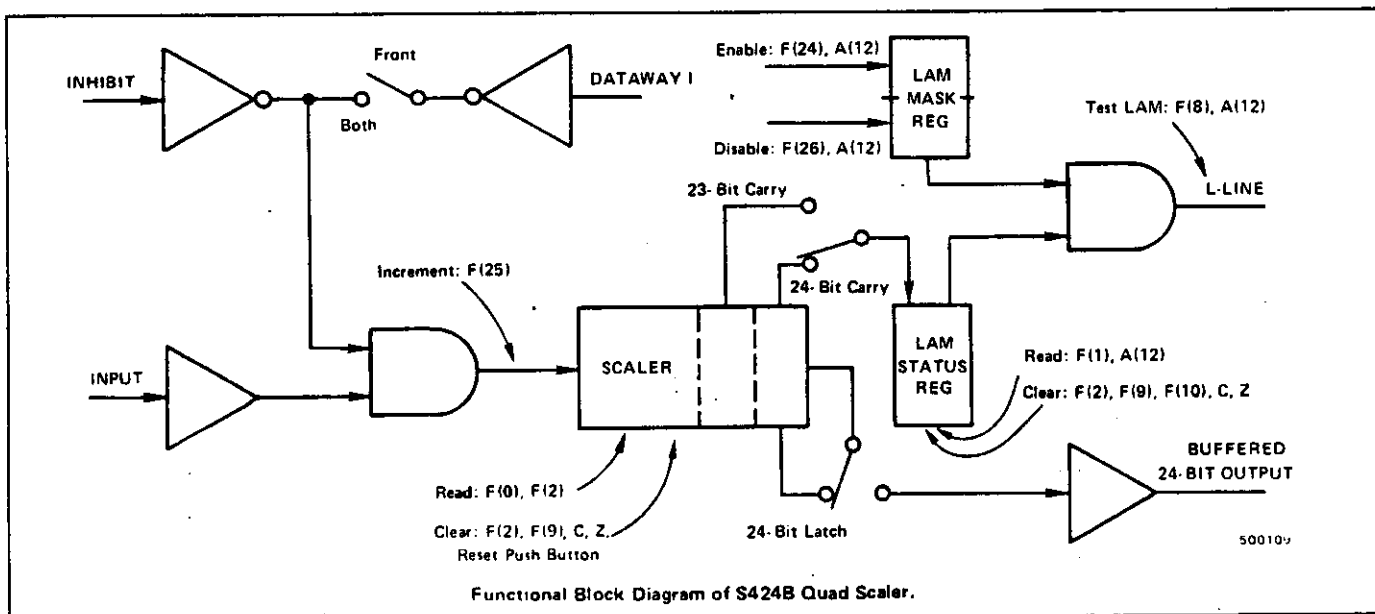
X Function accepted line; X = 1 is sent for all above function codes with N and A.

ELECTRICAL AND MECHANICAL

POWER REQUIRED

-6 V, 650 mA;
+6 V, 650 mA.

DIMENSIONS Single-width module per TID-25875 (17.2 mm x 222.25 mm x 290 mm).



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Scalable
Controlled
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