EG&G/ORTEC

HIGH ENERGY PHYSICS

Operating and Service Manual

TD811
CAMAC
Time Digitizer

This manual applies to instruments
"Rev 00" (on rear panel)

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ORTEC/EG&G TD811 TIME DIGITIZER MANUAL

1. DESCRIPTION

The TD811 Octal Time Digitizer contains eight precision time-to-digital converters that are coupled to a common start input for measuring time intervals over a range of 0 to 200 ns with a resolution of 100 ps.

A valid start is a pulse that is accepted through the Start input when the TD811 is in a reset status. On receipt of a valid start the stop inputs are rapidly enabled and an internal busy latch is set (which may be tested by CAMAC command). Stop signals can be accepted within 200 ns after the valid start and each stop signal signals a normal conversion in its channel.

At the leading edge of the valid start input, eight separate timing capacitors begin to charge with constant current. Each capacitor continues to charge until a stop pulse arrives at its input; then it discharges at a much slower rate. If no stop is furnished within 200 ns, an internal timer simulates a stop and the measurement will be overrange. This limits the converter circuit and reduces recovery time. For each channel in which the stop input was received within the 200-ns time range, the time is converted to a charge; an internal clock is gated to a scaler through both the charge and discharge intervals to accumulate the measurement that is temporarily stored in the scaler.

The Time Digitizer is designed with a 90-μs fixed conversion time, which is independent of the start-to-stop period and provides full LAM logic. At the completion of the conversion cycle, the unit generates a LAM service request by setting a LAM status bit. The LAM may be controlled at the module level by an enable/disable latch and can be tested by CAMAC command in accordance with recommended practice.

If it is desired to abort the conversion cycle, a front panel fast Clear input may be used at any time during the first 70 μs of the 90-μs conversion interval and total reset will be accomplished within 1 μs from the leading edge of the Clear signal. The Time Digitizer is then ready to accept another start signal. After the 70-μs time window has elapsed, the Clear input is blocked and the normal conversion cycle will be completed.

A Veto input is included to achieve fast gating of the start input signal. If veto is used, it must overlap the valid start signal to prevent a response in the TD811.

Each scaler contains 11 valid data bits and a 12th bit that is used to indicate overrun in that section. The scaler capacity, using the 11 valid bits, is 2047 units of time (100 ps/time unit). The accumulated data for each measurement is stored in its register for subsequent readout through the CAMAC Dataway.

The module can be tested externally by use of the common stop input. All eight registers will then contain measurements of the same start-to-stop interval. If computer testing is desired, the module will respond to the CAMAC F(25) command; this furnishes a start input and no stop input so all eight scalers will overrun and set the 12th bit, and the module then generates a request for service.

The TD811 may be blocked by either the internal busy latch or a Dataway inhibit signal. An indicator marked "B" on the front panel lights to show that the input is blocked, and start inputs are rejected.

An indicator marked "N" on the front panel lights to show when the unit is being addressed in the CAMAC system.

2. SPECIFICATIONS

2.1. DATA

Start Input One per module common to all sections; accepts NIM fast negative logic signals ≥5 ns (preferably <10 ns); Z_{in} 50Ω, dc coupled; protected to ±5 V dc.

Stop Inputs, 0 to 7 Eight front panel connectors, one per channel; each accepts NIM fast negative logic signals ≤5 ns to terminate the time interval for its section; Z_{in} 50Ω, dc coupled; protected to ±5 V.

Common Stop One per module common to all sections for dynamic test function; accepts NIM fast negative logic signals ≥5 ns to terminate the time interval for all sections simultaneously; Z_{in} 50Ω, dc coupled; protected to ±5 V; typical timing +5 ns relative to single stop input.

2.2. LOGIC

Veto One front panel connector per module, common to all sections; accepts NIM fast negative logic signals ≥5 ns to

block the start input; must overlap start signal; Z_{in} 50Ω, dc coupled; protected to ±5 V; response rise 3 ns and decay 15 ns.

Clear One front panel connector per module, common to all sections; accepts NIM fast negative logic signals ≥5 ns to cancel conversion and reset the unit without LAM; must be furnished <70 μs after valid start; Z_{in} 50Ω, dc coupled; protected to ±5 V.

2.3. OUTPUTS

Data 11 bits per channel onto CAMAC read lines R1 through R11, per TID-25875.

Overflow Indicated by bit onto CAMAC read line R12. Jumper provisions included to furnish this bit onto CAMAC read line R16.

2.4. INDICATORS AND CONTROL

B Indicator lights when module is blocked and cannot accept a start input.

N Indicator lights when module is being addressed in the CAMAC system.

Calibrate Eight internal potentiometers, one per channel, calibrate the effective conversion for each channel.

2.5. PERFORMANCE

Full Scale Time Range 4 to 200 ns, using 11 binary bits.

Calibration 100 ps/bit.

Resolution 100 ps.

Integral Nonlinearity ±0.1% (10% to 100% of full scale).

Differential Nonlinearity ±2% (10% to 100% of full scale).

Conversion Time ~90 μs; all channels in parallel.

Temperature Coefficient ≤±0.02%/°C (0 to 50°C).

2.6. CAMAC CODES

F(0)·A(k) (k = 0 to 7) read selected register.

F(2)·A(k) (k = 0 to 6) read selected register.

F(2)·A(7) Read register 7; clear all registers, busy, and LAM.

F(8)·A(12) Test LAM; Q = LAM.

F(10)·A(12) Clear LAM.

F(11)·A(12) Clear all registers, busy, and LAM.

F(24)·A(12) Disable LAM.

F(25)·A(k) (k = 0 to 7) test all registers. This triggers a simulated start and an overrun stop internally in the module to test response in all sections.

F(26)·A(12) Enable LAM.

F(27)·A(12) Test busy; Q = busy.

C Clears all data registers, busy, and LAM status.

Z Clears all data registers, busy, and LAM status, and disables LAM.

I Inhibits operation of all sections.

Q Returned for all F·A function codes except F(8)·A(12) and F(27)·A(12) where the Q response is conditional.

X Returned for all F·A function codes.

2.7. POWER REQUIRED

Maximum +6 V, 520 mA; −6 V, 720 mA; +24 V, 85 mA; −24 V, 55 mA.

3. OPERATION

3.1. INSPECTION AND INSTALLATION

After carefully unpacking the unit, thoroughly inspect it for evidence of damage in shipment. If it has been damaged, refer to the Warranty in the front of this manual for further instructions.

CAUTIONS

Always ensure that CAMAC crate power is turned off before installing or removing any CAMAC module.

Always ensure that all pins on the CAMAC Dataway connector on the rear panel are clean before installing any CAMAC module in its crate.

Never use excessive force in installing or removing any CAMAC module.

3.2. SIGNAL CONNECTION AND APPLICATION OF POWER

Note: 50Ω coaxial signal leads with LEMO connectors (male) are required for front panel connections to this unit.

Connect a signal lead to the start input that is common to all sections. Connect the proper signal lead to each of the stop inputs (front panel labeled Stop 0 through Stop 7) that is to be used. No further connections are required.

Turn on the CAMAC crate power. The unit should now be ready for performance testing (see Section 5.5).

3.3. SIGNAL CONNECTIONS

Table 3.1 summarizes the signal connections and their functions.

Table 3.1. Signal Connections.

Connector	Function	Connector	Function
Veto	Accepts NIM-standard negative signal to block the start input.	Common Stop	Accepts NIM-standard negative signal to terminate the time interval measured in all sections, 0 to 7.
Stop 0	Accepts NIM-standard negative signal to terminate the time interval measured in section 0.	Stop 4	Accepts NIM-standard negative signal to terminate the time interval measured in section 4.
Stop 1	Accepts NIM-standard negative signal to terminate the time interval measured in section 1.	Stop 5	Accepts NIM-standard negative signal to terminate the time interval measured in section 5.
Stop 2	Accepts NIM-standard negative signal to terminate the time interval measured in section 2.	Stop 6	Accepts NIM-standard negative signal to terminate the time interval measured in section 6.
Stop 3	Accepts NIM-standard negative signal to terminate the time interval measured in section 3.	Stop 7	Accepts NIM-standard negative signal to terminate the time interval measured in section 7.
Start	Accepts NIM-standard negative signal to start the time intervals measured in all sections, 0 to 7.	Clear	Accepts NIM-standard negative signal within 70 μs after valid start to cancel the measurement and reset the unit within 1 μs.

4. FUNCTIONAL DESCRIPTION

Refer to Figs. 4.1 through 4.4, Table 4.1, and schematic TD811-0101-S1, included at the back of the manual. For identification of individual portions of multielement integrated circuits, an output terminal number can be used to specify a selected portion. For example, IC802(9) or IC802(15) identifies the portion of IC802 that uses terminals 9 and 15 as the two complementary outputs.

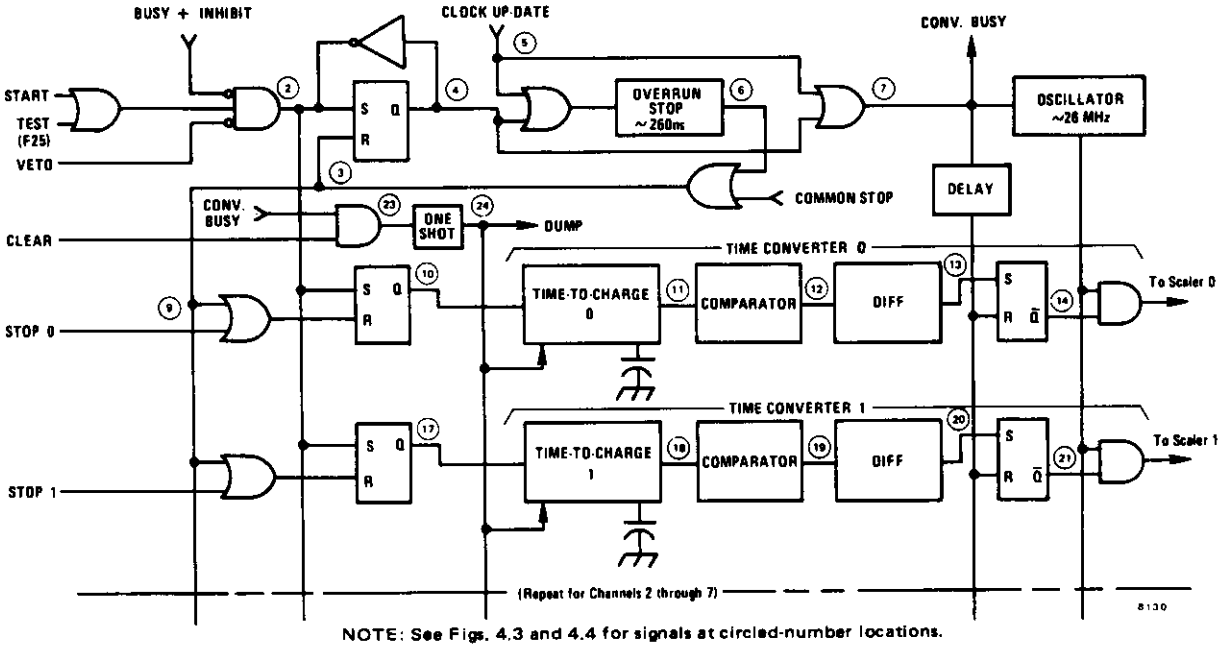
4.1. GENERAL FUNCTION

The intended function of the TD811 is to accept a valid start input pulse and to measure the time from this common start to a unique stop pulse in each of its eight sections. Any or all of the eight sections, or channels, can be used as required by the experimental application. Any unused channel(s) can be disregarded and left with no connection.

When it receives a valid start pulse, the TD811 starts to charge each of eight capacitors with a known constant current. The charge continues until a stop input switches the capacitor circuit so that it discharges, also at a constant current rate but much slower; each channel responds only to its unique stop input, so it is possible to measure eight different start-to-stop intervals that all begin at the common start time. During the charge interval and the subsequent discharge interval the output from an oscillator (~26 MHz) is gated to the scaler, and this time duration is proportional to the measured start-to-stop time for the channel. The oscillator is common to all channels, while the gating intervals are unique to each channel.

In each channel that does not receive a stop input within the normal range time (~200 ns), an overrun stop timer furnishes a simulated stop input so that the capacitor charge interval is terminated before it is excessive. The overrun stop timer furnishes its output at about 260 to 270 ns after the valid start and the resulting time measurement stored in the register for that channel is automatically long enough to set R12 and indicate that it is not a valid measurement.

A conversion timer measures an interval of about 90 μs, which is adequate to accommodate any valid measurement. At the end of the 90-μs time after the valid start, it provides an L (LAM) output through the CAMAC Dataway. A significant bit configuration, using an 11-bit register, is retained in each of the eight scalers (with overflow indicated by a 12th bit in each scaler), where one scaler serves each stop input channel. At the proper Dataway command from the crate controller each register delivers its count level through the first 12 Dataway lines, R1 through R12. By jumper selection, the 12th bit can be furnished through Dataway line R16 instead of through R12 to simplify programming when used with a PDP-11 computer.



NOTE: See Figs. 4.3 and 4.4 for signals at circled-number locations.

Fig. 4.1. Block Diagram of the Time-to-Charge Converter and Digitizing Circuits in TD811.

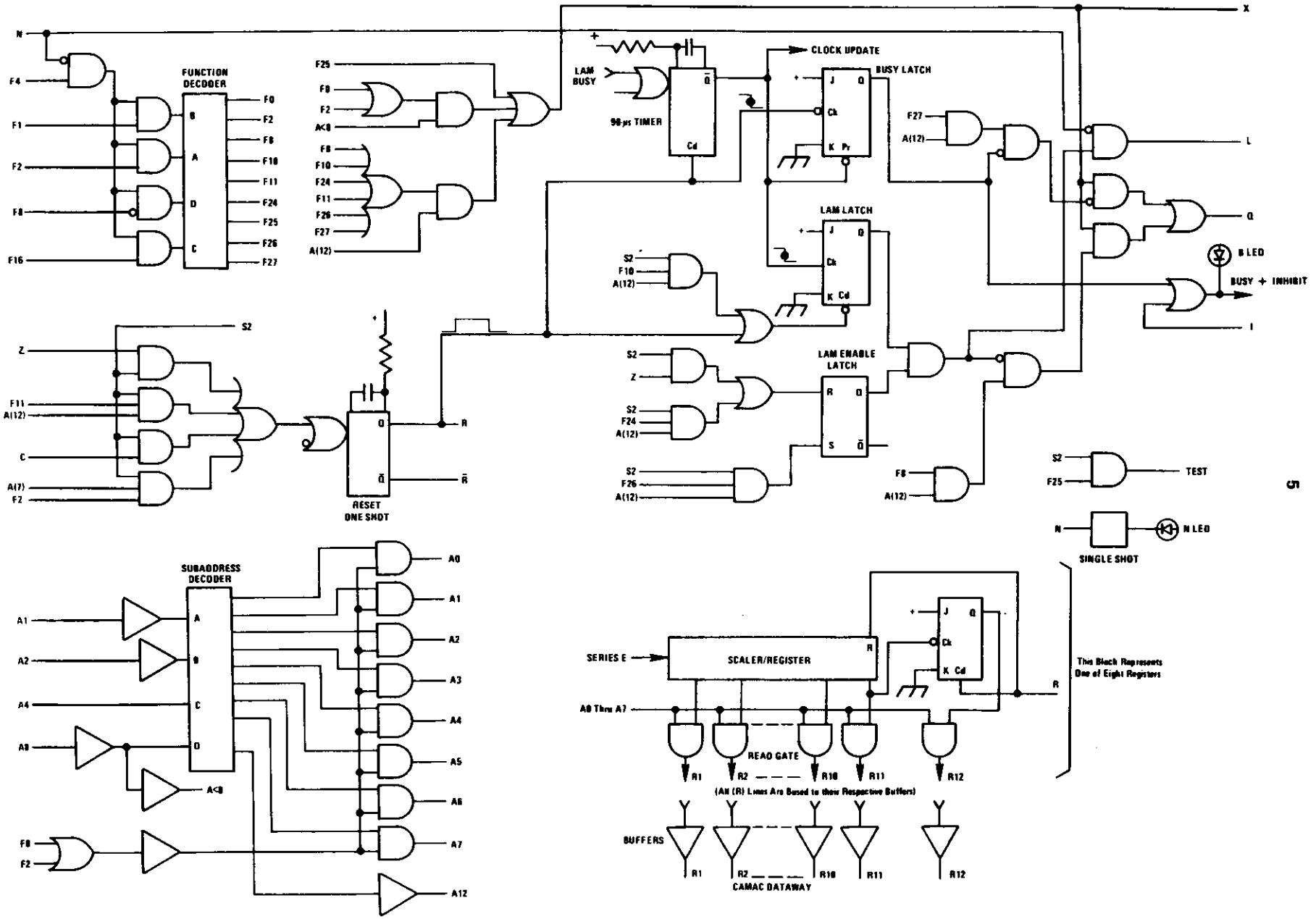
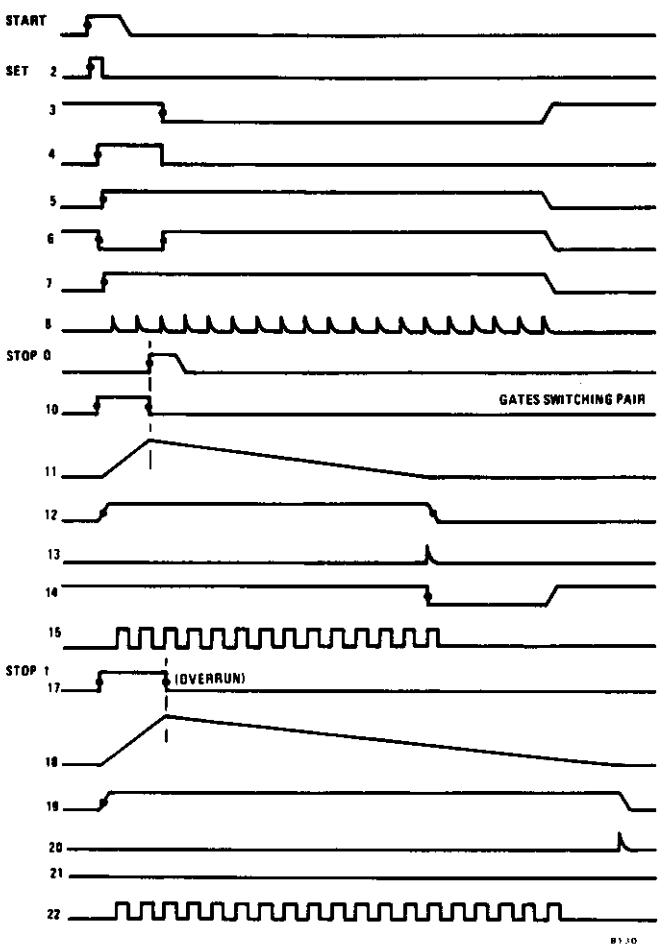
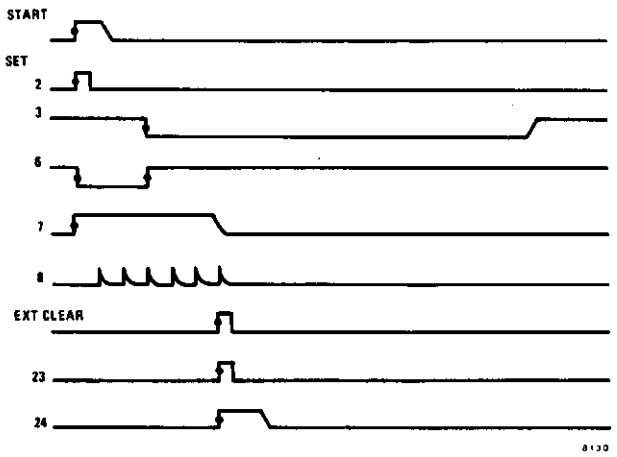


Fig. 4.2. Block Diagram of the Scaler-Registers and CAMAC Logic in TD811.



NOTE: See Fig. 4.1 for circuit locations of key numbers.

Fig. 4.3. Timing Diagram for a Normal Operating Cycle.



NOTE: See Fig. 4.1 for circuit locations of key numbers.

Fig. 4.4. Timing Diagram of Normal Cycle Aborted by Clear.

Front panel control signals can vary the standard program. For example, a signal through the veto connector that overlaps a start input signal will inhibit the module from accepting the start signal. If a signal is furnished through the clear input within the first 70 μs of the 90-μs conversion interval, the conversion is aborted and the module is reset within 1 μs, ready to accept a new start signal.

Either of two conditions generates a block condition for the start input and lights the B indicator on the front panel. These are the presence of a busy condition or an inhibit input from the Dataway I line. A signal through the veto connector on the front panel inhibits the start input from responding to a pulse.

Most commands from the crate controller will include a signal on the Dataway N line that identifies the station location of the TD811 in the crate, a function code such as F(0) or F(24), a subaddress code such as A(0) or A(12), and an S2 strobe. The N(), F(), and A() portions are not required for I (inhibit), Z (initialize), or C (clear) codes.

Whenever the module is addressed by N(k) from the crate controller, where k is the crate station location (1 through 23), the front panel N LED lights and the L status is inhibited from generating an L output signal to the Dataway until N is removed. While N is present, the function code decoder is enabled in this module only, and this is the method used to select the module according to its station location number.

All eight channels can be tested by either of two methods. A valid start input, followed by a signal through the common stop input on the front panel within <200 ns, will activate a measurement in all eight channels; the measurements will be similar but not necessarily identical because of the differences in transit time for the pulse to reach the various stop inputs and because of the walk in leading edge response time between the individual logic circuits. The other method is to furnish an F(25)·S2 command from the Dataway, and the module simulates a start signal and each channel counts the time interval to the overrun time automatic stop; all eight channels will contain a true R12 output to indicate that an overflow measurement has been made.

Any input command except Z or C generates an X response and, except for F(8)·A(12) and F(27)·A(12) it will also generate a Q response. For an F(8)·A(12) command Q = the internal L status unless the LAM enable latch is disabled. For an F(27)·A(12) command, Q = the internal busy status.

Figure 4.1 is a simplified block diagram of the time-to-charge converter and digitizing circuits in the TD811. Figure 4.2 shows the 12-bit registers and the circuits that generate or respond to CAMAC logic. The components that are included in the blocks in these figures are listed in Table 4.1.

Table 4.1. Components Comprising Blocks in Figs. 4.1 and 4.2.

Block Diagram Nomenclature	Components	Block Diagram Nomenclature	Components
Start	Q801, Q803	Time Converter 4	Q402 through Q415, C405 (Charge), R415 (Cal.), IC401(2), Q823, Q824, IC804(11)
Stop 0	Q001, IC001(9)	Time Converter 5	Q502 through Q515, C505 (Charge), R515 (Cal.), IC501(2), Q825, Q826, IC805(3)
Stop 1	Q101, IC101(9)	Time Converter 6	Q602 through Q615, Q605 (Charge), R615 (Cal.), IC601(2), Q827, Q828, IC805(8)
Stop 2	Q201, IC201(9)	Time Converter 7	Q702 through Q715, C705 (Charge), R715 (Cal.), IC701(2), Q829, Q830, IC805(11)
Stop 3	Q301, IC301(9)	90-μs Timer	IC2G(9)
Stop 4	Q401, IC401(9)	Busy Latch	IC2H(6)
Stop 5	Q501, IC501(9)	LAM Enable Latch	IC1F(10) and (13)
Stop 6	Q601, IC601(9)	LAM Latch	IC2H(9)
Stop 7	Q701, IC701(9)	Dump (and Reset)	IC2G(6)
Common Stop	Q804, IC802(2)	Scaler 0	IC4A, IC5A, IC3B(9)
Veto	Q802, IC801(14)	Read Gate 0	IC3A, IC4B, IC5B
Clear	Q811, Q812, Q813	Scaler 1	IC4C, IC5C, IC3B(12)
Inhibit	IC1H(3)	Read Gate 1	IC3C, IC4D, IC5D
Function Code Decoder	IC1B, IC1C(4) and (12), IC2B	Scaler 2	IC4E, IC5E, IC3F(9)
Subaddress Decoder	IC1L(6), (8), and (12), IC1C(2), IC2K	Read Gate 2	IC3E, IC4F, IC5F
C Line	IC2E(8)	Scaler 3	IC4G, IC5G, IC3F(12)
Z Line	IC2E(8), (11)	Read Gate 3	IC3G, IC4H, IC5H
S2 Line	IC1L(2)	Scaler 4	IC4J, IC5J, IC3K(9)
N Line	IC1C(10), IC1G(1)	Read Gate 4	IC3J, IC4K, IC5K
N Single Shot	Q832, Q833	Scaler 5	IC4L, IC5L, IC3K(12)
Test	IC1A(1), IC1C(8)	Read Gate 5	IC3L, IC4M, IC5M
Overrun Stop	R824, C802	Scaler 6	IC4N, IC5N, IC3P(9)
Time Converter 0	Q002 through Q015, C005 (Charge), R015 (Cal.), IC001(2), Q815, Q816, IC803(6)	Read Gate 6	IC3N, IC4P, IC5P
Time Converter 1	Q102 through Q115, C105 (Charge), R115 (Cal.), IC101(2), Q817, Q818, IC803(8)	Scaler 7	IC4R, IC5R, IC3P(12)
Time Converter 2	Q202 through Q215, C205 (Charge), R215 (Cal.), IC201(2), Q819, Q920, IC803(11)	Read Gate 7	IC3R, IC4S, IC5S
Time Converter 3	Q302 through Q315, C305 (Charge), R315 (Cal.), IC301(2), Q821, Q822, IC804(8)	Read Buffers	IC1R, IC1S
		Oscillator	Q807, Q808, Q810

Figure 4.3 is a timing diagram of the signal sequence and the approximate time relations for a normal cycle of operation. The start input initiates measurements for all eight channels. A stop input is shown for channel 0 within the 200-ns range, while no stop input is furnished to channel 1 so that its conversion interval is measured to the overrun stop time. The location of each indicated pulse in the figure is keyed to a numbered location in Fig. 4.1.

Figure 4.4 is a timing diagram of the signal sequence that occurs when an external clear input is furnished before a conversion has been completed. The dump command that is

generated in the TD811 aborts the measurement and resets its registers and logic within 1 μs.

4.2. LOOK-AT-ME SIGNAL

A LAM enable latch, IC1F(10) and (13), must be enabled so that an internal L signal can be generated. The latch is enabled by code N()·F(26)·A(12)·S2 from the Dataway. It is disabled by Z·S2 or by N()·F(24)·A(12)·S2.

If the latch has been set, a LAM status will be set 90 μs after a valid start unless a clear signal has been furnished prior to that time.

4.3. BUSY STATUS

A busy status is established quickly when a valid start is accepted. The busy condition inhibits the start input circuit from accepting any further signals until the module has completed its cycle and has been reset. The 90 μs conversion timer, IC2G(9), furnishes the inhibit signal to the start input and also triggers the busy latch, IC2H(6). The busy latch can be reset by either of two conditions; dump, due to a clear input signal within the conversion time, or a reset code from the Dataway. The busy status can be tested by F(27)·A(12).

4.4. TIME CONVERTERS

The circuit for each of the eight time converters is outlined in schematic TD811-0101-S1, across the bottom of the drawing. The complete circuit is shown for the Stop 0 channel, in which all components except for the output AND gate and driver use identification numbers in the 000 through 099 series. The equivalent components in each of the other channels use identification numbers that reflect the channel number, 1 through 7, as the most significant digit of the component designation. The following discussion uses the component numbers shown for channel 0 and each of the other channels operates identically.

Input flip-flop IC001(14) is set as a result of the common valid start input signal. This permits C005 to charge through Q004 at a constant current rate that is calibrated with R015. When a stop signal is furnished (through stop 0, from the common stop, or from the overrun stop), IC001(14) is reset and the constant current switches from Q004 to Q003; C005 then discharges through Q005 and R016 at a rate that takes about 500 times as long as the charging interval.

The total charge and discharge time interval for C005 is defined by a comparator, Q007 through Q012. During this time the comparator generates an output for trailing edge differentiation (Q013 and Q014) to reset flip-flop IC001(2). Flip-flop IC001(2) is normally held in its set state by Q015 and Q806 after a signal is furnished from IC802(3), and this occurs prior to the valid start pulse. Q815 translates the level furnished from IC001(2) to control AND gate IC803(6). The gate, with hysteresis from Q816, controls oscillator pulses to the scaler for the channel such that they can be counted until the stop control is effective.

The 26-MHz oscillator is turned on at valid start and runs until reset of the 90-μs timer, so oscillator pulses are available from start until the end of the fixed conversion time. By gating through IC803(6), they are furnished to the scaler for a significant portion of the total time during which they are available. The enabled interval is proportional to the start-to-stop time so the scaler count digitizes the expanded interval of time.

Q814 enables the path for a clear input signal. If a clear signal is furnished before the end of the 90-μs conversion time, a dump signal is generated to provide quick discharge of C005 through Q006 and to provide internal reset in IC2G(6) to abort the 90-μs timer and reset the busy latch and the scaler circuits.

4.5. SCALER/REGISTER CIRCUITS

Each of the eight 12-bit scalers counts the burst of oscillator pulses that are furnished from the AND gate. For each channel that measures 200 ns or less, the number of clock pulses will not overflow the 11-bit valid scaler capacity. If a stop input pulse fails to arrive within about 260 ns after the valid start, the overrun stop terminates the charging interval and starts discharge, so the maximum range that can be measured is sufficient to overflow the 11 valid bits and to set bit 12. When bit 12 has been set, the time indication is considered to be invalid because it may have been the result of a true stop input (later than 200 ns) or it may have resulted from the automatic overrun stop.

The scaler for channel 0 includes IC5A, IC4A, and IC3B(9). The accumulated count is held in the scaler until a reset occurs. The 12 bit identifications are furnished to gates IC5B, IC4B, and IC3A. At N()·F(0 + 2)·A(0)·S2 the A0 strobe is furnished to the gates and the 12 bits are furnished through the Dataway R1 through R12 lines. Since the bit on R12 identifies overflow, and the computer may be programmed to recognize the overflow identity on its R16 line, there is a jumper provision on the printed circuit by which the 12th bit can be routed through Dataway line R16 instead of through R12.

Each of the other seven scalers operates in exactly the same manner as that described for channel 0. The equivalent components are indicated on schematic TD811-0101-S1, at the right side of the drawing.

4.6. FUNCTION CODE DECODER

The function code decoder is IC2B. It is enabled by N()·F(4) and can generate codes F(0), F(2), F(8), F(10), F(11), F(24), F(25), F(26), and F(27) from signals through

the CAMAC F lines. These codes are all listed in Section 2, Specifications.

4.7. FUNCTION CODE F(0)

F(0) will be provided together with A(0) through A(7). The F(0) code commands read from the scaler/register that is designated by the A() subaddress code.

4.8. FUNCTION CODE F(2)

F(2) commands read only when it is furnished with A(0) through A(6), the same as for F(0) above. When F(2) is combined with A(7), it commands read of scaler/register 7 and then, at S2 time, clears all registers, busy, and LAM.

4.9. FUNCTION CODE F(8)

F(8) operates with A(12) to test the internal LAM status. The test is applied to the LAM status signal following the LAM enable latch function. It is derived from IC1G(4) and the Q output is equal to the LAM status at S2 time.

4.10. FUNCTION CODE F(10)

F(10) operates with A(12) to reset LAM latch IC2H(9) at S2 time. No other condition in the TD811 is affected by this code, and it is not operative during conversion because the LAM latch is not set until the end of the 90-μs conversion time.

4.11. FUNCTION CODE F(11)

F(11) operates with A(12) to provide a general reset at S2 time. Reset is furnished to all eight scaler/registers and to both the busy and LAM status latches.

4.12. FUNCTION CODE F(24)

F(24) operates with A(12) to selectively disable LAM enable latch IC1F(10) and (13). When this latch is disabled, it inhibits gating for the LAM status indication at the end of conversion, so the L output signal can neither be tested nor furnished through the Dataway N line.

4.13. FUNCTION CODE F(25)

F(25) operates with any subaddress, A(0) through A(7), to test all eight channels simultaneously at S2 time. The test command is furnished as a start input through IC1G(10) and Q803. Since it is not followed by a stop input in any channel, the internal overrun stop is effective and all channels will count an interval that will cause the 12th bit to be set, providing that the time converter and scaler operates properly in each channel.

4.14. FUNCTION CODE F(26)

An F(26)·A(12) code selectively enables LAM enable latch IC1F(10) and (13). After the latch has been enabled, it permits the LAM status to be both tested and furnished through Dataway L line.

4.15. FUNCTION CODE F(27)

F(27) operates with A(12) to test the status of busy latch IC2H(6). The Dataway Q signal is equal to the busy status at S2 time.

4.16. CODE Z·S2

Z·S2 is not dependent upon an N code and is the general signal to initialize all modules in the crate. In the TD811 it clears all eight scaler/registers to zero, clears the LAM and Busy status latches, and disables LAM enable latch IC1F(10) and (13). After this signal has been used, an N()·F(26)·A(12)·S2 signal must be used to again enable the latch before any L signals can be tested or furnished.

4.17. CODE C·S2

C·S2 is not dependent upon an N code and is the general signal to clear all modules in the crate. In the TD811 it clears all eight scaler/registers to zero and clears the busy and LAM status latches. It does not affect the LAM enable latch.

4.18. SUPPLEMENTARY DATAWAY INFORMATION

The relative timing of signals in a Dataway operation is shown in Fig. 4.5 and Tables 4.2 through 4.5 are provided as an aid for using a CAMAC system. These tables show standard Dataway usage, connector pin assignments at both "normal" and "control" stations, and the function codes. The control station is always the highest numbered station location in the crate. In a 25-station crate, this is station 25 and stations 1 through 24 are all normal stations. Since a type A crate controller must occupy the control station and at least one adjacent normal station, the TD811 must be assigned a location within the group from 1 through 23. Its station location is its N() identification for selection of any code that includes an F() function code.

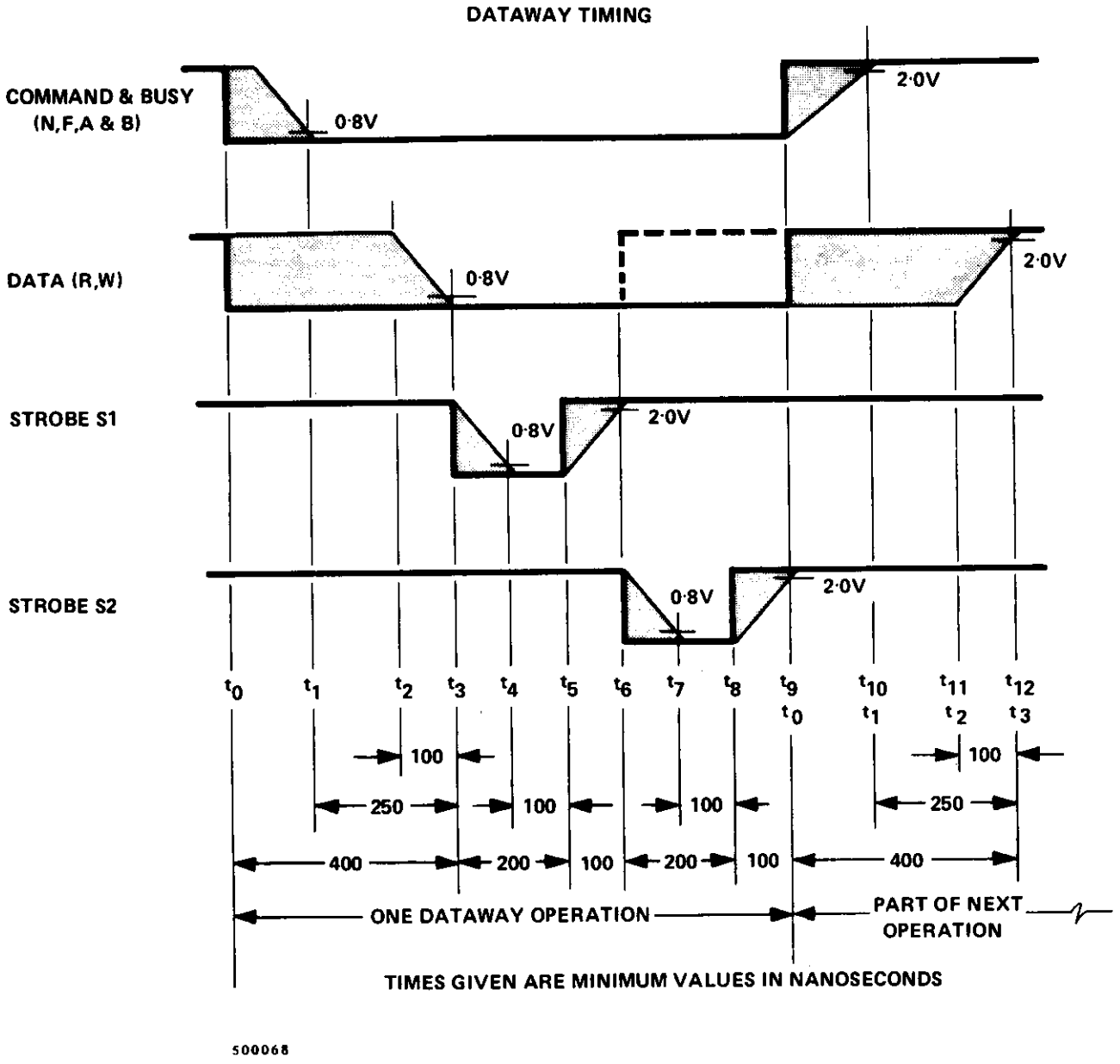


Fig. 4.5. Timing of a Dataway Operation (Fig. 9 of TID-25875).

Table 4.2. Standard Dataway Usage (Table I of TID-25875).

Title	Designation	Contacts	Use at Module
Command			
Station Number	N	1	Selects the module (Individual line from control station).
Sub-Address	A1,2,4,8	4	Selects a section of the module.
Function	F1,2,4,8,16	5	Defines the function to be performed in the module.
Timing			
Strobe 1	S1	1	Controls first phase of operation (Dataway signals must not change).
Strobe 2	S2	1	Controls second phase (Dataway signals may change).
Data			
Write	W1–W24	24	Bring information to the module.
Read	R1–R24	24	Take information from the module.
Status			
Look-at-Me	L	1	Indicates request for service (Individual line to control station).
Busy	B	1	Indicates that a Dataway operation is in progress.
Response	Q	1	Indicates status of feature selected by command.
Command Accepted	X	1	Indicates that module is able to perform action required by the command.
Common Controls			*Operate on all features connected to them, no command required.*
Initialise	Z	1	Sets module to a defined state. (Accompanied by S2 and B).
Inhibit	I	1	Disables features for duration of signal.
Clear	C	1	Clears registers. (Accompanied by S2 and B).
Non-Standard Connections			
Free bus-lines	P1,P2	2	For unspecified uses.
Patch contacts	P3–P5	3	For unspecified interconnections. No Dataway Lines.
Mandatory Power Lines			*The crate is wired for mandatory and additional lines.*
+24 V d.c.	+24	1	
+6 V d.c.	+6	1	
−6 V d.c.	−6	1	
−24 V d.c.	−24	1	
0 V	0	2	Power return.
Additional Power Lines			*Lines are reserved for the following power supplies*
+200 V d.c.	+200	1	Low current for indicators etc.
+12 V d.c.	+12	1	
−12 V d.c.	−12	1	
117 V a.c. (Live)	ACL	1	
117 V a.c. (Neutral)	ACN	1	
Clean Earth	E	1	Reference for circuits requiring clean earth.
Reserved	Y1,Y2	2	Reserved for future allocation.
TOTAL		**86**	

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Table 4.3. Contact Allocation at a Normal Station (Table II of TID-25875).

(Viewed from front of crate)

Bus-line	Free Bus-line	P1	B	Busy	Bus-line
Bus-line	Free Bus-line	P2	F16	Function	Bus-line
Individual patch contact		P3	F8	Function	Bus-line
Individual patch contact		P4	F4	Function	Bus-line
Individual patch contact		P5	F2	Function	Bus-line
Bus-line	Command Accepted	X	F1	Function	Bus-line
Bus-line	Inhibit	I	A8	Sub-address	Bus-line
Bus-line	Clear	C	A4	Sub-address	Bus-line
Individual line	Station Number	N	A2	Sub-address	Bus-line
Individual line	Look-at-Me	L	A1	Sub-address	Bus-line
Bus-line	Strobe 1	S1	Z	Initialise	Bus-line
Bus-line	Strobe 2	S2	Q	Response	Bus-line
		W24	W23		
		W22	W21		
		W20	W19		
		W18	W17		
24 Write Bus-lines		W16	W15		
		W14	W13		
W1 = least significant bit		W12	W11		
W24 = most significant bit		W10	W9		
		W8	W7		
		W6	W5		
		W4	W3		
		W2	W1		
		R24	R23		
		R22	R21		
		R20	R19		
		R18	R17		
24 Read Bus-lines		R16	R15		
		R14	R13		
R1 = least significant bit		R12	R11		
R24 = most significant bit		R10	R9		
		R8	R7		
		R6	R5		
		R4	R3		
		R2	R1		
Power Bus-lines	−12V d.c.	−12	−24	−24V d.c.	Power Bus-lines
	+200V d.c.	+200	−6	−6V d.c.	
	117V a.c. Live	ACL	ACN	117V a.c. Neutral	
	Reserved	Y1	E	Clean Earth	
	+12V d.c.	+12	+24	+24V d.c.	
	Reserved	Y2	+6	+6V d.c.	
	0V (Power Return)	0	0	0V (Power Return)	

The assignment of contacts at the Dataway connector and their connections to bus-lines, individual lines and patch contacts must be as shown in Table II for normal stations and Table III for the control station. The control station must be to the right of all normal stations.

Table 4.4. Contact Allocation at the Control Station (Table III of TID-25875).

(Viewed from front of crate)

Individual patch contact		P1	B	Busy	Bus-line
Individual patch contact		P2	F16	Function	Bus-line
Individual patch contact		P3	F8	Function	Bus-line
Individual patch contact		P4	F4	Function	Bus-line
Individual patch contact		P5	F2	Function	Bus-line
Bus-line	Command Accepted	X	F1	Function	Bus-line
Bus-line	Inhibit	I	A8	Sub-address	Bus-line
Bus-line	Clear	C	A4	Sub-address	Bus-line
Individual patch contact		P6	A2	Sub-address	Bus-line
Individual patch contact		P7	A1	Sub-address	Bus-line
Bus-line	Strobe 1	S1	Z	Initialise	Bus-line
Bus-line	Strobe 2	S2	Q	Response	Bus-line
		L24	N24		
		L23	N23		
		L22	N22		
		L21	N21		
		L20	N20		
		L19	N19		
		L18	N18		
		L17	N17		
		L16	N16		
		L15	N15		
		L14	N14		
24 individual Look-at-Me lines		L13	N13	*24 individual Station Number lines*	
L1 from Station 1, etc.		L12	N12	N1 to Station 1, etc.	
		L11	N11		
		L10	N10		
		L9	N9		
		L8	N8		
		L7	N7		
		L6	N6		
		L5	N5		
		L4	N4		
		L3	N3		
		L2	N2		
		L1	N1		
	−12V d.c.	−12	−24	−24V d.c.	
	+200V d.c.	+200	−6	−6V d.c.	
Power	117V a.c. Live	ACL	ACN	117V a.c. Neutral	Power
Bus-lines	Reserved	Y1	E	Clean Earth	Bus-lines
	+12V d.c.	+12	+24	+24V d.c.	
	Reserved	Y2	+6	+6V d.c.	
	0V (Power Return)	0	0	0V (Power Return)	

The method of construction of the Dataway must be consistent with the signal standards for signal lines (see Section 7) and with the maximum current loads specified for the power lines (see Section 8).

Table 4.5. The Function Codes (Table IV of TID-25875).

No.	Function	F16	F8	F4	F2	F1	No.
0	Read Group 1 Register — Functions which use the R lines	0	0	0	0	0	0
1	Read Group 2 Register	0	0	0	0	1	1
2	Read and Clear Group 1 Register	0	0	0	1	0	2
3	Read Complement of Group 1 Register	0	0	0	1	1	3
4	Non-standard — Additional functions which use the R lines	0	0	1	0	0	4
5	Reserved	0	0	1	0	1	5
6	Non-standard	0	0	1	1	0	6
7	Reserved	0	0	1	1	1	7
8	Test Look at Me — These functions do not use the R or W lines	0	1	0	0	0	8
9	Clear Group 1 Register	0	1	0	0	1	9
10	Clear Look at Me	0	1	0	1	0	10
11	Clear Group 2 Register	0	1	0	1	1	11
12	Non-standard — Additional Functions	0	1	1	0	0	12
13	Reserved	0	1	1	0	1	13
14	Non-standard	0	1	1	1	0	14
15	Reserved	0	1	1	1	1	15
16	Overwrite Group 1 Register — Functions which use the W lines	1	0	0	0	0	16
17	Overwrite Group 2 Register	1	0	0	0	1	17
18	Selective Overwrite Group 1 Register	1	0	0	1	0	18
19	Selective Overwrite Group 2 Register	1	0	0	1	1	19
20	Non-standard — Additional functions which use the W lines	1	0	1	0	0	20
21	Reserved	1	0	1	0	1	21
22	Non-standard	1	0	1	1	0	22
23	Reserved	1	0	1	1	1	23
24	Disable — These functions do not use the R or W lines	1	1	0	0	0	24
25	Increment Preselected Registers	1	1	0	0	1	25
26	Enable	1	1	0	1	0	26
27	Test Status	1	1	0	1	1	27
28	Non-standard — Additional Functions	1	1	1	0	0	28
29	Reserved	1	1	1	0	1	29
30	Non-standard	1	1	1	1	0	30
31	Reserved	1	1	1	1	1	31

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5. MAINTENANCE AND CALIBRATION

5.1. CAUTIONS

When any maintenance is done on this unit, it is strongly advised that the following Cautions be observed.

CAUTIONS

Certain solvents may possibly damage the printed-circuit board or other components. If uncertain as to the compatibility of a specific solvent and any of the components, consult EG&G/ORTEC before using it.

Always ensure that CAMAC crate power is turned off before installing or removing any CAMAC module.

Always ensure that all pins on the CAMAC Dataway connector on the rear of the unit are clean before installing any CAMAC module in its crate.

Always heat-sink the leads to diodes, transistors, and IC's whenever soldering or unsoldering them.

Never use excessive force in installing or removing any CAMAC module.

Handle all printed-circuit boards with care.

Do not clean solder-clogged printed-circuit board holes by heating and then pushing a wire through them. This procedure can damage the board by lifting the land. Heat the hole as little as possible and then use a solder puller to remove excess solder.

5.2. PREVENTIVE MAINTENANCE

The only preventive maintenance required involves giving reasonable attention to mechanical details. Keep the signal connectors clean, and periodically remove the cover plates to inspect the interior of the module for excessive dust accumulation. Clean as often as required by local conditions (normally about once every 12 months).

5.3. CORRECTIVE MAINTENANCE

Corrective maintenance will generally be restricted to replacing defective components, such as resistors, capacitors, diodes, transistors, and IC's, to replacing missing hardware, and to tightening loose hardware. In tightening screws, nuts, etc., ***do not*** use excessive force.

When replacing components on a printed-circuit board, be sure that the board is not damaged by excessive heating. When unsoldering leads, grip the lead to be unsoldered with a tool that also acts as a heat sink. Heat the solder joint as little as possible while maintaining a steady pull on the component lead to assure prompt removal of the lead. Use a solder puller to remove excess solder from the board. ***Do not*** redrill holes in the printed-circuit board. When the integrity of a plated-through hole is in doubt, solder the component lead on both sides of the board.

5.4. TEST POINTS AND VOLTAGES

Digital circuits operate in only the on state or the off state. Therefore, with the exception of certain circuit points in networks consisting of resistors, capacitors, diodes, and transistors that are external to integrated circuits, the voltages will normally be either nominal ground or approximately the supply voltage. The voltage read at any point depends on the function of the IC, transistor, or other component and on its input.

The voltages listed in Table 5.1 are typical values that were measured in the portions of the TD811 circuits that differ from the normal digital type and therefore have significant levels that are different from the supply level. These voltages are to be considered as typical, rather than absolute, and are furnished to aid in troubleshooting suspected circuits where a malfunction occurs.

The conditions used for the measurements included: measurements were made with a DVM with an 11 MΩ input impedance; the proper supply voltage levels were furnished at the module connector; and the module had received a start input pulse followed by Z·S2. The test points are listed for components that are included in channel 0 and are typical of the equivalent test points in each of the other seven channels.

5.5. PERFORMANCE TESTING

The following test procedure is considered sufficient to determine that the TD811 is in operating condition:

1. With the TD811 in an assigned location in a crate and with power applied, furnish N()·F(11)·A(12) from the Dataway. Check for an X and a Q response, and check the N indicator for a short flash.

2. Furnish N()·F(0)·A(*k*) (where *k* is the channel number, 0 through 7, applied sequentially). Read zero for all 12 bits from each channel and check for an X and Q response.

3. Furnish N()·F(8)·A(12). Check for X = 1 and Q = 0.

4. Furnish N()·F(27)·A(12). Check for X = 1 and Q = 0.

5. Furnish N()·F(26)·A(12). Check for X = 1 and Q = 1.

Table 5.1. Typical Voltage Measurements.

Test Point	Voltage	Test Point	Voltage	Test Point	Voltage	Test Point	Voltage
Q001E	−0.74	Q013E	0	Q810E	−6.0	(6)	+4.1
Q001B	−0.01	Q013B	−0.83	Q810B	−5.6	(7)	0
Q001C	0	Q013C	−0.1	Q810C	+2.5	(8)	+4.1
Q002E	−5.5	Q014E	0	Q811E	0	(9)	+4.1
Q002B	−4.8	Q014B	0	Q811B	−0.15	(10)	+0.25
Q002C	−1.5	Q014C	+1.2	Q811C	+3.2	(11)	+4.1
Q003E	−1.5	Q015E	−0.73	Q812E	−6.0	(12)	+4.1
Q003B	−0.78	Q015B	−0.1	Q812B	−0.22	(13)	+0.25
Q003C	−0.1	Q015C	0	Q812C	+0.51	(14)	+5.0
Q004E	−1.5	Q801E	−0.76	Q813E	+0.53	IC804(1)	+2.5
Q004B	−1.2	Q801B	−0.01	Q813B	0	(2)	+2.5
Q004C	+3.25	Q801C	0	Q813C	−4.6	(3)	+0.25
Q005E	+5.5	Q802E	0	Q814E	+6.0	(4)	+0.25
Q005B	+5.0	Q802B	−0.36	Q814B	+5.75	(5)	+0.25
Q005C	+3.25	Q802C	−1.0	Q814C	−0.1	(6)	+3.8
Q006E	+3.25	Q803E	−0.01	Q815E	−0.65	(7)	0
Q006B	+3.1	Q803B	−0.32	Q815B	0	(8)	+4.1
Q006C	+3.25	Q803C	−6.0	Q815C	+4.3	(9)	+4.1
Q007E	−0.65	Q804E	−0.70	Q816E	+5.0	(10)	+0.25
Q007B	0	Q804B	−0.01	Q816B	+5.0	(11)	+4.1
Q007C	0	Q804C	0	Q816C	+4.1	(12)	+0.25
Q008E	−0.65	Q805E	0	Q831E	0	(13)	+4.1
Q008B	−0.15	Q805B	−0.38	Q831B	+0.7	(14)	+5.0
Q008C	+3.25	Q805C	−0.71	Q831C	+0.1	IC805(1)	+4.1
Q009(A)E	+4.7	Q806E	−0.08	Q832E	0	(2)	+0.25
Q009(A)B	+13.6	Q806B	−0.72	Q832B	+0.08	(3)	+4.1
Q009(A)C	+3.25	Q806C	−6.0	Q832C	+0.7	(4)	+3.8
Q009(B)E	+4.7	Q807E	−1.44	Q833E	0	(5)	+3.8
Q009(B)B	+13.6	Q807B	−0.72	Q833B	+0.7	(6)	+0.25
Q009(B)C	+3.25	Q807C	−0.81	Q833C	+0.1	(7)	0
Q011E	+14.3	Q808E	−0.74		[(N) light on]	(8)	+4.1
Q011B	+13.6	Q808B	−1.49	IC803(1)	+3.8	(9)	+4.1
Q011C	−0.15	Q808C	−5.6	(2)	+5.0	(10)	+0.25
Q012E	+14.3	Q809E	0	(3)	+0.25	(11)	+4.1
Q012B	+13.6	Q809B	−0.80	(4)	+0.25	(12)	+0.25
Q012C	−0.83	Q809C	+5.1	(5)	+4.1	(13)	+4.1
						(14)	+5.0

6. Furnish N()·F(25)·A(*k*) (where *k* is any channel number, 0 through 7). This generates an internal test in which all scalers count to an overrun condition, setting bit 12. At the end of the conversion, it sets LAM. Check the front panel B indicator for the busy status indication.

7. Furnish N()·F(8)·A(12). Check for X = 1 and Q = 1.

8. Read the scaler contents by N()·F(0)·A(0 through 7) (in sequence). At each read command check the scaler contents to see that its 11 valid bits read some number other than zero and that the 12th bit has been set. Each command generates X = 1 and Q = 1.

9. Repeat step 8, using N()·F(2)·A(0 through 7). At each command the scaler contents and the X and Q responses should be the same as in step 8, and all scalers should be reset after channel 7 has been read.

10. Furnish N()·F(25)·A(*k*) (where *k* is any channel number, 0 through 7). This restores a count into all scalers as in step 6.

11. Furnish N()·F(11)·A(12) to reset all scalers, the busy status, and LAM. Then furnish N()·F(0)·A(0 through 7) to read each scaler for response to the reset.

12. Furnish N()·F(10)·A(12) to reset the LAM status latch without affecting the busy latch or the scaler count levels. Furnish N()·F(8)·A(12) to test LAM; check for X = 1 and Q = 0. Furnish N()·F(27)·A(12) to test busy; check for X = 1 and Q = 1.

13. Furnish C through the Dataway common line. Read each scaler for zero and then test both busy and LAM status indications for Q = 0.

14. Restore a count and the LAM status with N()·F(25)·A(0 through 7).

15. Furnish Z through the Dataway common line. Read each scaler for zero and then test for Q = 0 for both busy and LAM.

16. Restore a count with N()·F(25)·A(0 through 7).

17. Furnish N()·F(8)·A(12) to test for the LAM status. Check for X = 1 and Q = 0; even though the LAM status is known to be present, the test for it results in Q = 0 because the LAM enable latch was reset by Z in step 15.

18. Furnish N()·F(26)·A(12) to set the LAM enable latch.

19. Test L with N()·F(8)·A(12). Check for X = 1 and Q = 1.

5.6. CALIBRATION

Calibration of the TD811 consists of adjusting the constant current that is used in each channel during the charging interval of its charge capacitor (e.g. C005). The potentiometers that are used to adjust this function are located near the front of the printed circuit board, where one control is mounted in each channel section on the board. Since the rate of constant current determines the level to which the capacitor charges during the start-to-stop interval, it also controls the resulting discharge time and the overall time during which the oscillator pulses are gated into the scaler. Each channel should be adjusted to provide a calibration of 100 ps per scaler count, referring to the start-to-stop interval measured in that channel. The common stop input and test functions cannot be used for precise calibration because of the transit time variations to the separate stop inputs and to the threshold level variations at which the input flip-flops will respond. Calibrated 50Ω cable may be used to provide a precise start-to-stop delay for adjusting the calibration potentiometer in each separate channel.

APPENDIX

REPLACEABLE PARTS

ORDERING INFORMATION

The Replaceable Parts List shown below contains information needed for ordering spare and/or replacement parts. Each listing indicates the reference designator number, the part number, a description of the component, and the part manufacturer and manufacturer's part number.

All inquiries concerning spare and/or replacement parts and all orders for same should include the model and serial numbers of the instruments involved and should be addressed to the Customer Service Department at 100 Midland Road, Oak Ridge, Tennessee 37830. The Manager of Customer Services can be reached by telephone at (615) 482-4411. The minimum order for spare and/or replacement parts is $25.00.

ORDERING INFORMATION FOR PARTS NOT LISTED

In order to facilitate the ordering of a part not listed below, the following information should be submitted to the Customer Service Department:

1. the instrument model number,
2. the instrument serial number,
3. a description of the part,
4. information as to the function and location of the part.

NOTE: In the following List of Replaceable Parts, those parts that are repeated within the 8 sections of the TD811 and that use the section number as the most significant digit in the reference designation appear with a "k" to replace the section number. Thus, Rk14 represents resistors R014, 114, 214, 314, 414, 514, 614, and 714.

Replaceable Parts List

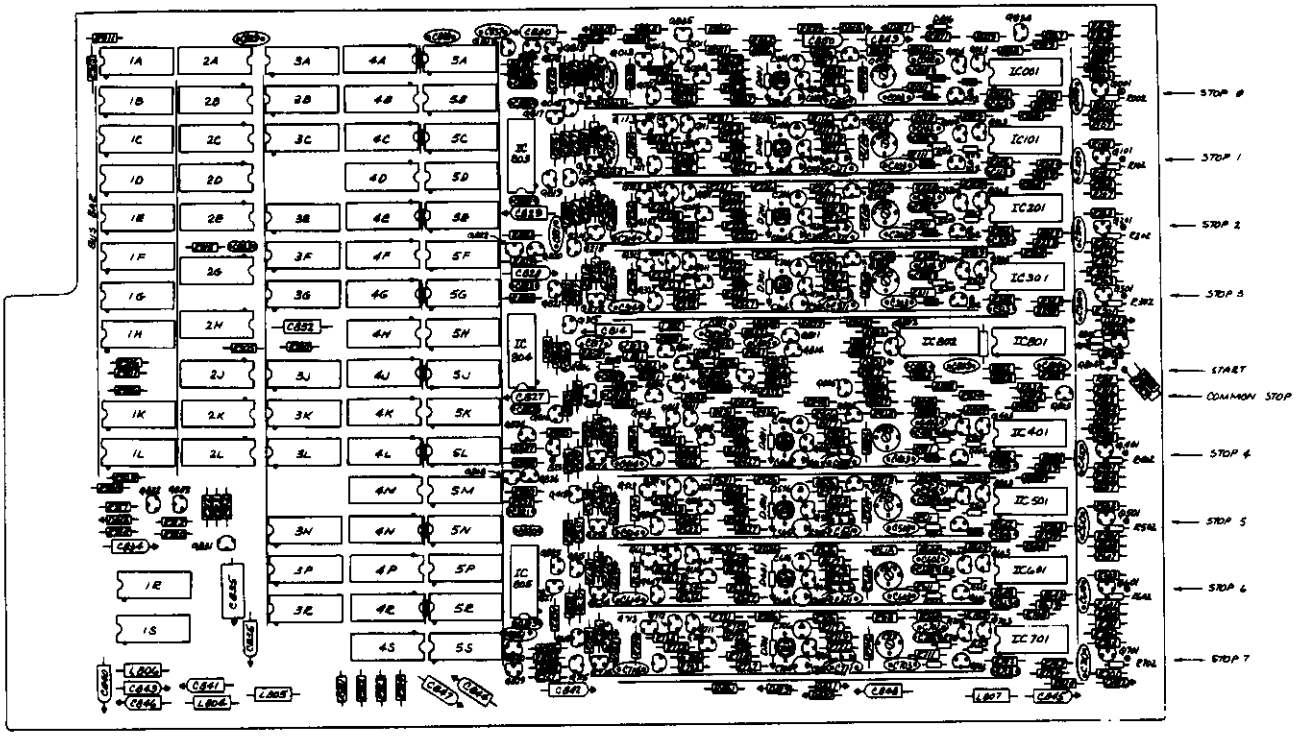
Description	ORTEC Part No.	Reference Designations
Capacitors		
15 pF 5% SM	47156	Ck12
22 pF 5% 1KV Disc	40875	C805
39 pF 5% 500V Mica	40908	C819, 820, 821, 822, 823, 824, 825, 826
91 pF 2% 500V Mica	41717	C813
100 pF 2% 500V Mica	40886	Ck13, 804
150 pF 5% 100V DM	47167	C816, 833
180 pF 5% 500V Mica	40888	C812
330 pF 2% 500V Mica	41710	Ck05, 815
1000 pF 2% 100V Mica	40895	C802
0.01 μF 20% 50V Disc	65506	Ck02, k03, k10, k11, 808, 809, 811, 817, 818, 831, 837, 838, 839, 851
0.027 μF 5% 100V Mylar	45905	C832
1 μF 10% 35V Tan	49546	C827, 828, 829, 830, 834, 836, 840, 841, 842, 843, 844, 845, 846, 847, 848, 849, 850
6.8 μF 20% 35V Tan	49542	Ck04, k06, k09
60 μF 20% 6V Tan	40955	C814
220 μF 20% 10V	40953	C835
Diodes		
1N270	41098	D801, 803, 813
1N752A	41106	D817, 820
1N942	60206	D818, 821
1N4005	60228	D822, 823
1N4009	41125	D815, 819
1N4153 75V	44217	D816
FD-777 Special	60202	Dk03, 802
NDP-116	60203	Dk01

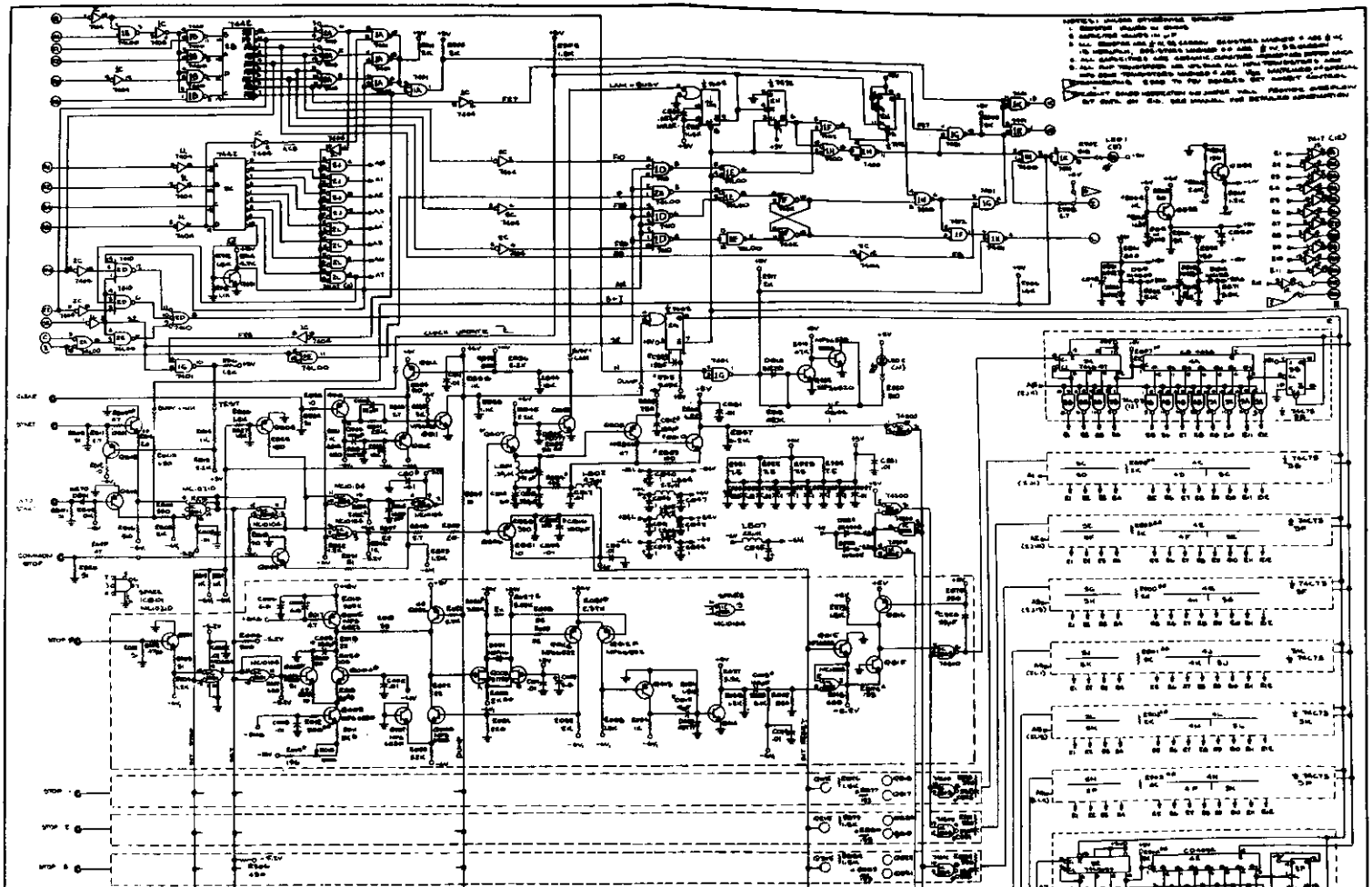
Replaceable Parts List (continued)

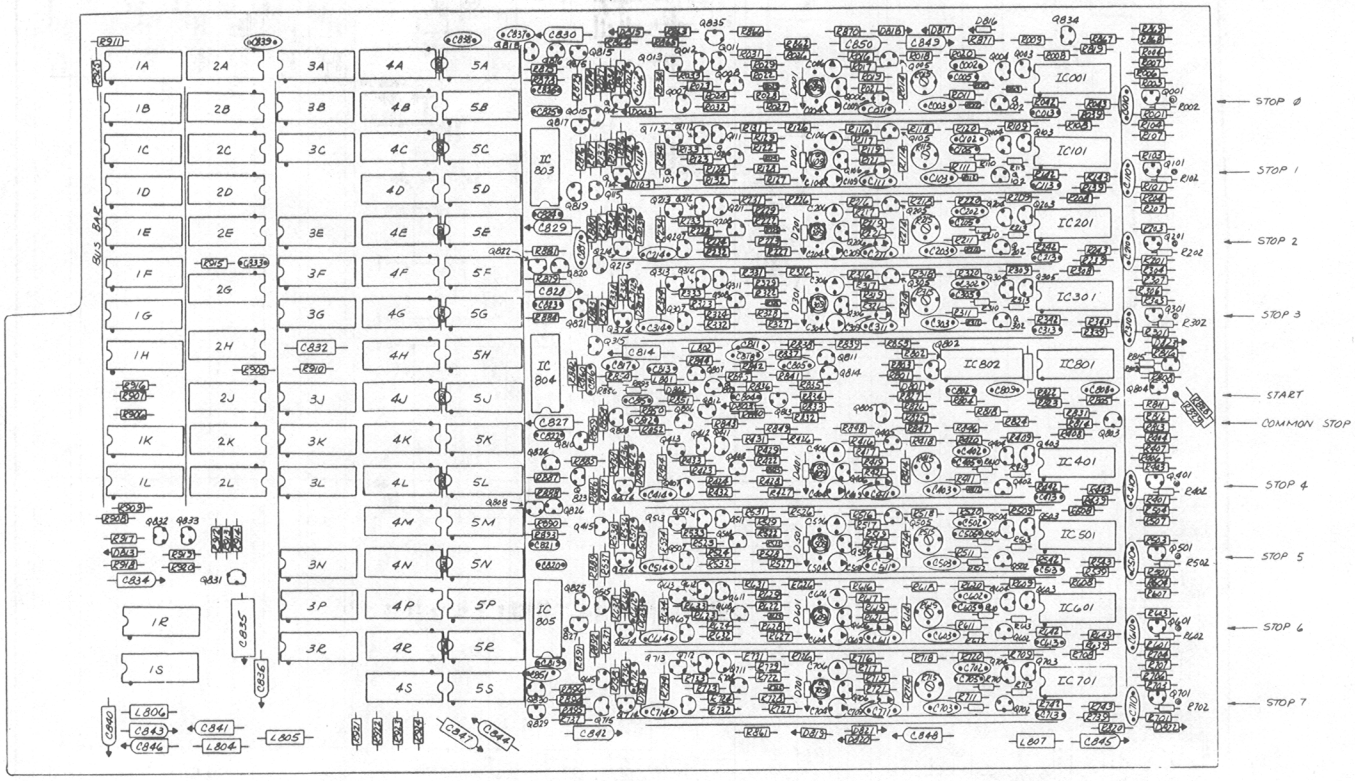
Description	ORTEC Part No.	Reference Designations
Integrated Circuits		
73C73	66163	IC3B, 3F, 3K, 3P
74L00	65487	IC1E, 2E
74LS197	65488	IC5A, 5C, 5E, 5G, 5J, 5L, 5N, 5R
9602PC	63752	IC2G
MC10104	66170	ICk01, 802
MC10210	66158	IC801
SCL4024AE	66164	IC4A, 4C, 4E, 4G, 4J, 4L, 4N, 4R
SN7400N	44073	IC1B, 1H
SN7401N	44074	IC1A, 1G, 1K
SN7402N	44086	IC1F
SN7404	44079	IC1C, 1L, 2C
SN7410N	44081	IC1D, 2A, 2D
SN7417N	65460	IC1R, 1S
SN7442N	49495	IC2B, 2K
SN7474N	49504	IC2H
SN74L02	65441	IC2J, 2L
SN74L03	63765	IC3A, 3C, 3F, 3G, 3J, 3L, 3N, 3R, 4B, 4D, 4F, 4H, 4K, 4M, 4P, 4S, 5B, 5D, 5F, 5H, 5K, 5M, 5P, 5S
SN74S00	63769	IC803, 804, 805
Inductors		
0.39 μH Deciductor	41234	L801
4.7 μH Choke	47088	L802
Ferroxcube VK200 10/3B	61177	L804, 805, 806, 807
Transistors		
FD1735	48018	Qk09
MPS2369	47844	Qk01, k14, 801, 804, 809, 815, 817, 819, 821, 823, 825, 827, 829, 831, 834, 835
MPS2369 Select	47845	Qk03, k04, 807, 810
MPS3640	43652	Qk13, 802, 803, 805, 806, 808, 812, 813, 814, 816, 818, 820, 822, 824, 826, 828, 830
MPS3640 Select	47857	Qk06
MPS6520	43649	Qk02, k07, k08, k15, 811, 832, 833
MPS6522	43654	Qk05
MPS6522 Select	48028	Qk11, k12
Resistors		
2.7Ω CC 1/4W 5%	43949	R811, 840, 847, 848, 908
4.7Ω CC 1/4W 5%	40295	Rk17
7.5Ω CC 1/4W 5%	43975	R921, 922, 923, 924
10Ω CC 1/4W 5%	40202	R812, 833, 839, 851
10Ω CC 1/8W 5%	60891	Rk13
20Ω CC 1/4W 5%	40296	Rk09, k10, 849, 865
20Ω CC 1/8W 5%	60893	R815
22Ω CC 1/4W 5%	40204	Rk18, k22, k28, k29
30Ω CC 1/8W 5%	60894	R855
33Ω CC 1/4W 5%	40205	Rk19
47Ω CC 1/4W 5%	40206	R829
47Ω CC 1/8W 5%	60947	Rk02, 809, 856
51Ω CC 1/4W 5%	40271	Rk01, k03, k08, 801, 808, 828, 831, 832
100Ω CC 1/4W 5%	40209	Rk20, 852
100Ω CC 1/8W 1% T–O	40489	R859

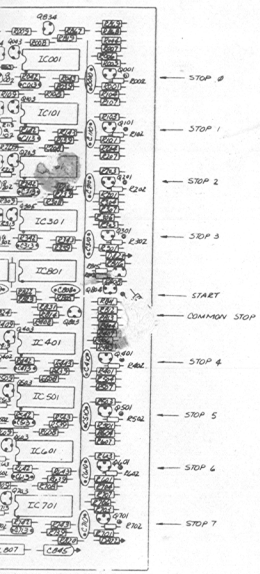
Replaceable Parts List (continued)

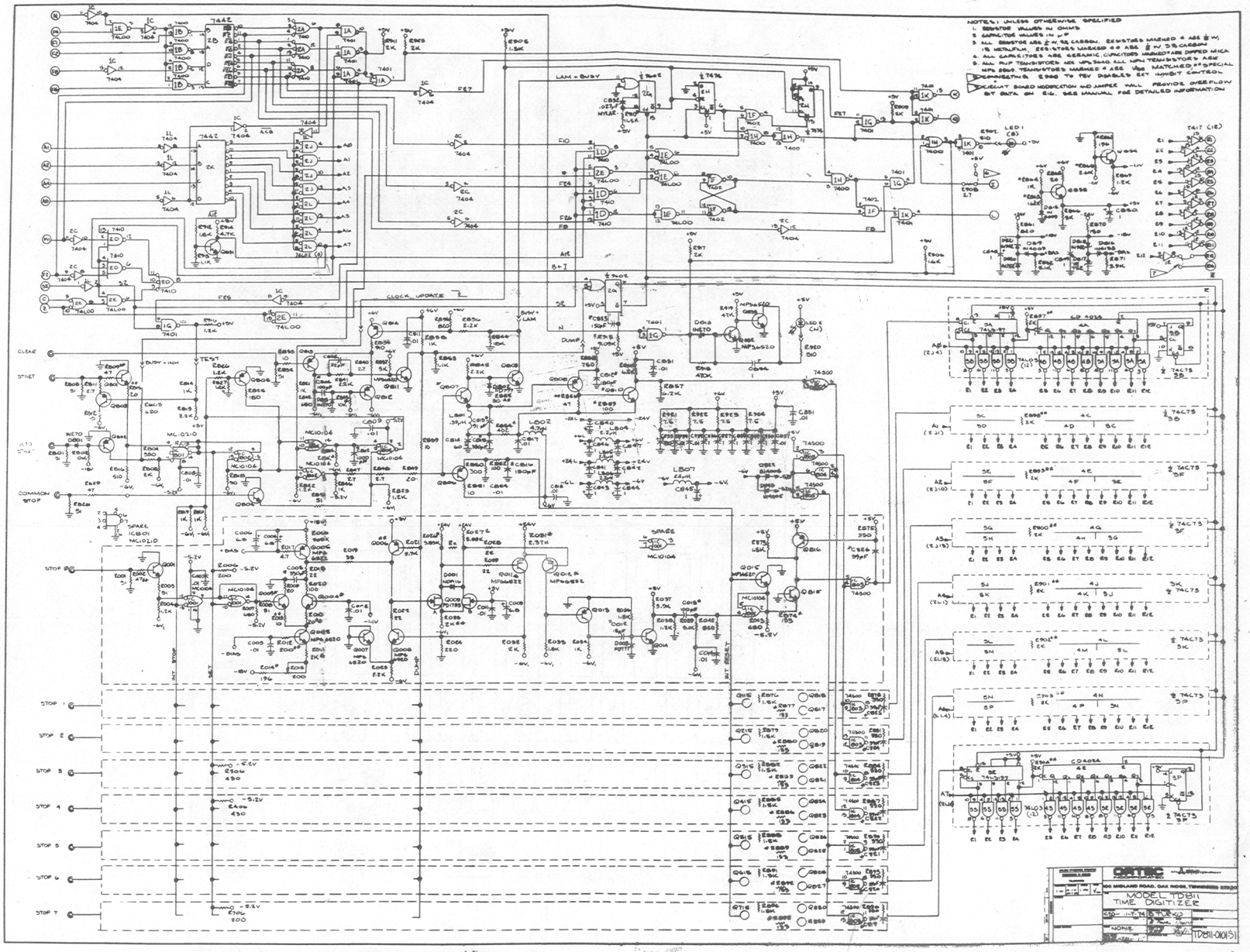
Description	ORTEC Part No.	Reference Designations
130Ω CC 1/4W 5%	40286	R870
133Ω MF 1/8W 1% T–O	40491	R874, 877, 880, 883, 886, 889, 892, 895
180Ω CC 1/4W 5%	40269	R825
196Ω MF 1/8W 1% T–O	40496	Rk14, 867
200Ω CC 1/4W 5%	40212	R006, 706
200Ω CC 1/8W 5%	60901	Rk12
200Ω 4-turn BRN Pot	49203	Rk15
220Ω CC 1/4W 5%	40213	Rk24
300Ω CC 1/4W 5%	40215	R850
330Ω CC 1/4W 5%	40216	R804, 875, 878, 881, 884, 887, 890, 893, 896
402Ω MF 1/8W 1% T–O	40506	R854
430Ω CC 1/4W 5%	40201	R306, 406
470Ω CC 1/4W 5%	40273	R918
510Ω CC 1/4W 5%	40220	R816, 907, 920
620Ω CC 1/4W 5%	40221	R803
680Ω CC 1/4W 5%	40222	Rk07, k43, 842
681Ω MF 1/8W 1% T–O	40513	Rk26, k27
750Ω CC 1/4W 5%	40223	R858
820Ω CC 1/4W 5%	40224	Rk42, 835, 861
910Ω CC 1/4W 5%	40225	R818, 834
1K CC 1/4W 5%	40226	Rk34, 814, 819, 820, 821, 838, 846
1K MF 1/8W 1% T–O	40515	R864
1.1K CC 1/4W 5%	40227	R853, 913
1.2K CC 1/4W 5%	40228	Rk04, k38, 822, 823, 826, 827, 869, 916
1.5K CC 1/4W 5%	40229	Rk36, 873, 876, 879, 882, 885, 888, 891, 894, 905
1.6K CC 1/4W 5%	40276	R906
1.62K MF 1/8W 1% T–O	40519	R863
1.8K CC 1/4W 5%	40230	Rk33, 912
2K CC 1/4W 5%	40231	Rk32, 805, 909, 911, 917, 925
2K CC 1/8W 5%	60910	Rk25, 897, 898, 899, 900, 901, 902, 903, 904
2K MF 1/8W 1% T–O	40522	Rk11
2.15K MF 1/8W 1% T–O	40523	R824
2.2K CC 1/4W 5%	40232	Rk23, 813, 836, 841, 845
2.37K MF 1/8W 1% T–O	40525	Rk31
2.61K MF 1/8W 1% T–O	40527	R868
2.7K CC 1/4W 5%	40234	Rk21
3K CC 1/4W 5%	40235	R837, 866
3.9K CC 1/4W 5%	40237	Rk37, 871
4.7K CC 1/4W 5%	40238	R914
5.1K CC 1/4W 5%	40239	Rk39, 862
6.2K CC 1/4W 5%	40259	R857, 860
9.09K MF 1/8W 1% T–O	40541	R915
10K CC 1/4W 5%	40245	R802
10K MF 1/8W 1% T–O	40545	R843
11.5K MF 1/8W 1% T–2	61694	R910
18K CC 1/4W 5%	40249	R844
47K CC 1/4W 5%	40255	R919
909K MF 1/8W 1%	43730	Rk16
Miscellaneous		
LED Indicators	60269	D1, D2
LEMO Panel Connectors	60815	12 used


STOP 0
STOP 1
STOP 2
STOP 3
START
COMMON STOP
STOP 4
STOP 5
STOP 6
STOP 7




STOP Ø
STOP 1
STOP 2
STOP 3
START
COMMON STOP
STOP 4
STOP 5
STOP 6
STOP 7
BUS BAR
IC001
IC101
IC201
IC301
IC802
IC801
IC401
IC501
IC601
IC701
IC 803
IC 804
IC 805


STOP 0
STOP 1
STOP 2
STOP 3
START
COMMON STOP
STOP 4
STOP 5
STOP 6
STOP 7


NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTOR VALUES IN OHMS
2. CAPACITOR VALUES IN μF
3. ALL RESISTORS ARE ±5% 1/8 CARBON
1/8 METALFILM. RESISTORS MARKED * ARE ± 1% 1/8 CARBON
4. ALL CAPACITORS ARE CERAMIC. CAPACITORS MARKED ** ARE DIPPED MICA
5. ALL PNP TRANSISTORS ARE MPS6520 ALL NPN TRANSISTORS ARE MPS 2369. TRANSISTORS MARKED # ARE VBE MATCHED, ## SPECIAL
6. DISCONNECTING E908 TO +5V DISABLES EXT INHIBIT CONTROL
7. CIRCUIT BOARD MODIFICATION AND JUMPER WILL PROVIDE OVERFLOW BIT DATA ON E16. SEE MANUAL FOR DETAILED INFORMATION
CLOCK UPDATE
CLEAR
START
COMMON STOP
STOP 0
STOP 1
STOP 2
STOP 3
STOP 4
STOP 5
STOP 6
STOP 7
MODEL TD811
TIME DIGITIZER
TD811-010151