1151E & 1151N

16 CHANNEL VME SCALERS

August 1993

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* * * * * * * CAUTION * * * * * * *

Before inserting the module, the user must set its base address on four rotary hex switches, making sure that the selected page is located in an unused portion of the microprocessor's memory space. The base address must be different for every module in the same systems. The first 256 bytes following the base address are allocated to the module.

Inserting the module while the VME crate is powered up can damage the scaler. Voltages of +5 and -12 must be present on the backplane with sufficient current drive to power all the inserted modules. The ventilation of the modules should be in proportion to the power consumption. Care should be taken to prevent any obstruction to the air inlets and outlets.

Due to power consumption requirements, the 1151 module must only be plugged into backplanes containing both P1 and P2 connectors.

GENERAL INFORMATION

PURPOSE

This manual is intended to provide instructions regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

The Service Documentation should be consulted for the schematics, parts lists and other material that apply to the specific version of the instrument as identified by its ECO number.

UNPACKING AND INSPECTION

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier filing a damage claim.

WARRANTY

LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts and repairs are warranted for 90 days. This warranty extends only to the original purchaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers warranty only.

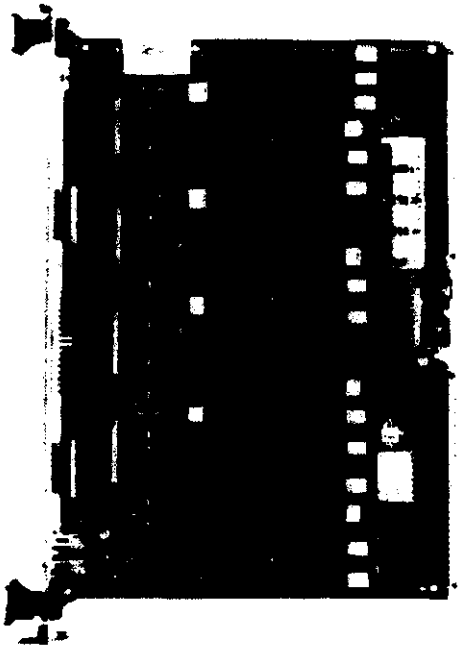
In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department or an authorized service facility within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental or consequential damages, whether in contract or otherwise.

LeCroy

1151E SCALER WITH ECL INPUTS
1151N SCALER WITH NIM INPUTS



- **High Density: 16 Channels**
- **High Speed Counting: 80 MHz**
- **NIM or ECL Versions**
- **Wide Dynamic Range: 32 Bits**
- **Flexible Operation: Common Gate for Control**
- **Bidirectional Counting with Preset**
- **Fast Readout via Standard VME**

FOR COUNTING AND PRE-SCALING IN CONTROL SYSTEMS AND EXPERIMENTS

The VME Model 1151 features 16 channels of high speed scaler to count detector pulses and logic signals from physics research experiments and monitor/control applications. High counting rates and wide dynamic range are coupled to flexible control for count up/count down requirements.

Two versions are available depending on the input signal standard and connector selected: Model 1151N for standard NIM signals via LEMO style 00 connectors; 1151E for ECL and LeCroy high density ECLine compatible signals and connectors.

The readout of this instrument is in accordance with the VME Standard (ANSI/IEEE-1014). Therefore, this scaler may be controlled and read out via standard VME hardware systems (e.g. VME Master) and software packages.

This instrument was designed by CEN SACLAY, France.

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2.0 PRODUCT DESCRIPTION

2.1 OVERVIEW

The LeCroy 1151N and 1151E VME Scaler modules were designed to count up to 16 separate channels of NIM/ECL level input pulses, respectively, from detector or logic signals, in physics research experiments and/or monitoring/controlling applications. The modules consist of 16 counting registers of 32 bit each, and have a maximum frequency of 80 MHz. Each counter can be reset to zero and placed in either an upcount or a downcount (preset count) mode. A preset count can be written into each register which automatically institutes a downcount mode, and the receipt of each input pulse would then decrement the count by 1. When any of the downcount registers reaches its terminal count (all 1's), an on-board programmable VME Bus Interrupter Module is available to interrupt the VME Bus on one of 7 interrupt levels and a NIM level TRIGOUT pulse is generated on a front-panel connector.

The TRIGOUT signal, indicates that one of the 16 channels has received a "preset count plus one" number of input pulses. The TRIGOUT signal is delayed 20 ns relative to the input pulse that causes its generation. The same condition can be used to trigger a Bus Interrupter Module which can then generate a VME Bus Interrupt under program control.

The modules conform to the VME standard for double-height boards (6U 160mm), with both P1 and P2 rear connectors. The front panel contains 16 counting inputs, the GATE input, the TRIGOUT output, and 18 LED's located near each connector to indicate the presence of the corresponding signals. Two other LEDs indicate the DTACK and BERR signals which are generated by the module on the VME Bus. See Figure 1 for details of the front-panel layout.

A VME Bus master can read the contents of the counting registers, with or without resetting them to zero, or can write in the value of the preset count and automatically force a downcount mode. A VME Bus write to a particular location or a VME Bus SYSRESET signal will reset all the registers to zero. All internal registers of the Bus Interrupter can be accessed via the VME Bus.

2.2 SPECIFICATIONS

INPUTS	16 PULSE INPUTS	to be counted during presence of GATE signal, minimum pulse width 5 ns. Model 1151N - NIM levels, matched to 50 ohms. Model 1151E - ECL level input.
	GATE	Count enable signal; NIM level input.
OUTPUTS	TRIGOUT	pulse output whenever any of the 16 registers is set to a downcount mode and is decremented to all ones, indicating that the number of input pulses during the GATE signal has reached pre-set count + 1; NIM level output.
CAPABILITY		Sixteen 32-bit binary up/down counting registers, Maximum count per register - 4,294,967,295, Maximum counting frequency - 80 MHZ
LED Displays	16 inputs(red)	denotes status of input levels.
	GATE (red)	denotes presence of GATE signal.
	TRIGOUT (red)	denotes that one of the 16 channels received preset number of input pulses during GATE signal.
	DTACK (green)	denotes module access on VME Bus.
	BERR (red)	denotes module bus error.
VME Interface		VME A24 with D16, D32 Protocol. Base address on module set by four hexadecimal switches. VME read of each count register with reset to zero. VME read of each count register without reset to zero. VME write of preset count into each count register with automatic setting of register into down-count mode. VME reset of all registers to zero.

An LED is present at each input connection, to indicate the presence of the corresponding signal. It must be noted that a single input pulse will not be discernible on the LED. A series of input pulses must occur before its presence can be viewed. Essentially, the brightness of the LED will be proportional to the the frequency of the pulses.

2.4 VME Interface

The module operates in an A24 D32/D16 mode. The address of the module must be specified in a 24-bit field and the data to and from the module can appear in either 32 or 16 bit word formats. The 6 address modifier bits (AM0 - AM5) must be either hex 3D or 39, to specify a 24 bit address field in either a supervisory or non-privileged data access mode respectively.

The base address on the module is selected by means of four hexadecimal rotary switch located on a sub-assembly that plugs into the board. Each base address (16 hi order bits) reserves a page of 256 locations (8 low order bits) for each module. The allocation of the address space within the page is shown in Figure 2.

A VME Bus D16 word write to address (BASE + 0x00) causes a Master Reset, which resets the contents of all 16 counting registers to zero and also sets all bits of the Preset Count Register to the preset count mode. For this write only, the data on the bus is disregarded.

The on board Bus Interrupter module contains eight programmable read/write registers which can be accessed from VME address (BASE + 0x10) thru (BASE + 0x1F). The 8 data bits to and from the chip are tied to the 8 low order data bits on the VME Data Bus. Accesses to odd addresses must be on a byte basis while accesses to even addresses must be on a word basis with only the low order 8 bits containing useful information.

Reading of the 16 counting registers can occur at two address fields relative to the base. In the first field, between (BASE + 0x40) and (BASE + 0x7C), the registers can be read and then automatically reset to zero. In the second field, located between (BASE + 0x80) and (BASE + 0xBC), the registers can be read without any effect on the register contents. One long word access containing 32 bits or two 16 bit word accesses, can be used.

BASE ADDRESS	FUNCTION IMPLEMENTATION
0xFE	Rev Number, Serial Number
0xFC	Manufacturer Number, Module Type
0xFA	Fixed Module ID
:	:
0xF0	:
:	:
0xBC	Read Scaler 16
0xB8	Read Scaler 15
0xB4	Read Scaler 14
0xB0	Read Scaler 13
0xAC	Read Scaler 12
0xA8	Read Scaler 11
0xA4	Read Scaler 10
0xA0	Read Scaler 9
0x9C	Read Scaler 8
0x98	Read Scaler 7
0x94	Read Scaler 6
0x90	Read Scaler 5
0x8C	Read Scaler 4
0x88	Read Scaler 3
0x84	Read Scaler 2
0x80	Read Scaler 1
:	
0x7C	Read, Reset, Write, Preset 16
0x78	Read, Reset, Write, Preset 15
0x74	Read, Reset, Write, Preset 14
0x70	Read, Reset, Write, Preset 13
0x6C	Read, Reset, Write, Preset 12
0x68	Read, Reset, Write, Preset 11
0x64	Read, Reset, Write, Preset 10
0x60	Read, Reset, Write, Preset 9
0x5C	Read, Reset, Write, Preset 8
0x58	Read, Reset, Write, Preset 7
0x54	Read, Reset, Write, Preset 6
0x50	Read, Reset, Write, Preset 5
0x4C	Read, Reset, Write, Preset 4
0x48	Read, Reset, Write, Preset 3
0x44	Read, Reset, Write, Preset 2
0x40	Read, Reset, Write, Preset 1
:	
0x1F	Generator Control
0x10	Interruptions
:	
0x00	Generate Module 0

Figure 2 Allocation of Address Space

Three locations at the highest addresses of the page are used for module identification. The coding for this data is contained in two 16L8 PAL's, each one generating 8 bits. The configuration of this information is as follows:

	15 10	9 0
BASE + 0xFC	No. of Mfg.	Module Type

	15 12	11 0
BASE + 0xFE	Revision (Def. 1)	Serial No. of Module (Def 02)

	15 8	7 0
BASE + 0xFA	0xFA	0xF5

Fixed Module Identifier

The BERR (bus error) signal will be generated when an access to an unused location or an invalid access to a used location is detected. For each VME Bus access to an address within the page, the module will respond either with a DTACK or a BERR.

Note: LeCroy Mfg # = 1 (dec)
1151E and 1151N Module Type = 7(dec)

3.0 INSTALLATION

3.1 General

The user must take into consideration the fact that operations on the front-panel are being executed in real time, and are performed asynchronously with those occurring on the VME Buses. In particular, one should avoid writing a preset value to a counting register, while the latter is in the process of counting. Reading a counting register without a reset to zero will not disturb the functioning of the counter, although the value read may be incorrect if the counter is in the process of updating.

External logic must be used to ensure the proper coordination of front end operations and those linked to the VME bus (See Section 4.5 Sequence of Operation).

The 1151 Scaler is a standard 6U 160mm VME module and can be used in any slot in a VME crate. Voltages of +5 and -12 must be present on the backplane with sufficient current drive to power all the inserted modules. The ventilation of the modules should be in proportion to the power consumption. Care should be taken to prevent any obstruction to the air inlets and outlets.

Due to power consumption requirements, the 1151 module should only be plugged into backplanes containing both P1 and P2 connectors. Inserting the module with the crate powered up must be avoided.

3.2 Setting In Base Address

Before inserting the module, the user must set its base address on four rotary hex switches, making sure that the selected page is located in an unused portion of the microprocessor's memory space. The base address must be different for every module in the same systems. The first 256 bytes following the base address are allocated to the module.

The block diagram for the test setup is shown in Figure 3. The VME Test Processor coordinates the entire operation of generating input pulse sequences and reading the results on the VME Bus. For example: A VME module, IOREG, generates two signals under control of the VME Test Processor. One is applied to the GATE input of the 1151 and the other to the input of a Pulse Generator. The Pulse Generator output is then fed into a Distributor which fans out to the 16 pulse inputs of the 1151.

4.0 Operating Instructions

4.1 Role of the Bus

Upon the startup of an acquisition program, reading the identification registers makes it possible to check the presence on the modules at the provided address space. It also facilitates the setting up of a data base in which to record the history of the module.

In the acquisition program itself, VME bus accesses permit reading the contents of any register with or without reset to zero, writing a preset count into any register, and simultaneously resetting the contents of all registers to zero.

Access to the on board bus interrupt module (BIM) is effected via the VME Bus. The BIM can be initialized and enabled to generate an interrupt when any counter in a preset mode reaches (preset count + 1).

4.2 Preset Count Register

A 16 bit register is used to store the mode of the 16 counting registers, each one of which can be either in a count (upcount) or preset count (downcount) mode. One bit is allocated per channel to establish the mode of its corresponding counting register. A bit will be set to the preset count state whenever a valid VME Bus write is performed on its counting register, either as a long word or a D16 write to either the LSB or MSB of the register. A bit will be set to the count state whenever a valid VME Bus read is performed on it's counting register, either as a long word or as a D16 read of the LSB portion. A VME Bus D16 read of the MSB portion of the countine register will not change the bit. A master reset will place all 16 counting registers in the preset count mode. This register is comprised of two 8 bit addressable latch chips (74H259).

4.3 Format of the data

32 bit Transfers

The 32 bits of each counter can be accessed at addresses BASE + 0x40, BASE +0 x44, BASE + 0x7C (read with reset to zero/ write) or at addresses BASE + 0x80, BASE + 0x84, BASE + 0xBC (read only with no reset) on date bits 0 - 31.

- The TRIGOUT signal can be used to close the GATE.
- Since counters in preset count mode continue downcounting after reaching (preset count + 1) if the GATE is open, the count of the total number of input pulses will be accurate.
- The read program can re-initialize the module and restart the counting.

4.6 Software

After choosing the base address of the module by means of the on-board rotary switches, the absolute addresses corresponding to the labels (symbolic names) used in the program must be determined.

4.7 Bus Interrupter Module

The Bus Interrupter Module (BIM) is a Motorola MC68153 programmable device that is VME Bus compatible and is capable of generating interrupt requests on the 7 interrupt levels of the VME Bus. It is triggered to be the same condition that causes a TRIGOUT signal, i.e. any of the resisters in a preset count mode reaching the preset count + 1. The module can be programmed via the VME Bus to generate an interrupt request on any or none of the 7 VME Bus interrupt levels as a result of its receipt of a trigger. It will also supply an interrupt vector in response to an interrupt acknowledge from a System Interrupt Handler.

In response to valid VME Bus accesses to the BIM, the latter will generate its own DTACK signal, which is "ORed" with the DTACK signal for valid non-BIM accesses to produce the VME Bus DTACK.

4.8 Programming

For systems using one of Motorola's 68000 family of microprocessors access to the counter registers will generally be by means of a MOVE.L (move 32 bit long word) instruction. With certain precautions, two MOVE.W (move 16 bit word) instructions may be used.

To effect a Master Reset, a write word cycle (.W) to address (BASE + 0x00) of the module should be executed. The CLEAR instruction is to be avoided due to the fact that, on some 680xx's, this instruction causes a read followed by a write cycle. The read cycle to (BASE + 0x00) would trigger a BERR signal.

ADDRESS	MODE		RESPONSE	FUNCTION EXECUTED
BASE+0x00	Write	L	BERR	No action
	Read	L	BERR	No action
	Write	W	DTACK	Even or odd word, total Module Reset
	Read	W	BERR	No action
	Write	B	BERR	Even or odd byte, no action
	Read	B	BERR	Even or odd byte, no action
BASE+0x10 to BASE+0x1F	Read	L	BERR	No action
	Write	L	BERR	No action
	Read	W	DTACK	Read registers of BIM
	Write	W	DTACK	Write to registers of BIM
	Read	B	BERR	Even byte, no action
		B	DTACK	Odd byte, read BIM registers
	Write	B	BERR	Even byte, no action
		B	DTACK	Odd byte, write BIM registers
BASE+0x40 to BASE+0x7C	Read	L	DTACK	Read 32 bits of counter w/reset to zero and place counter in count mode.
	Write	L	DTACK	Write 32 bit preset count & place counter in preset count mode.
	Read	W	DTACK	Even word, read 16 MSB's w/no reset.
		W	DTACK	Odd word, read 16 LSB's w/reset to zero & set counter to count mode.
	Write	W	DTACK	Even word, write 16 MSB's & place counter into preset count mode.
	Read	B	BERR	Odd or even byte, no action.
	Write	B	BERR	Odd or even byte, no action.
BASE+0x80 to BASE+0xBC	Read	L	DTACK	Read 32 bits of counter w/no reset
	Write	L	BERR	No action
	Read	W	DTACK	Even word, read 16 MSB's w/no reset.
		W	DTACK	Odd work, read 16 LSB's w/no reset.
	Write	W	BERR	Even or odd word, no action.
	Read	B	BERR	Odd or even byte, no action.
	Write	B	BERR	Odd or even byte, no action.
BASE+0xFA	Read	L,B	BERR	No action
	Write	L,B	BERR	No action
	Read	L,B	DTACK	Validation 0xFAF5
	Write	W	BERR	No action

Figure: 4: Memory Map

5.0 Theory of Operation

5.1 Introduction

The 1151 module is made up of two intermeshed systems. One section of circuits operates in real time to count the number of incoming pulses present at the front-panel coincident with a common gate signal. Another section of circuits operates under control of the VME Bus to setup the counters, and then read and/or reset their contents. The external logic must coordinate the interaction of these two systems to provide meaningful test data.

This module is chiefly implemented in "FAST" TTL logic. A block diagram appears in Figure 5 below. Double lines are used to denote connections to the VME Bus.

5.2. Real Time System

This circuitry operates on the 16 counting inputs, the GATE input, and the TRIGOUT output. It contains the 16 counting registers with their associated controls, the 16 input signal level/TTL level converters, and the TRIGOUT generator.

5.2.1 Level Converters

Model 1151N - The NIM level input signals enter via 17 front- panel LEMO coaxial connectors terminated in 50 Ω resistors. The conversion from NIM level to TTL level is accomplished in two stages. Each NIM signal is applied to the base of an NPN 2N918 transistor (Count inputs to T1 - T16, GATE input to T17), whose emitter output provides a level shift of -700 mv. The NIM input voltage range of 0/-800 mV is thus shifted to -700 mV/-1500 mV, compatible with standard ECL levels. These ECL level signals are then fed into 10H125 ECL/TTL converters (IC3, IC6, IC9, IC12, IC36) whose TTL outputs are applied to the coincidence circuits.

Model 1151E - The 16 ECL level input signals enter via a 34 pin flat signals are fed directly into the 10H125 ECL/TTL converters (IC3, IC6, IC9 IC12). The NIM level GATE input enters via a front panel LEMO connector and is applied to transistor T17 and ECL/TTL converter IC36.

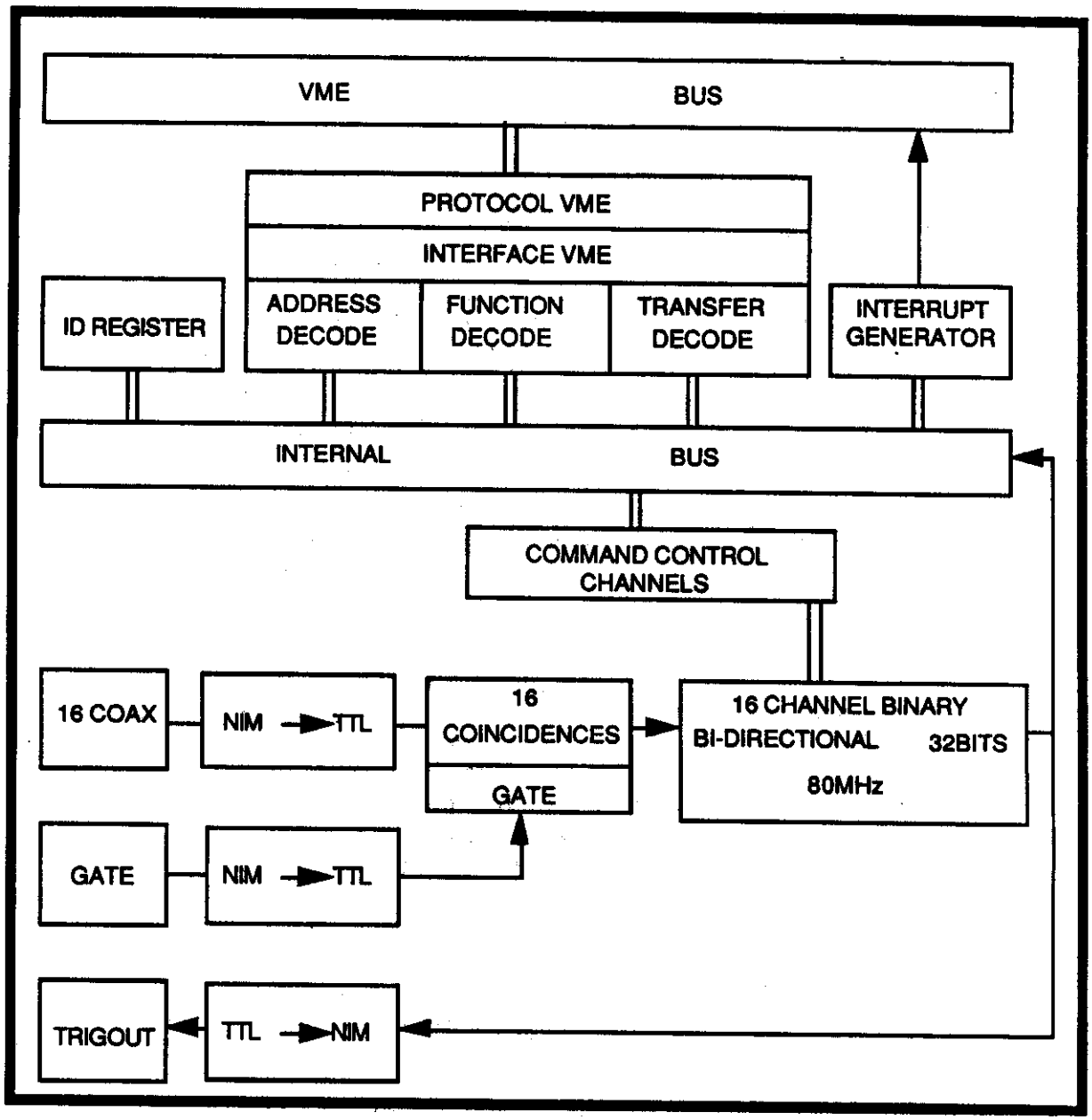


Figure 5 Block Diagram of the 1151 Scaler

5.4 VME BUS FUNCTIONS

5.4.1 Address Decoding

A subassembly on the board contains four hex rotary switches, two 74F520 8 bit comparators and two 74ALS138 1 of 8 decoders. The 16 most significant bits of the VME Bus address (A8 to A23) are compared on a bit by bit basis with the settings of the four hex rotary switches and an output generated when all 16 bits compare. In addition, VME Bus address bits A4 to A7 are decoded during the above compare and generate 16 additional outputs, which are not used in the current design.

VME Bus address bits A8 to A23 are used to select the base address of the module and reserve a page of 256 bytes. Figure 3 shows the address assignments within the page. The least significant address bits (A1 - A7) are buffered by a 74F244 chip (IC159) and applied to PAL (IC156) which decodes the functions used. The latter generates the VALEC (valid read) and VALWR (valid write) signals which set up VME Bus data transfers.

The VME Bus address modifiers, AM0 to AM5, are decoded by (IC128) and combined with the base address decode and VME Bus signal as to produce the VALADR (Valid Address) signal for the decoding PAL. IC156 and IC28 also supplies the signal IACKAS to the BIM module, indicating the initiation of an interrupt acknowledge cycle.

5.4.2 Function Decoding

VME Bus function decoding takes place in IC156. Two 74F244 bus receivers (IC147 and IC159) provide buffering between the VME Bus and the internal bus. IC156 utilizes internal bus signals INA1 - INA7, INWR, INLWRD, INRESET, INDS0 and INDS1, in conjunction with the VALADR signal of the PAL (IC128).

When the PAL decodes a VME Bus access that is not executable, due to an unused address, an unacceptable format, or an invalid write, it will generate the INBERR signal. When the PAL decodes an executable operation, it will generate both the appropriate decode signal and also the INDTACK signal.

zeroes. The 16 zeroes for the LSB's are derived from 74F244 bus drivers IC38 and IC59. These 16 zeroes are transferred to the MSB's by means of 74F245 transceivers IC76 and IC109. The reset signals are delayed 35 ns relative to the read by means of "ANDing" the INSD0 and INDS1 signals in a 74LS20 (IC137) and then delaying the output in a 74LS31 (IC155). PAL's IC130, IC135, IC139 and IC143 set up the register for a write.

During a 16 bit word read, the zero reset of the entire register occurs only after the LSB read. Therefore, the MSB should read first.

The RAZTOT signal, generated upon decode of a word write to BASE + 0x0 or upon receipt of the SYSRESET signal, resets all registers to zero by the same procedure described above. PAL's IC39, IC44, IC49 and IC54 generate the clock signals necessary for the write.

Write of Preset Count

PAL's IC130, IC135, IC139 and IC143 set up the addressed register for a write cycle. The signals VALWR and BYPASWR control VME writes to either 2 or 4 stages of the register. A write to a register automatically sets the corresponding bit in the 16 bit preset count register (IC133 and IC154) to the preset count (downcount) mode.

Read of the Three Identifier Words

PAL IC156 generates the LECIDEN (Read Identifier) signal. This signal enables two 16L8 PAL's labeled IC126 and IC127, to feed out one of three stored 16 bit words onto the data bus, each PAL supplying 8 bits. The PALs decode address bits INA1, INA2, and INA3 and respond with one of three unique words only if 0xA, 0xC, or 0xE, corresponding to 32 bit addresses BASE + 0xFA, BASE + 0xFC, or BASE + 0xFE, is detected.

5.4.4 Generating VME Bus Protocol

The signals VALEC and VALWR, generated by IC156 control read and write paths, respectively, between the internal data bus and the VME data bus.

The signal BYPASLEC, generated by PAL IC156, controls feeding the 16 MSB's of the internal data bus onto the 16 LSB's of the VME Bus during even address 16 bit reads. The signal BYPASWR, also generated by IC156 controls feeding the 16 LSB's on the VME Bus onto the 16 MSB's of the internal data bus during even address writes.

Address	D7	D6	D5	D4	D3	D2	D1	D0	Register
ADB + 0x11			0**	1*		L2	L1	L0	Control Register 0
ADB + 0x13	x	x	x	x	x	x	x	x	not used
ADB + 0x15	x	x	x	x	x	x	x	x	not used
ADB + 0x17	x	x	x	x	x	x	x	x	not used
ADB + 0x19	V7	V6	V5	V4	V3	V2	V1	V0	Control Vector 0
ADB + 0x1b	x	x	x	x	x	x	x	x	not used
ADB + 0x1D	x	x	x	x	x	x	x	x	not used
ADB + 0x1F	x	x	x	x	x	x	x	x	not used

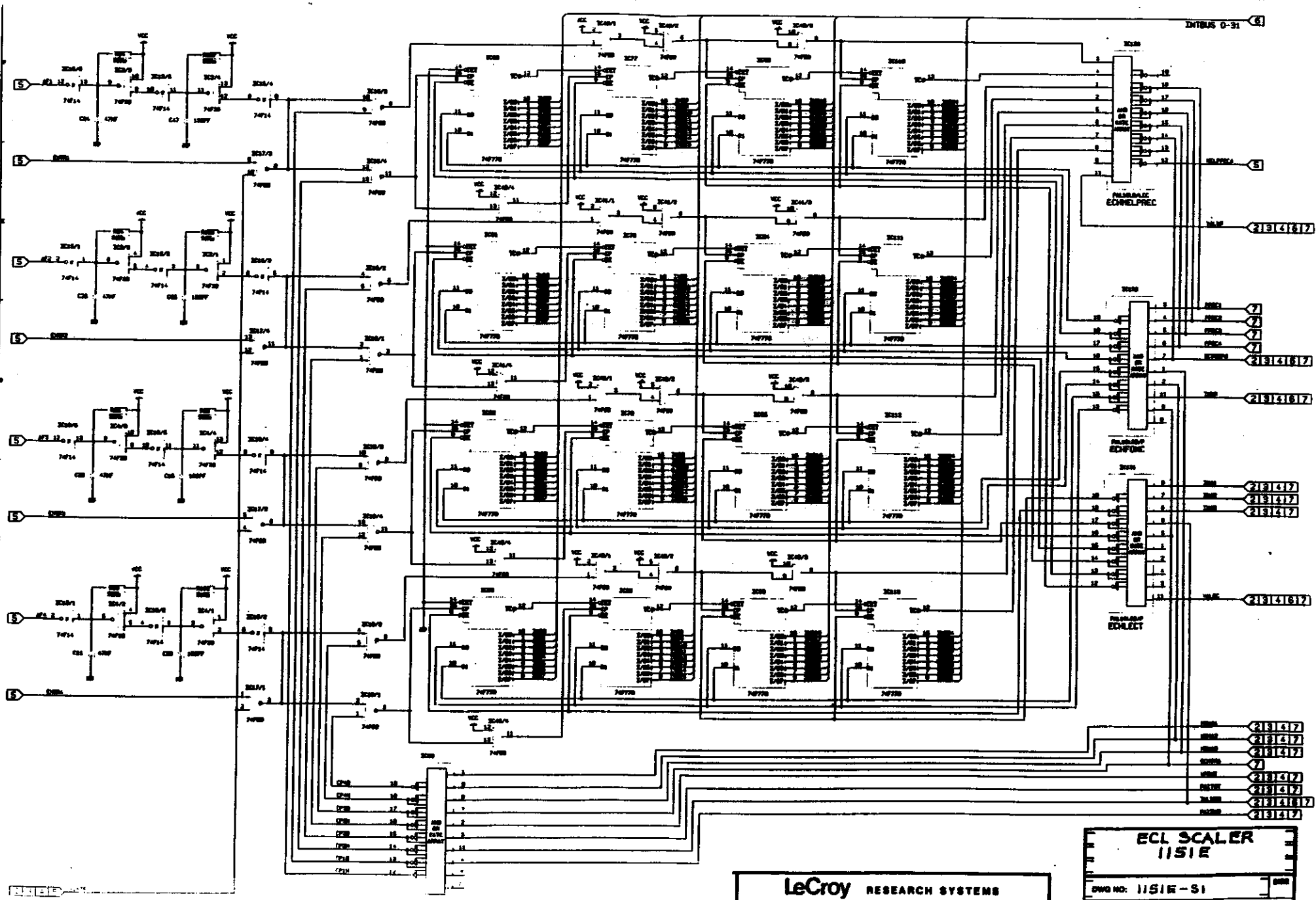
* To enable interrupts
** To enable DTACK and vector data responses

During the interrupt acknowledge cycle, the IC148 74F74 will get reset by the RIT signal from IC128 as a result of the BIM INTAE signal.

5.6 LED Indications

The two signals INDTACK and INBERR drive two 74123 1 ms monostable circuits (IC1) whose outputs feed LED's. R63 and CH2 control the one-shot timing for DTACK, while R38 and CH1 do likewise for BERR. Thus, the green LED for DTACK and the red LED for BERR will light for 1 ms each time their respective signals are sent. 16 LEDs, situated close to the 16 count inputs, indicate the presence of the input signals. There are also 2 LED's to indicate thepresence of the GATE input signal and TRIGOUT output signal, each situated close to its respective connector.

PART NUMBER	DESCRIPTION	QUANTITY PER
102412151	CAP CERA DISC 100V 150 PF	18
103326473	CAP CERA MONO 50V .047UF	18
103327103	CAP CERA MONO 50V .01 UF	53
140493105	CAP TANT METAL CASE 1 UF	2
146424106	CAP MINI ALUM 20% 10 UF	3
161225101	RES CARBON FILM 100 OHMS	4
161225150	RES CARBON FILM 15 OHMS	1
161225224	RES CARBON FILM 220 K	2
161225331	RES CARBON FILM 330 OHMS	2
161225390	RES CARBON FILM 39 OHMS	2
161225470	RES CARBON FILM 47 OHMS	1
161225471	RES CARBON FILM 470 OHMS	1
161225510	RES CARBON FILM 51 OHMS	3
161225513	RES CARBON FILM 51 K	36
161225561	RES CARBON FILM 560 OHMS	2
161225681	RES CARBON FILM 680 OHMS	1
190042102	RESISTOR NETWORK 1 K	1
190892510	RESISTOR NETWORK 51 OHMS	6
205790910	IC 24 MACRO EPLD EP910	1
207244124	IC QUAD TTL-MECL 10H124	1
207244125	IC QUAD MECL-TTL 10H125	5
208127001	IC VOLT REG -5.2V 7905.2	1
227168153	IC MICRO BUS INTER 68153	1
230110005	DIODE SWITCHING 1N4448	2
256233209	DIODE LED RED TIL209A	1
256532232	DIODE LED (GRN) TIL232-1	1
270171918	TRANSISTOR NPN 2N918	3
400381040	SOCKET IC SOLD TAIL DIP-40	3
402130001	CONN RT ANGL PC MTG LEMO	2
403119234	HDR DBL ROW RT ANGL 34	1
405812002	SOCKET STRIP SOLDR 20 POS	2
413120001	SWITCH 16-POS MICRO BCD DIP	4
454311032	HDR SOLD TAIL/MALE 32	2
454610096	HDR SOLD TAIL/MALE 96	2
500860302	INSULATOR FOR TO-220	1
550125110	SCREW PAN HD M2.5X10	5
552425100	NUT HEX M2.5	5
574409005	WASHER SHOULDER NYLON #4	1
711151001	PC BD PREASS'Y 1151E	1
711151011	PC BD PREASS'Y 1151E-1	1
721151002	FRONT PNL TAB BOT PREASS'Y 1151E	1
721151003	FRONT PNL PREASS'Y 1151E	1
721151022	FRONT PNL TAB TOP PREASS'Y 1151N	1
SM200172000	IC 2-INPUT NAND 74F00	14
SM200172008	IC AND GATE 74F08	16
SM200172014	IC HEX INV 74F14	9
SM200172038	IC 2-IN NAND 74F38	12
SM200172074	IC D-TYP FLOP 74F74	1
SM200172259	IC 8-BIT DMUX/LATCH 74F259	2
SM200173138	IC DECODER 74ALS138	2
SM200174020	IC 4-IN NAND 74LS20	1
SM200174031	IC DELAY ELEMENT 74LS31	1
SM200272779	IC 8-BIT UP/DN BIN COUNTER 74F779	64
SM200274123	IC MONOST MULTIVIBR LS123	1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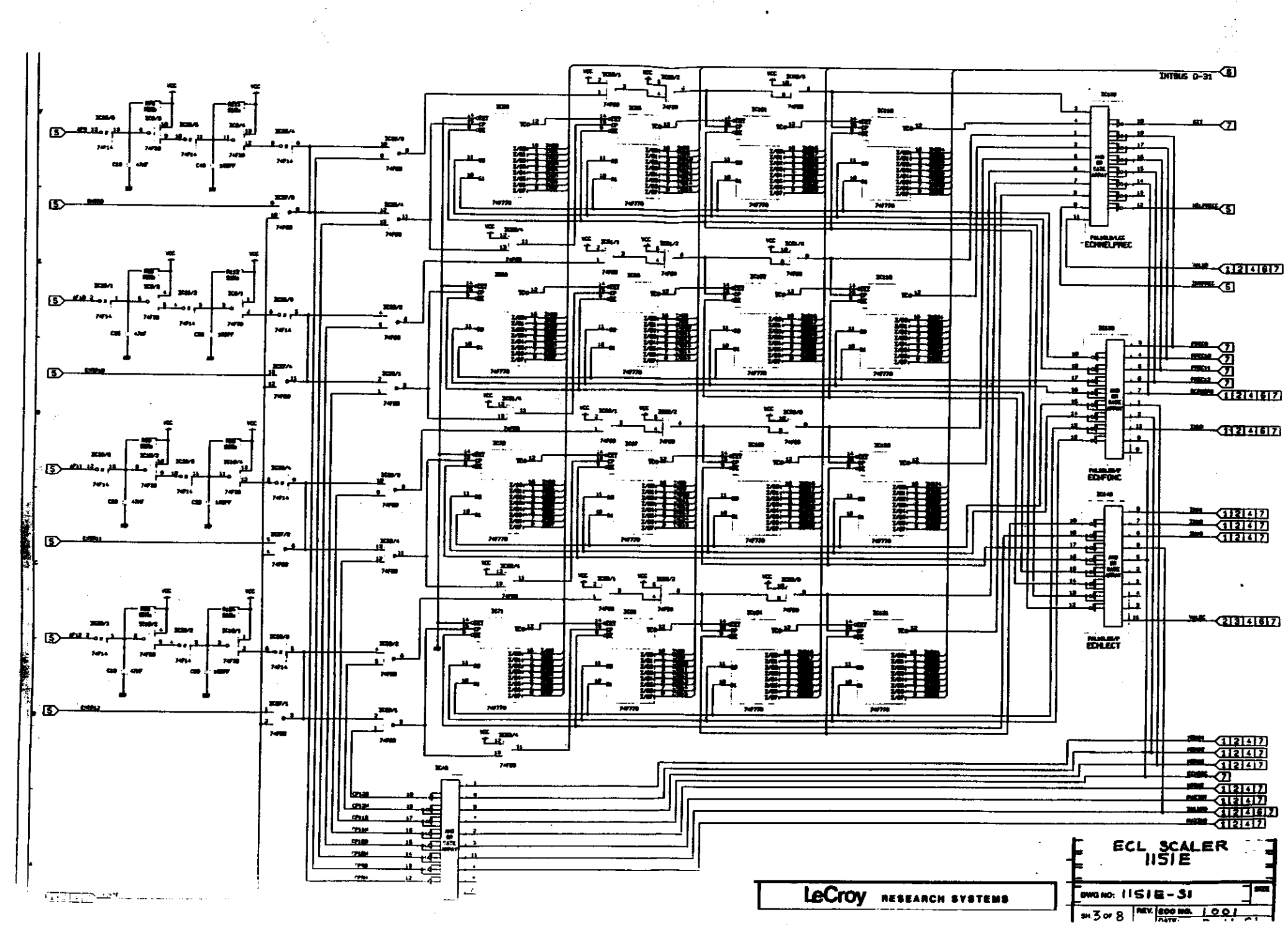
ECL SCALER
1151E
DWG NO: 1151E-S1
REV
ECO NO. 1001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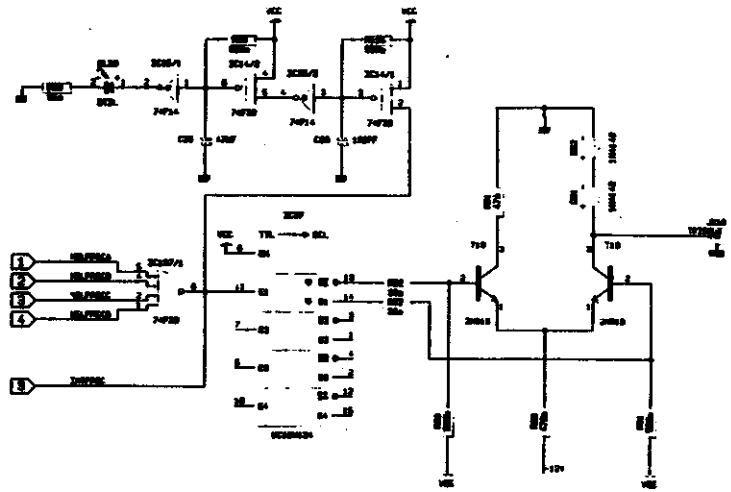
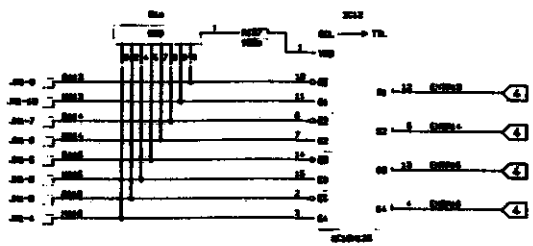
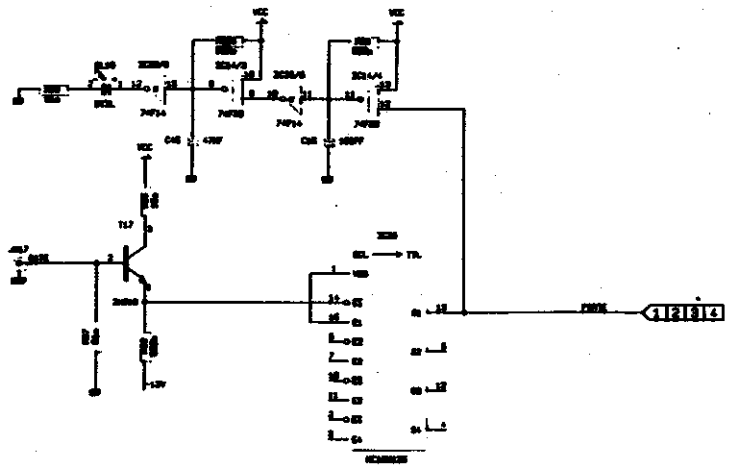
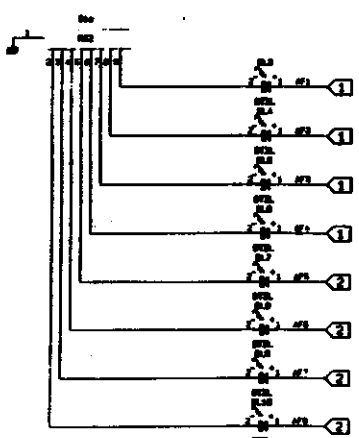
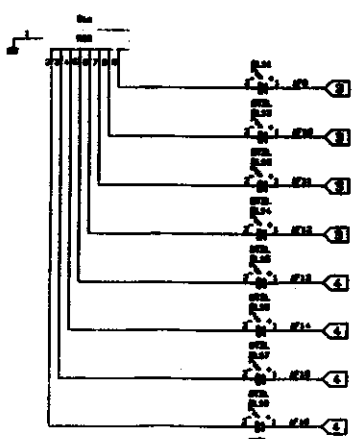
1151E
LeCroy RESEARCH SYSTEMS
DWG NO: 1151E-31
SH 3 OF 8
REV.
ECO NO. 1001









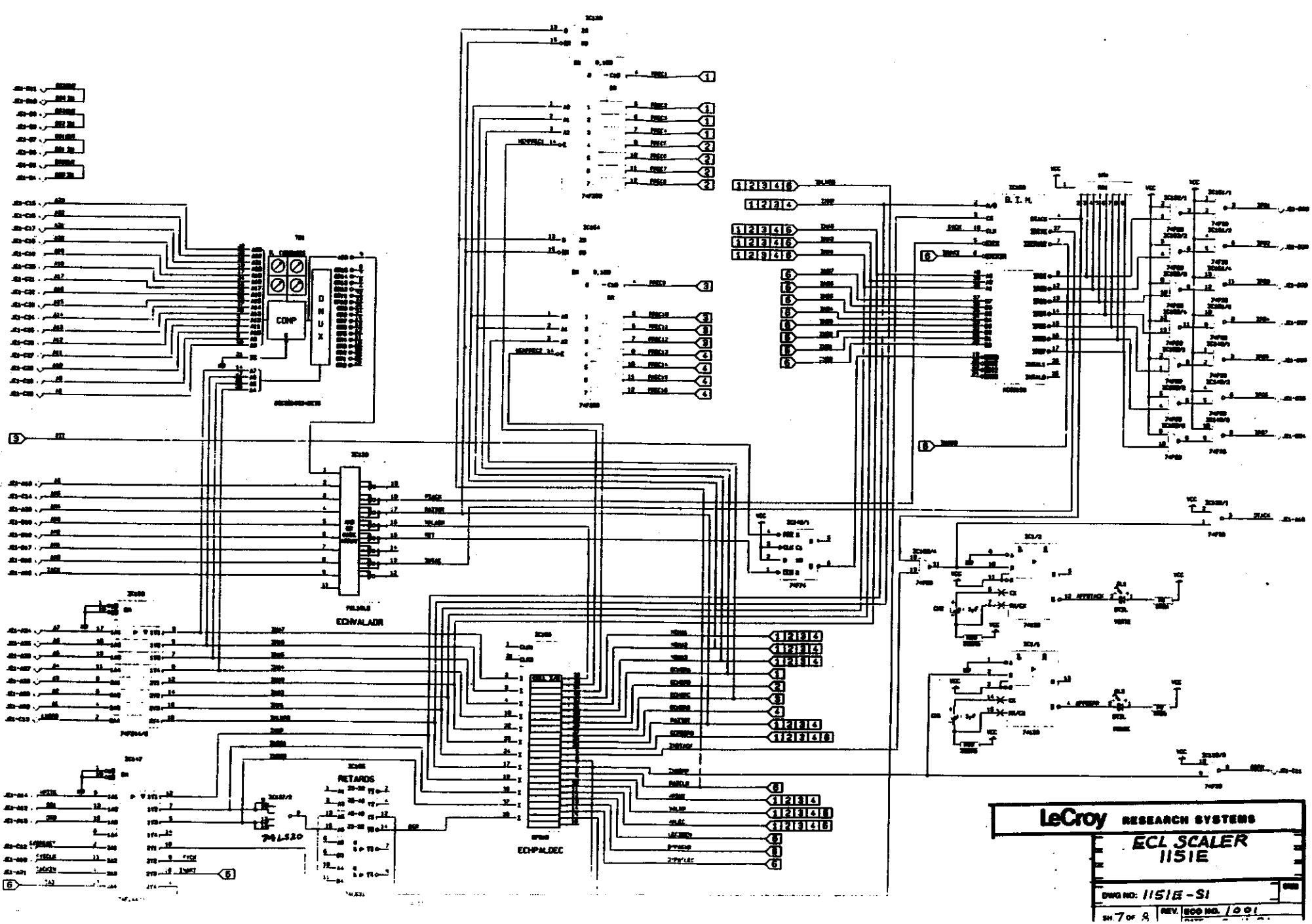


LeCroy RESEARCH SYSTEMS

ECL SCALER
1151E

DWG NO: 1151E-S1

SH. 6 OF 8 | REV. | ECO NO. 1001 | DATE: 2-11-91



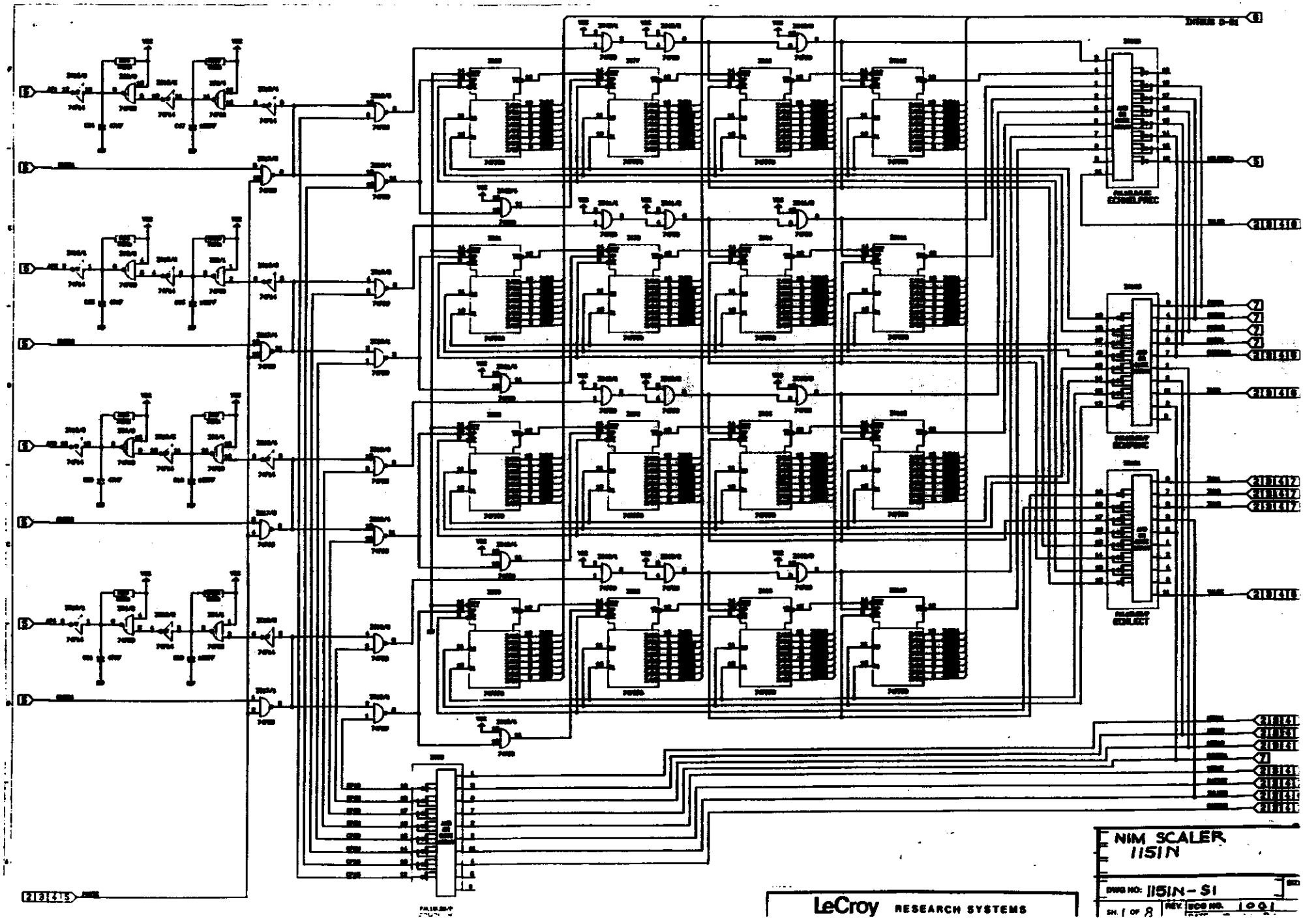
LeCroy RESEARCH SYSTEMS

ECL SCALER
1151E

DWG NO: 1151E-SI

SH 7 OF 8 | REV. | ECO NO. 1001

PART NUMBER	DESCRIPTION	QUANTITY PER
102412151	CAP CERA DISC 100V 150 PF	18
103326473	CAP CERA MONO 50V .047UF	18
103327103	CAP CERA MONO 50V .01 UF	53
140493105	CAP TANT METAL CASE 1 UF	2
146424106	CAP MINI ALUM 20% 10 UF	3
161225150	RES CARBON FILM 15 OHMS	17
161225224	RES CARBON FILM 220 K	2
161225331	RES CARBON FILM 330 OHMS	2
161225390	RES CARBON FILM 39 OHMS	2
161225470	RES CARBON FILM 47 OHMS	1
161225471	RES CARBON FILM 470 OHMS	1
161225510	RES CARBON FILM 51 OHMS	35
161225513	RES CARBON FILM 51 K	36
161225561	RES CARBON FILM 560 OHMS	2
161225681	RES CARBON FILM 680 OHMS	17
190042102	RESISTOR NETWORK 1 K	1
205790910	IC 24 MACRO EPLD EP910	1
207244124	IC QUAD TTL-MECL 10H124	1
207244125	IC QUAD MECL-TTL 10H125	5
208127001	IC VOLT REG -5.2V 7905.2	1
227168153	IC MICRO BUS INTER 68153	1
230110005	DIODE SWITCHING 1N4448	2
256233209	DIODE LED RED TIL209A	1
256532232	DIODE LED (GRN) TIL232-1	1
270171918	TRANSISTOR NPN 2N918	19
400381040	SOCKET IC SOLD TAIL DIP-40	3
402130001	CONN RT ANGL PC MTG LEMO	18
413120001	SWITCH 16-POS MICRO BCD DIP	4
454311032	HDR SOLD TAIL/MALE 32	2
454610096	HDR SOLD TAIL/MALE 96	2
500860302	INSULATOR FOR TO-220	1
540407000	VME PANEL EJECTOR KIT	1
550125110	SCREW PAN HD M2.5X10	5
552425100	NUT HEX M2.5	5
574409005	WASHER SHOULDER NYLON #4	1
711151011	PC BD PREASS'Y 1151E-1	1
711151021	PC BD PREASS'Y 1151N	1
721151021	FRONT PNL PREASS'Y 1151N	1
721151022	FRONT PNL TAB TOP PREASS'Y 1151N	1
721151023	FRONT PNL TAB BOT PREASS'Y 1151N	1
SM200172000	IC 2-INPUT NAND 74F00	14
SM200172008	IC AND GATE 74F08	16
SM200172014	IC HEX INV 74F14	9
SM200172038	IC 2-IN NAND 74F38	12
SM200172074	IC D-TYP FLOP 74F74	1
SM200172259	IC 8-BIT DMUX/LATCH 74F259	2
SM200173138	IC DECODER 74ALS138	2
SM200174020	IC 4-IN NAND 74LS20	1
SM200174031	IC DELAY ELEMENT 74LS31	1
SM200272779	IC 8-BIT UP/DN BIN COUNTER 74F779	64
SM200274123	IC MONOST MULTIVIBR LS123	1
SM200372520	IC 8-BIT COMP 74F520	2
SM205720116	IC PAL 16L8-7A	4
SM205720168	IC PAL-C 16L8-25	16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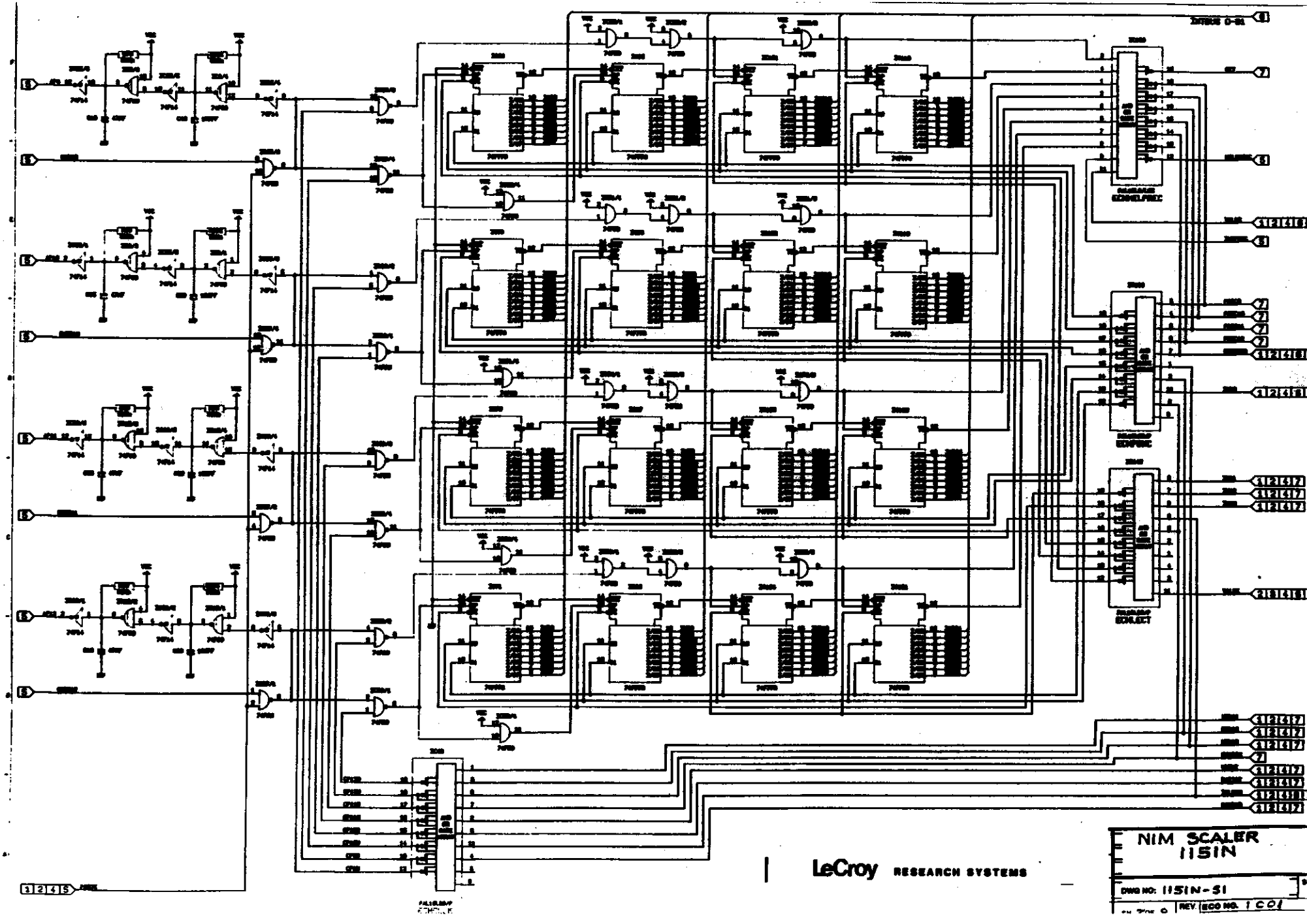
1151N
DWG NO: 1151N-S1
SH. 1 OF 8
REV.
ECO NO. 1001
LeCroy RESEARCH SYSTEMS



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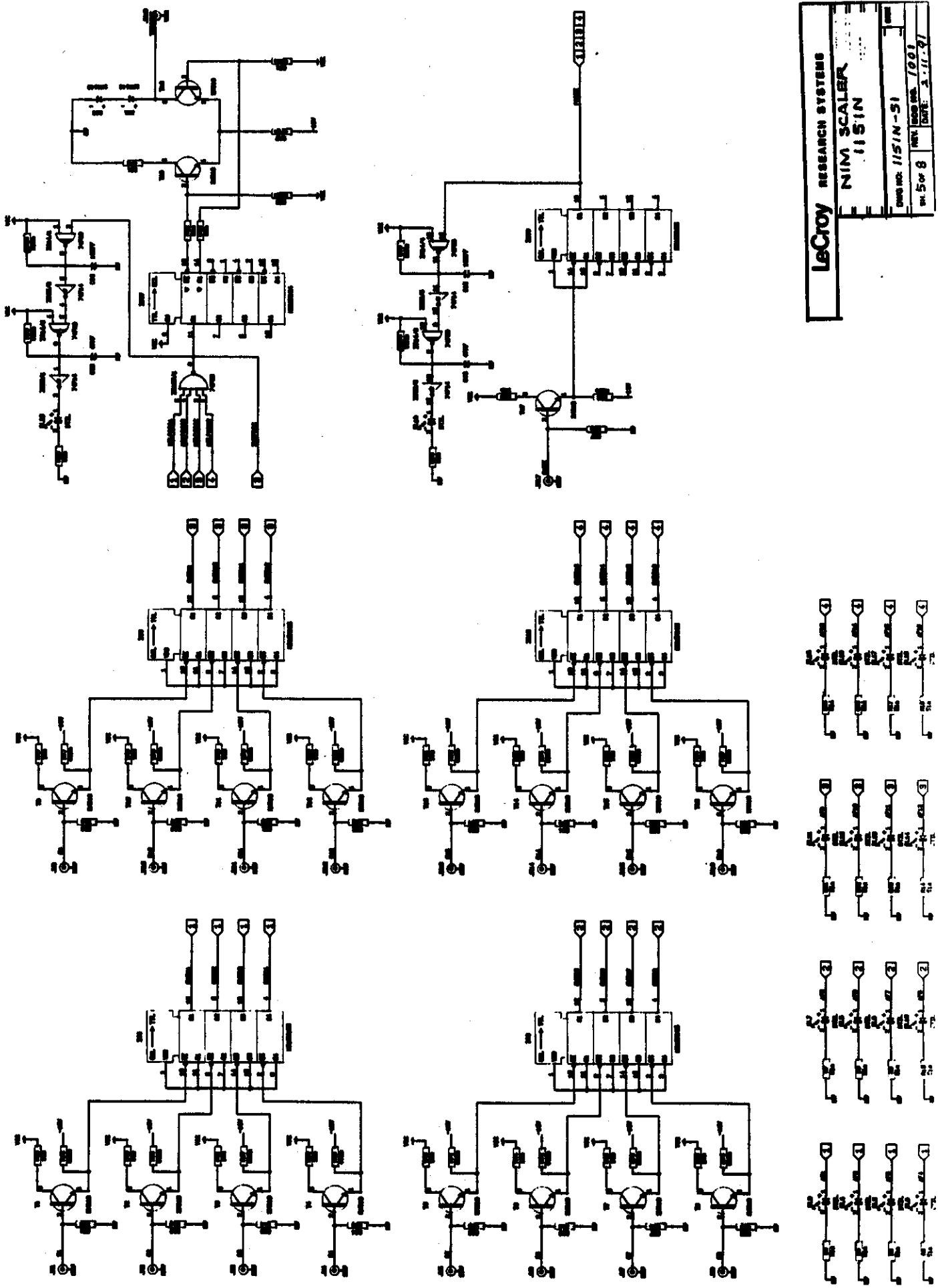
NIM SCALER
1151N

DWG NO: 1151N-51

REV. ECO NO. 1 C01


LeCroy RESEARCH SYSTEMS
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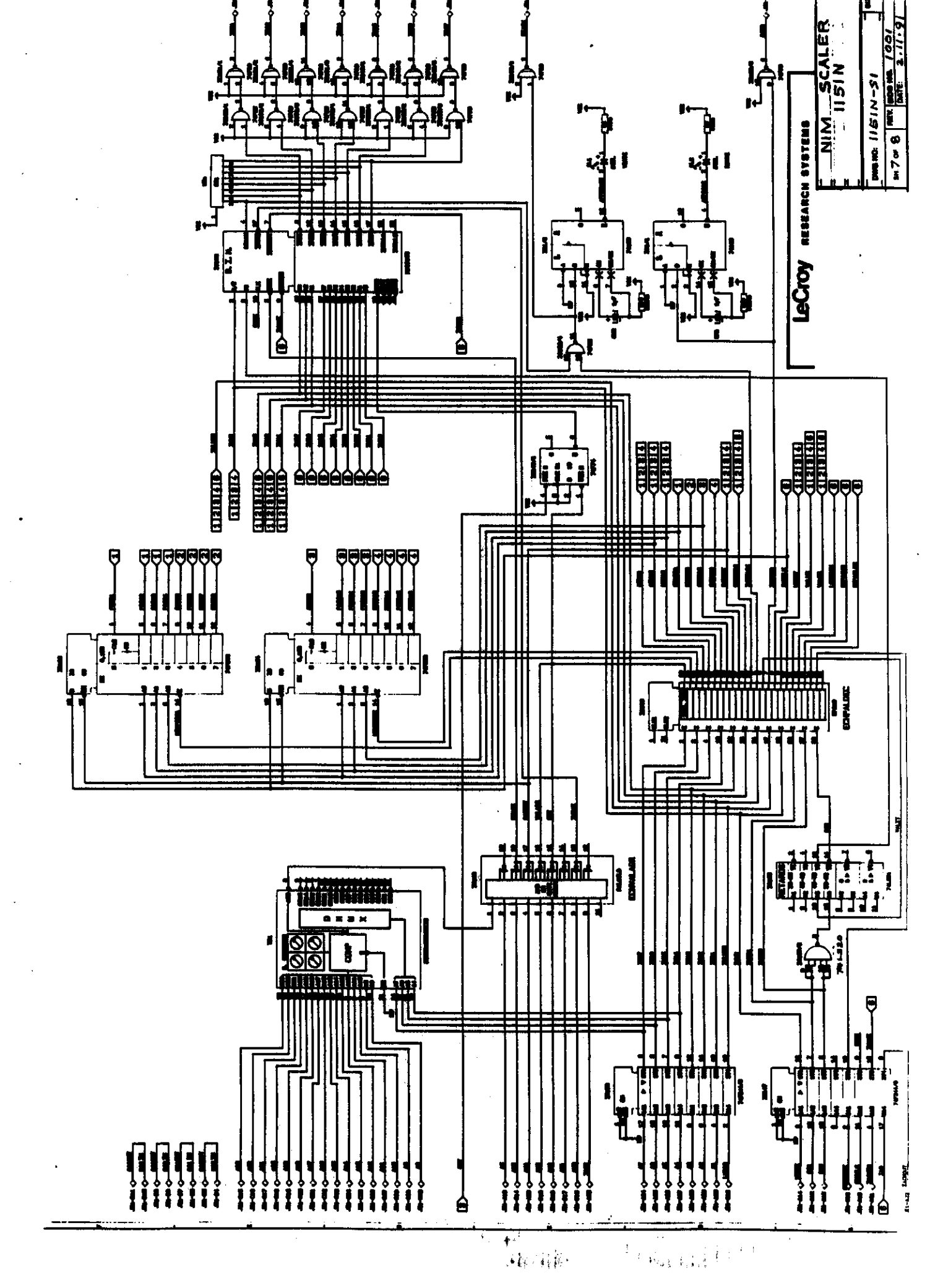
REV 1001
SH 5 OF 8
DATE 2/11/81


LeCroy RESEARCH SYSTEMS
NIM SCALER
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DWG NO: 1151N-51
REV: 1001
SH 7 OF 8
DATE: 2.11.91