MODEL 2228A/2229

OCTAL TIME-TO-DIGITAL CONVERTER

Revised
February, 1985

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ALL SHIPMENTS OF LECROY INSTRUMENTS FOR REPAIR OR ADJUSTMENT should be made via Air Freight or "Best Way" prepaid. The instrument should be shipped in the original packing carton; or if it is not available, use any suitable container that is rigid and of adequate size. If a substitute container is used, the instrument should be wrapped in paper and surrounded with at least four inches of excelsior or similar shock-absorbing material.

A T T E N T I O N

THE 2228A AND 2229 SHOULD ALWAYS BE INITIALIZED WITH AN F(24) (Disable LAM) OR AN F(26) (Enable LAM) AND AN F(10) (Clear LAM) WHENEVER THE CRATE POWER IS TURNED ON.

CRATE POWER SHOULD BE TURNED OFF DURING INSERTION AND REMOVAL OF UNIT TO AVOID POSSIBLE DAMAGE CAUSED BY MOMENTARY MISALIGNMENT OF CONTACTS.

SEE POCKET IN BACK OF MANUAL FOR SCHEMATICS, PARTS LISTS AND ADDITIONAL ADDENDA WITH ANY CHANGES TO MANUAL.

A T T E N T I O N

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TECHNICAL DATA

LeCroy

CAMAC ECLine Model 2229
Octal Time-to-Digital Converter

- **8 channels in single-width module**
- **Complementary ECL inputs and strobes**
- **11-bit resolution**
- **Full-scale time ranges — 100, 200, and 500 nsec**
- **Time resolutions — 50, 100, or 250 psec/count**
- **Rejects stops before starts**
- **Fast Clear input**
- **Internal test capability**
- **Common stop input for precision testing**
- **Q and LAM suppression**

The LeCroy Model 2229 is an Octal Time-to-Digital Converter, packaged in a single width CAMAC module. It incorporates all the advanced operating characteristics which experience has indicated necessary for accurate and reliable measurement of nanosecond time intervals. It employs the new ECLine logic standard resulting in cabling convenience and economy.

The Model 2229 has 8 independent channels, each of which measures the time from the leading edge of a Common Start pulse to the leading edge of its individual Stop pulse. Any stop pulses received before Start signal are ignored and only one Stop is accepted for every Start.

Conversion begins upon receipt of the start signal and proceeds until one of the following: a stop signal is received; the cycle is terminated by the application of a front-panel Fast Clear signal; or the TDC reaches full scale.

The 2229 converts the measured time intervals into a 11-bit digital number at the rate of 20 MHz, for a full scale digitizing time of 100 microseconds. Rear-panel control of full-scale and conversion slope permits digitization to fewer bits and a shorter conversion time if desired. The conversion clock is started in phase with the TDC start signal to assure synchronization and eliminate the inaccuracy introduced by the free-running oscillators in conventional designs. LAM, if enabled, is generated at the end of the conversion interval.

The 2229 has three switch-selectable full-scale time ranges, 100, 200, and 500 nsec, which are digitized to 95% of 11 bits (2048 channels) and provide 50, 100, and 250 psec resolutions respectively. Longer time ranges (up to 10 microseconds) may be provided on request at slight expense of stability and accuracy.

On line testing is facilitated by either a front-panel Common Stop input or F(25). A signal at the Common Stop input generates simultaneous stops for each channel, permitting accurate testing of both front end and scaler section of the module and uniform system testing and time calibration. F(25) is provided for a quick test of the front end and scaler sections with a time measurement of 80% of full scale.

In high rate or colliding beam experiments, excessive system deadtime due to false starts may be eliminated through use of the 2229's fast clear input. Accepting ECL level signals, this input allows the TDC to be cleared at any point in its conversion cycle without the necessity for any Dataway operations.

All standard LAM functions are available in the 2229 to facilitate data readout. To minimize readout time, both Q and LAM may be suppressed if the module does not contain data.

November 1982

Innovators in Instrumentation

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TWX: 710-577-2832 CABLE: LERESCO TELEPHONE: (914) 425-2000

SPECIFICATIONS
CAMAC Model 2229
OCTAL TIME-TO-DIGITAL CONVERTER

Stop Inputs:	Eight, using a 2 × 8 pin connector (mates with LeCroy 403211016 or 3M 3452-6016 or equivalent); accepts differential ECL input levels; 110 Ω input impedance pin-to-pin; direct coupled; 5 nsec minimum width; inputs ignored unless preceded by a "Start" input.
Common Start Input:	One, common to all channels, using a pin pair on the control group (2 × 8-pin) connector (mates with LeCroy 403211016 or 3M 3452-6016 or equivalent); accepts differential ECL input levels; 112 Ω input impedance pin to pin; direct coupled; 5 nsec minimum width.
Common Stop Input:	One, common to all channels, input characteristics identical to Common Stop. Functions identical to the individual Stop inputs above, used for on-line testing.
Fast Clear:	One, common to all channels, input characteristics identical to Common Stop except 50 nsec minimum width. Requires 1.4 μsec after start of clear signal to settle to 1 ± 1 counts. (However, if the unit is always cleared at a fixed time before each start, it will settle to a constant offset with a small uncertainty, effectively permitting fast reset times on the order of 500 nsec).
Full-Scale Time Range:	11-bit binary output corresponds to 100, 200, and 500 nsec nominal, switch-selectable (with longest range field-adjustable up to 1 μsec). Larger full-scale possible by factory option up to 10 μsec. Both the full-scale value and conversion slope are rear-panel adjustable, permitting faster conversion at the expense of range.
Integral Non-linearity:	< ± 2 counts (20 nsec to full scale).
Differential Non-linearity:	Channel widths vary by < ± 10% (10 nsec to full scale). < ± 30% for long-range option.
Time Resolution:	50 psec on 100 nsec range; 100 psec on 200 nsec range; 250 psec on 500 nsec range.
Temperature Coefficient:	Typically (± 0.02% of full scale ± 0.01% of reading) per degree C.
Digitizing Time:	Approximately 100 μsec for 11 bits; rear-panel adjustable for fewer bits, shorter conversion time.
Readout Time:	Readout may proceed at the fastest rate permitted by the CAMAC standard after digitizing is complete.
Test Functions:	An internal start/stop is generated with approximately 80% of full scale time in response to an F(25) command. On-line testing and calibrations can be done with common start and common stop above.
Data:	The proper CAMAC function and address command gates the binary data of the selected channel onto the R(1) to R(11) (2^0 to 2^{10}) Dataway bus lines. The full-scale number of bits, and thus the conversion time, can be selected by a rear-panel pot and test point. The overflow flag is always presented on R(12).
CAMAC Commands:	Z or C: All registers are simultaneously cleared by the CAMAC "Clear" or "Initialize" command. Requires "S2". I: "Start" input is inhibited during CAMAC "inhibit" command. Q: A Q = 1 response is generated in recognition of an F(0) or F(2) Read function, or an F(8) function if LAM is set for a valid "N" and "A", but there will be no response (Q = 0) under any other condition. The Q response for empty modules is suppressed (see Q and LAM suppression). X: An X = 1 (Command Accepted) response is generated when a valid F, N, and A command is generated. L: Look-At-Me signal is generated from end of digitizing until a module Clear or Clear LAM. LAM is disabled for duration of N, can be permanently enabled or disabled by the Enable or Disable function command, and can be tested by Test LAM. Switch-selectable option causes LAM to be suppressed by empty modules.
CAMAC Function Codes:	F(0): Read registers; requires N and A. A(0) through A(7) are used for channel address. F(2): Read registers and clear module; requires N, A, and S2. Clears on A(7) only. F(8): Test Look-At-Me; requires LAM, N and any A from A(0) to A(7). Q is Generated if LAM is present and enabled. F(9): Clear module (and LAM); requires N and any A from A(0) to A(7), and S2. F(10): Clear Look-At-Me; requires N, S2 and any A from A(0) to A(7). F(24): Disable Look-At-Me; requires N, S2 and any A from A(0) to A(7). F(25): Test module; requires N, S2 and any A from A(0) to A(7). F(26): Enable Look-At-Me; requires N, S2 and any A from A(0) to A(7). Remains enabled until Z or F(24) applied. Caution: The state of the LAM mask will be arbitrary after power turn-on.
Q and LAM Suppression:	A module receiving no stop inputs will produce no Q response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The Q and LAM suppress features can be disabled with side-panel switches.
Packaging:	In conformance with CAMAC standard for nuclear modules. (ESONE Report EUR4100 or IEEE Report #583). RF-shielded CAMAC #1 module.
Power Requirements:	+ 24 V at 25 mA − 24 V at 140 mA + 6 V at 600 mA − 6 V at 600 mA.

SPECIFICATIONS SUBJECT TO CHANGE

SECTION 1

SPECIFICATIONS

1.2 Introduction

The LRS Model 2228A and 2229 TDC modules contain eight complete time-to-digital converters in a single-width CAMAC module. The time-to-digital conversion is accomplished in two steps. A capacitor is charged up by a constant current source initiated by the common start pulse and terminated by the stop pulse. The total charge delivered to the capacitor is an analog representation of the time interval to be measured. An analog-to-digital conversion is then performed by using the Wilkinson rundown method. In this technique, the charge is removed from the capacitor at a constant rate during which time pulses from an oscillator are gated into a scaler. The final count is thus proportional to the time interval measured.

1.3 Inputs

The eight Stop inputs of the 2228A require standard NIM levels supplied via coax, terminated at the individual 50 ohm Lemo-type connectors. The eight Stop inputs of the 2229 require differential ECL levels supplied via twisted pair or flat ribbon cable that is terminated in 112 Ω at a dual eight pin connector. These cables (Model CST 34/16) may be ordered from the factory or built by the user (see Figure 1.2). Note that if the module driving the 34 pin end of this cable conforms to the ECLine standard, then a half twist in this cable will be necessary.

Pulses at these inputs define the end of the timing intervals for the eight channels. The Stop input pulses should be a minimum of 5 nsec Full Width at Half Maximum. Since an accidental Stop pulse overlapping the Start will cause the channel to ignore the real Start pulse a short Stop pulse width is recommend to minimize this possibility.

The Common Start, Common Stop and Common Clear of the 2228A each accept NIM pulses and are terminated in 50 Ω at Lemo-type connectors. In the 2229, these three common signals use three pairs of a five pair ribbon cable that is optionally terminated in 112 Ω at a dual eight pin connector. The SIP Termination resistor package can be removed via the side panel access (a storage location is provided for this SIP at the bottom of the module) allowing use of a multiconnector ribbon cable "daisy chaining" all Common inputs of several 2229 modules. This requires only one driver per 16 modules, but it is important that the last and only the last connector be terminated. Total cable length should be minimized (i.e., < 2 meters) for minimum pulse distortion and module to module delay. However the user may find that a small amount of slack should be allowed in the daisy chain between each module to allow easy removal of one module from the chain. A cable (Model CST 34/10-L shown in Figure 1.3) suitable for driving the Common inputs to twenty-four 2229 modules is available from LeCroy.

A pulse applied to the Common Start input begins the timing measurement unless it is held in an inhibited condition by the CAMAC I (Inhibit) command.

A pulse applied to the Common Stop input will stop all inputs and is intended for calibration and test use (see Section 2.2).

1.4 Full Scale Count

The Full Scale Count can be adjusted by a rear panel potentiometer. The range is from 250 to 1950 counts (about 8 to 11 bits). A voltage proportional to the Full Scale is provided at a rear panel test point. To get a more accurate setting, test the TDC with a Start pulse and no Stop pulse. A graph of the Full Scale Count vs V_{BFS} (Test Point Voltage) is shown in Figure 1.1.

1.5 Conversion Gain

Three Conversion Gain ranges can be selected by a switch on the side panel. These are factory set for 50, 100 and 250 psec/count. These correspond to Full Scale Input times of 100, 200 and 500 nanoseconds. The 250 psec/count range can be extended to 500 psec/count by the trim pot provided. (Temperature Drift is increased by up to a factor of 4 by this method. If a more stable method is desired, see Section 2.3 on Extended Time Ranges).

1.6 Offset

Although the devices are selected at the testing stage to get a close match on offsets, the TDC is not absolutely calibrated. This means the offsets will vary from channel-to-channel and board-to-board. The typical offset is 7 ±2 nsec, when measured from the Common Start to the individual stops at the front panel. Offsets measured with Individual Stops vs. Common Stop will also differ slightly.

On its most sensitive range the 2228A and 2229 will resolve 50 pS per count. The time required for an electrical signal to travel approximately 1/2 inch is 50 psec in 50 Ω cable or on a printed circuit board. Additionally, propagation times for the gating circuitry may vary by 3 ns or more (60 counts) per device.

1.7 Conversion Time and Fast Clear

Conversion time for the 2228A and 2229 is approximately .05 μsec X Full Scale Count + 1 μsec. Maximum conversion time is, therefore, approximately 100 μsec. For an 8 bit conversion this time is reduced to about 14 μsec.

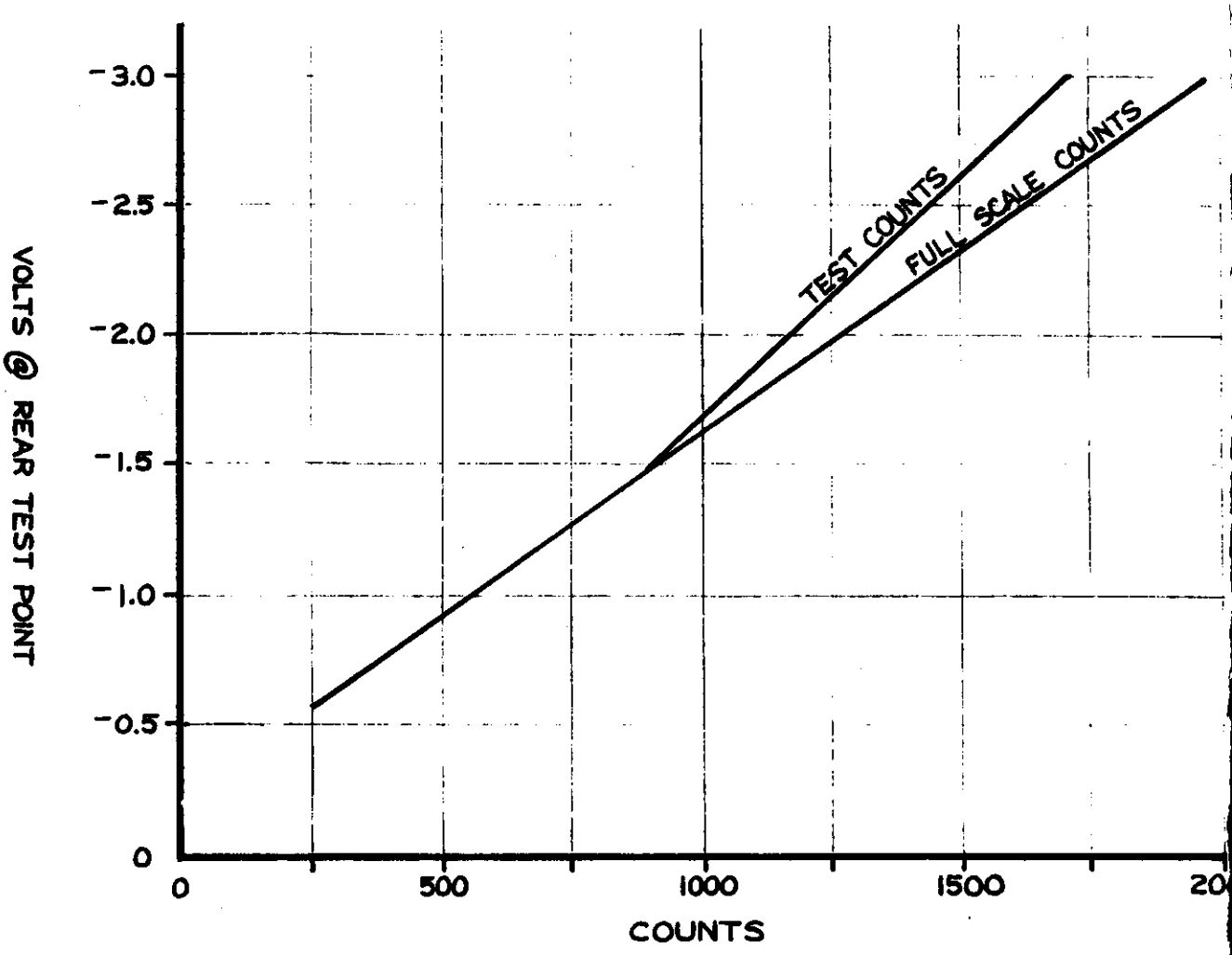
1.8 Clear

A Clear command, either CAMAC F(9) or front panel (50 nsec minimum), can be used to clear the 2228A or 2229 at any time. A waiting time of approximately 2 μsec is required to settle within 1 count of the proper value.

The fast clear signal forces all 8 channels of the unit to cease their conversions and be cleared and ready to accept another start pulse after the wait time. The fast clear feature allows TDC conversion to be initiated by a fast trigger and completed only if the event satisfies a complete trigger requirement.

1.9 Packaging and Power Requirements

The 2228A and 2229 are packaged in standard #1 width CAMAC modules (conforming to ESONE Committee Report EUR4100). Each dissipates a total of 8.3 watts of power.



FULL SCALE vs. TEST POINT VOLTAGE

TEST VALUE (F25) vs. TEST POINT VOLTAGE

Figure 1.1

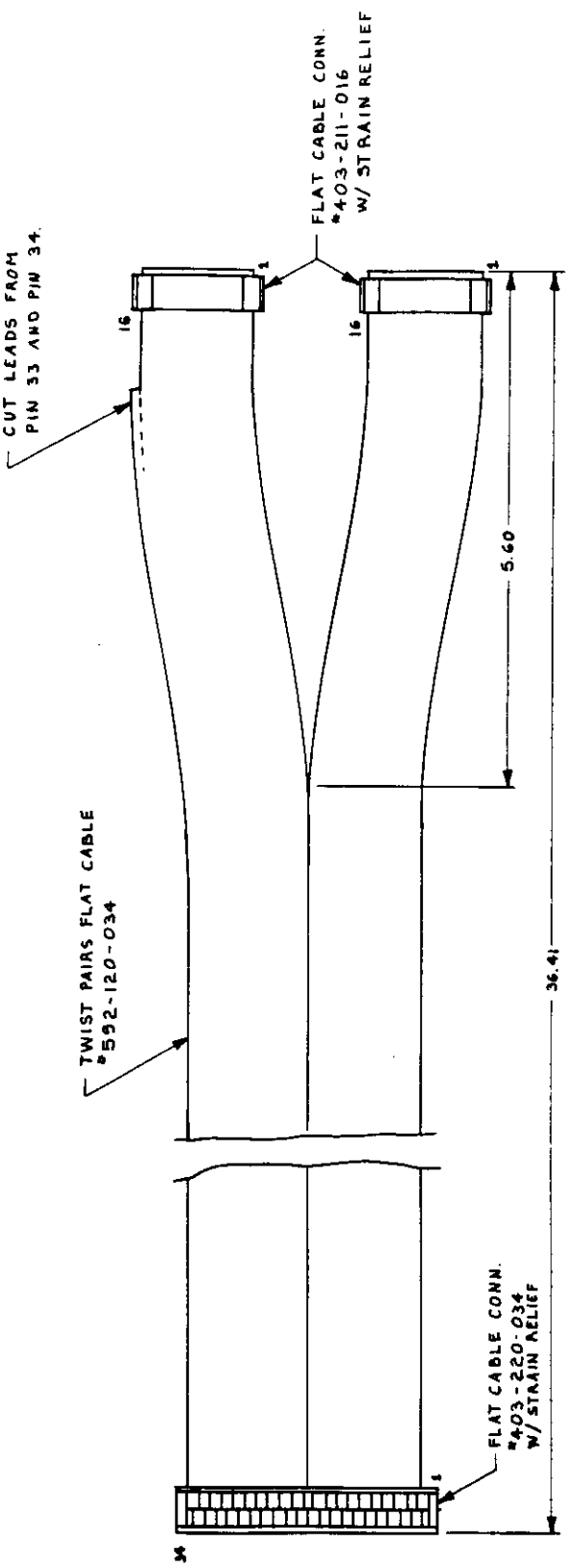

FLAT CABLE CONN.
#403-211-016
W/ STRAIN RELIEF
CUT LEADS FROM
PIN 33 AND PIN 34.
16
16
1
1
5.60
36.41
TWIST PAIRS FLAT CABLE
#592-120-034
FLAT CABLE CONN.
#403-220-034
W/ STRAIN RELIEF
1
34

Figure 1.2

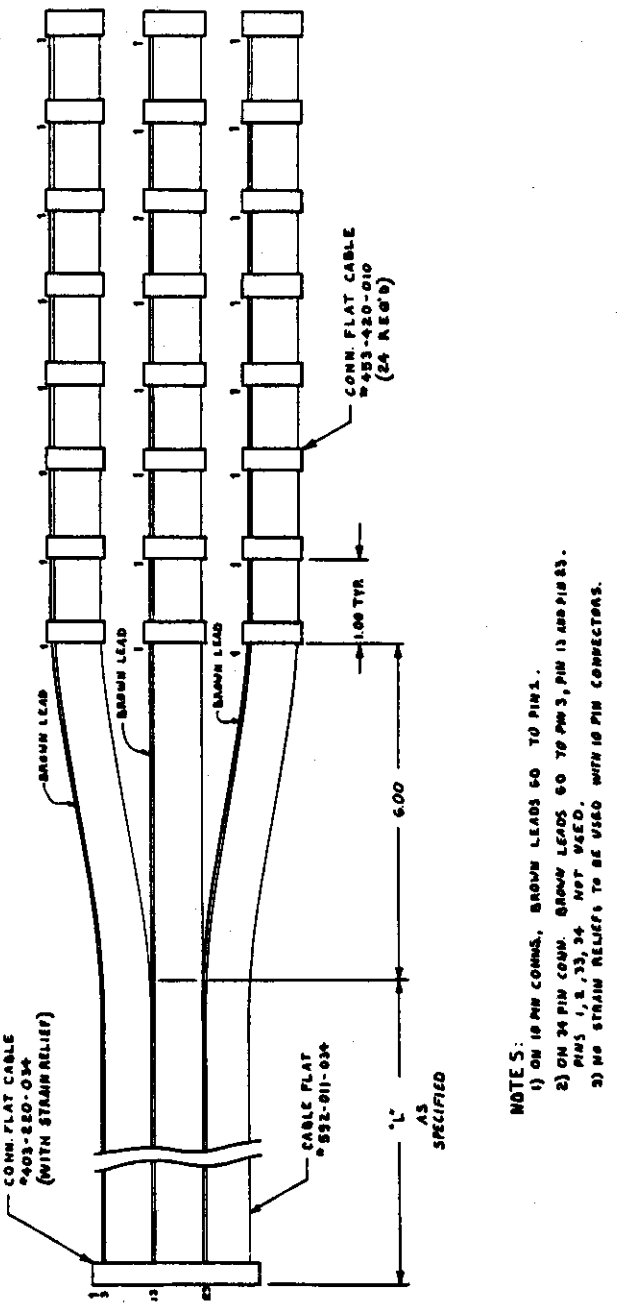

CONN. FLAT CABLE
*403-020-034
(WITH STRAIN RELIEF)
BROWN LEAD
BROWN LEAD
BROWN LEAD
CONN. FLAT CABLE
*453-420-010
(24 REQ'D)
1.00 TYP
6.00
'L'
AS
SPECIFIED
CABLE FLAT
*552-011-034
NOTES:
1) ON 10 PIN CONNS., BROWN LEADS GO TO PIN 1.
2) ON 24 PIN CONN. BROWN LEADS GO TO PIN 3, PIN 13 AND PIN 23.
PINS 1, 2, 13, 24 NOT USED.
3) NO STRAIN RELIEFS TO BE USED WITH 10 PIN CONNECTORS.

Figure 1-3

SECTION 2

A USER GUIDE TO OPERATION OF THE 2228A AND 2229

2.1 Data Readout Techniques

The data output is standard CAMAC-compatible (TTL negative logic) in 11-Bit binary format plus overflow. The digitized information is gated onto the R1 to R11 (2^0 to 2^{10}) and the overflow flag onto R12 of the Dataway bus by F(0)•N•A, where F(0) signifies the read function, N signifies the module to be read and A (from A(0) to A(7)) signifies which TDC channel in the module is to be read out. Generally, the unit is ready for readout when the LAM appears. The function F(2), Read and Clear, may also be used to read information from selected TDC channels. This readout is destructive only when A(7) is addressed.

The F(2)•N•A(7) clears all channels at one time. The F(2) command on addresses A(0) through A(6) will cause the TDC contents to be read with no clear and the input gate will remain disabled.

There are three basic types of readout schemes that can be used: read all channels, read all channels in only those modules having a LAM and read only those channels that have a LAM.

The first method, read all channels, allows for use of direct memory access which is simple to use and allows for read cycle times at maximum CAMAC or CPU rates. It requires a large memory and also requires sorting the data later to throw out the channels that overflowed.

The second method allows skipping of empty modules by using the Q and LAM suppression if all channels in the module overflowed (i.e., no valid data). This method does not allow the use of DMA since some logical decisions must be made based on LAM. However, for low "hit" rates, the readout may be faster and the amount of data to sort later is reduced.

The third method allows reading only those individual channels with valid data. This is accomplished by having the LAM reflect the status of the channels selected by the subaddress lines ("A" lines). Typically the read-out proceeds as follows: The A lines are set to the selected subaddress (for example read A(X) in an empty slot). The LAM status word is then read and checked to see if any modules have data. If data is available, a read cycle is started for the same A and the appropriate N's. When this is complete the computer advances to the next subaddress. This also requires logical decisions on LAM so DMA cannot be used but only valid data is put into memory. No further data compacting is needed.

The graph in Figure 2.1 shows example readout times per crate for the various readout schemes. It is based on 16 TDC's per crate, 3 μsec per DMA cycle and a software controlled read cycle of 20 μsec. Since the Read and DMA cycle times may be much different from those used in this example, it is recommended that the user investigate the available readout techniques to find the one best suited to his application.

2.2 Test Function

The Model 2228A/2229 offers two choices of on-line testing. The first method involves the use of the Common Stop input. A pulse applied to this input will simultaneously stop all channels. It is important to note that this Common Stop pulse will terminate the timing interval 4.5 +0.5 nsec later than if the same pulse were applied to the separate $\overline{\text{Stop}}$ inputs.

During the precision on-line testing using this Common Stop input, it is still possible for the individual Stop inputs to independently stop their respective channels earlier. It is, therefore, recommended that the normal Stop pulse sources be vetoed (inhibited) during the testing time.

A second method of performing on-line testing is via the CAMAC function F(25). Upon application of F(25)•N•A (any A from A0 to A7) at S2 time, an internal Start and Stop is generated, defining a time increment of approximately 75% of full scale for all 8 channels. Once again, a Stop input at any of the 8 channels will also terminate the time interval for that channel. For this reason, the sources of the stop pulses (logic units or discriminators) should be inhibited during testing, or multiple tests should be made to assure that no spurious pulses stopped any channel short of the full testing interval.

2.3 Using the TDC at >500 nsec Full Scale Settings

The Model TDC begins charging its integrating capacitor upon receipt of the Common Start pulse. A constant current source rundown also begins immediately. On the standard unit, an automatic stop is generated at about 1.2 times the full scale time range setting after the Common Start pulse (for channels which received no Stop input) and the oscillator is automatically started. Since the rundown began when the Start pulse was received, a number of 50 nsec-spaced clock pulses (20 MHz clock) will not be counted. This introduces a small constant time offset into the result (See Figure 2.2) which can be calibrated out by using different cable lengths for Start and Stop inputs (this also should be done to compensate for the minimum internal offset of approximately 7.0 nsec).

For users desiring a 500 psec/count range (achieved simply by readjusting the 250 psec/count range potentiometer) such as might be needed for drift chamber applications, this effect would total 24 counts or approximately 2.4%. Compensation for this would necessitate an additional 12 nsec of delay cable. To eliminate this necessity, it is possible, by moving one jumper, *for the TDC to trigger the oscillator with the leading edge of the start input. Turning on the oscillator within the timing interval causes some oscillatory noise which affects the integrating capacitor. Although this noise would affect the linearity of measurements using a 100 nsec full scale range, it is integrated out in the 1 μsec range and in the end contributes quite negligibly to integral non-linearities. Using this jumper option will also adversely affect the differential linearity of the TDC. For example the user may see more even than odd numbered TDC readings because even numbered "bin" widths may become slightly larger than odd bins. The integral linearity remains good because the average bin width is unaffected.

The effect described above is especially noticeable in units modified for extended time ranges as described in the next section.

2.3.1 Optional: Extended Time Ranges

The Model 2228A and 2229 are available at extra cost with a factory installed option providing .5, 1 and 2.5 nsec/count time ranges (order Mod 200 version).

2.4 Start-Stop Input Time Jitter and Drift

Each Start and Stop input has a "threshold" level which is affected by several factors (e.g., the base-emitter drop of an input emitter follower in the 2228A, etc.). If these factors were to change with temperature, voltage, or time variations this would cause triggering at a different amplitude level. Since the rise time of the input pulses is not equal to zero the result is a small time jitter and/or drift. The effect is worse for input pulses of longer risetimes. However, in the 2228A and 2229, the circuitry accepting the stop pulses and start pulses is identical (i.e., in the example above, although the base emitter drop does change by some small amount (=2 mV/°C), it changes nearly equally for both start and stop inputs). Therefore, if care is taken to use identical pulses (i.e., same risetime) for the start and stop inputs, the relative time difference between them will remain nearly constant, regardless of how far the "threshold" drifted. It is worthwhile to note that reasonable voltage variations and aging do not cause "threshold" drift of the inputs. The triggering level for both Start and Stop inputs is between -350 mV and -450 mV for the 2228A and at 0 volts differentially (-1.2 V nominal for symetrical pulses) for the 2229.

*Move jumper from G4-G4 to G3-G3. See Schematic Sheet 2 of 5.

2.5 Overflow Detection

The 2228A and 2229 have a continuously adjustable Full Scale (from approximately 8 to 11 Bits). This requires detection of Full Scale by some means other than using the next most significant bit as an indicator unless the Full Scale is set to approximately 5% beyond the desired count (e.g., 1024 + 5% = 1075). In addition, the state of the Analog to Time Converter is detected when the clock stops. This information is stored and presented on the R12 line independent of the Full Scale setting. This information is also used to determine LAM and Q response.

2.6 LAM and Q Response

The 2228A/2229 was designed to permit the elimination of readout of empty modules to achieve fast readout rate. A module in which no channel has received a stop pulse (i.e., all scalers overflowed) will produce no Q-response or LAM and appears as an empty CAMAC slot during readout, reducing readout time. An X-response is still generated.

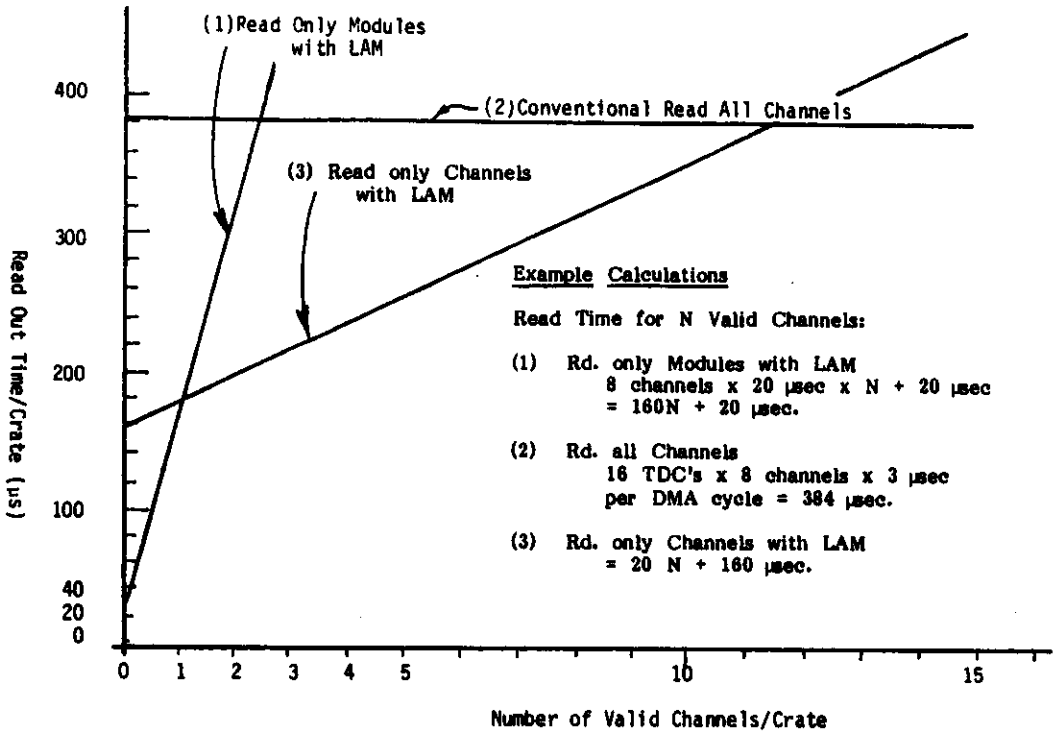
Some branch drivers (interfaces between computers and CAMAC crates) or readout schemes require a Q response or a LAM from any module that occupies a station (N) in the CAMAC crate. For these situations the Q Select Side Panel Switch should be turned to the "End of Conversion" position.

A LAM (Look-At-Me) signal is generated from end of conversion until a Module Clear or Clear LAM (Z, C, F(2) A(7), F(9) or F(10)). LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable F(26) or Disable F(24) function command, and can be tested by Test LAM F(8). LAM is suppressed for empty modules as indicated above.

The test function F(8) allows the LAM to be tested. In response to application of F(8) N A (where A is any A from A(0) to A(7)) independent of Disable LAM, a Q response will be generated if LAM is set and not masked. Although the LAM is disabled while the 2228A/2229 in question is being addressed (i.e., for the duration of N), once latched it will produce a Q response when an F(8) N A is applied. An F(10) will clear the LAM independent of the state of the LAM mask but this will also end Q response and disable readout until after the next conversion (gate). A safer way to eliminate the LAM signal is to use F(24) (Disable LAM) to mask the LAM signal. This will allow normal readout to continue.

Also see the section on 2228A/2229 Read Schemes.

IMPORTANT: The unit should always be initialized with an F(24) (Disable LAM) or an F(26) (Enable LAM) and an F(10) (Clear LAM) whenever the crate power is turned on.



READ OUT TIME vs. VALID CHANNELS/CRATE

Figure 2.1

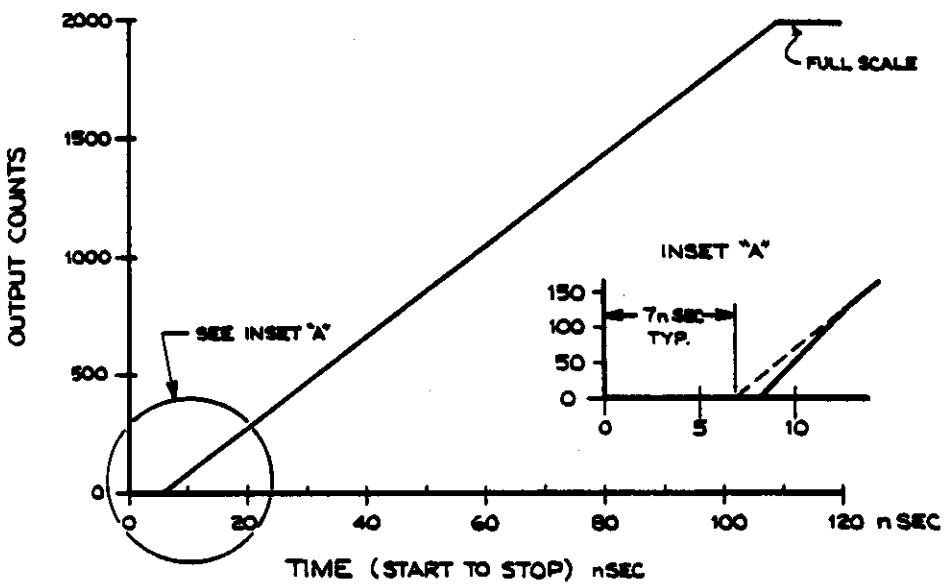


Figure 2.2

SECTION 3

FUNCTIONAL DESCRIPTION

3.1 General

The Model 2228A and 2229 consist of 8 independent identical TDC's and associated circuitry. Referring to the block diagram (Figure 3.1), the TDC circuitry is divided into seven basic sections:

a. A Common Start, Delayed Start and Common Stop circuit for distributing the start signal to the start-stop gates.

b. Eight Stop Input circuits.

c. Eight Time-To-Analog converters.

d. Eight Analog-To-Time converters.

e. Eight scalers.

f. A Gated oscillator

g. A CAMAC control section.

3.2 Start, Delayed Start and Common Stop

The Model 2228A requires NIM-level inputs for the Start and Stop, but uses ECL integrated circuits for gating and latching (see Figure 3.2). This requires a -800 mV shift in logic levels which is provided by using NPN emitter followers on all inputs. Timing stability is accomplished by providing both the start channel and the stop channels with approximately the same number and type of components assembled so that delay changes (caused by temperature and voltage changes) will cancel each other.

A pulse applied to the Common Start input, after receiving a voltage offset and level inversion, will set a latch (Schematic 2/5) formed from two ECL negative NAND gates. The latch output couples to two 3 input gates each driving the center point of 100 Ω strip line busses via 50 Ω coax. Each of the two busses provides four Stop channels with a Start Enable signal which is available until a Common Stop is received, until the delayed Start occurs, or until a clear pulse is received (see next three paragraphs for explanation of three Start-Disable functions).

Once the Start latch is set, it will remain set until a clear pulse resets the entire module. If the common Stop latch is set, or when the delayed Start occurs (either one disabling the Start latch output), they will remain in that condition until the Start latch is cleared. Thus, once one Start pulse is received, the entire section is made immune to any further Start pulses until the entire module is properly cleared. A

CAMAC Inhibit will disable the Start input emitter follower for the duration of the Inhibit.

The Common Stop Latch, when set, will disable the two 3-input gates, ending the Start Enable signal. The Common Stop input passes through the same levelshifting and inverting stages and uses the same type latch as the Start channel. The only differences are that the latch complement level is used to disable the 3 input coax drive gate and the latch is only enabled when the Start latch is set and is, therefore, cleared when the Start latch is cleared.

The delayed Start is a level which occurs approximately 1.2 times the full scale time range setting. It results from a level-sensing amplifier monitoring a capacitor which is being charged via a constant current source, which was unclamped when the Start latch set. Because the current source is controlled by the I-select line, it is always proportional to the current sources in the time-to-analog circuits (see next section).

A common module clear pulse, 1.0 to 1.2 μsec long, is used to clear the Start latch and keep it clamped (therefore disabled) for the duration of the clear.

The internal test capability is provided by generating a Common Start and a Common Stop upon receiving an F(25). These two pulses are generated by two voltage comparators that monitor a ramp generated by I_{SEL}. The delay is thus proportional to the psec/Count Range. The other side of the start comparator is tied to ground and the other side of the Stop comparator is tied to V_{BFS} which tracks the full scale range. The count obtained is thus about 75% of the full scale range for most psec/Count and full scale range settings.

3.3 Stop Input Circuits

The individual Stop circuits operate identically to the Common Stop (see previous section). When a Start enable signal occurs, it enables the linear gate of the Time-To-Analog Converter (TAC) stage via an ECL differential output gate. It also enables the Stop latch to be set which, until the Start enable signal appeared, was held clamped in a reset condition, preventing it from being set by a possible premature pulse at the Stop input.

Once the Stop latch is enabled, it will be set by the next Stop input pulse. (The input pulse uses the same level shifting, inverting, and latching techniques as the Start and Common Stop inputs.) When the Stop latch is set, it disables the ECL gate, thereby disabling the linear gate in the TAC.

3.4 Time-To-Analog Converters

Each Time-To-Analog Converter (TAC) utilizes a constant current generator where the actual value of current is determined by the difference between the voltage on the I-Select bus and the -24 volt bus. This current is gated into an integrating capacitor for the duration of time between common Start and a Stop, therefore, the voltage on the

capacitor is proportional to that time. This capacitor is then discharged by the Analog-To-Time Converter Stage.

As can be seen from sheet 3 of the schematic, the I-Select bus voltage is varied grossly to select ranges by switch selection of voltage levels of a compensated, tracking divider chain. Each range position has a fine control potentiometer which has been factory adjusted to provide the ranges shown on the side panel (and on the schematic). The 250 psec/Count range can be set as high as 500 psec/Count and used reliably.

Temperature drift is increased by up to a factor of 4 by this method. If a more stable method is desired, see section 2.3 (converting the TDC to longer time ranges).

3.5 Analog-To-Time Converter

The Analog-To-Time Converter (ATC) stage is functionally the inverse of the previous TAC stage, except that the capacitor discharge rate is much slower than the charge rate.

The charge which was delivered to the integrating capacitor through the linear gate of the TAC stage is subsequently removed by means of a stable current source (see Figure 3.2). Thus, the voltage across the integrating capacitor is returned to its quiescent level at a constant rate. (This rate is proportional to the difference between the +24 and V_{REF} inputs.) The output amplifier senses the voltage across this capacitor and generates an output level as long as this voltage is more negative than a reference level (which is set by the voltage divider between +3 volts and ground). The output time duration (T_2) is, therefore, proportional to the input time (T_1) of the TAC where time T_2 is approximately 1,000 times T_1 when used in the most sensitive 50 psec/Count range (i.e., $T_2 = 1000\ T_1$).

Stable operation of the QTC is assured by the on-board stabilized V_{REF} (approximately +12 V current source reference) to be independent of external supply variations. Whenever necessary elsewhere in the analog circuits, tracking dividers and temperature-compensating diodes or transistors are used to remove first order drift errors.

3.6 Scaler

The output of each Analog-To-Time Converter in the TDC is used to gate a clock into one half of a LeCroy hybrid SC100 Dual Eleven-Bit Scaler. The oscillator is synchronously started with respect to the leading edge of the Start input pulse (see Section 3.7). This insures no fractional pulses during the beginning of the run-down cycle.

When the conversion cycle is complete, readout of the addressed scaler can be done by enabling the proper SC100 (using decoded A2, A4 subaddress lines) and selecting the proper half of the SC100 (using the A1 subaddress). The 11-Bit data word will be gated out in parallel to the CAMAC dataway when an N, either an F(0) or an F(2) command and the appropriate A are received.

3.7 Gated Oscillator

The clock circuit is a modified Colpitts oscillator employing a highly temperature-stable clock and a mica capacitor as its resonant elements. Its frequency is 20 MHz. The oscillator is gated on at approximately 1.2 times the full scale range setting after the leading edge of the Start pulse. (In the optional long time range units it is gated on with the leading edge of the Start, as the clock noise becomes insignificant.) Synchronously, gating the oscillator on in this way eliminates the uncertainty of one count associated with an asynchronous oscillator and eliminates clock noise caused by not delaying the turn-on. The conversion time is approximately 1 μsec + (.05 μsec times the full scale count setting).

3.8 Full Scale Adjustment

The Model 2228A and 2229 allow for an adjustable full scale from about 8 bits to 11 bits of data. The adjustment is made via a rear panel pot. There is a test point provided at the rear panel to allow monitoring the full scale setting (see the conversion chart Figure 1.1). This feature reduces the conversion time in proportion to the full scale range.

3.9 Overflow Detection

Because the full scale is adjustable it is necessary to detect overflow (no stop within time range) by some means other than using the next bit as an overflow condition. (This method can still be used if desired on all but the 11 bit range by setting the full scale pot to about 5% beyond the desired count.) The method used in the 2228A and 2229 is to sample the state of the clock gate for each channel following the last clock pulse. If there was a valid stop, the gate should be closed. The information acquired is stored in latches and used to determine the Q and Look-At-Me status.

3.10 LAM and Q Response Circuits

As stated previously, the overflow information is used in the Q and LAM decisions. There are three switch selectable options for Q status:

a. All channels have Q=1 if conversion is complete.

b. All channels have Q=1 if conversion is complete and at least one channel has valid date (i.e., did not overflow).

c. Each channel has a Q=1 if at the end of conversion it had not overflowed.

The LAM status has 4 switch selectable options. These are:

a. LAM status = 1 if conversion is complete.

b. LAM status = 1 if conversion is complete and at least one channel has valid data (i.e., did not overflow).

c. LAM status = 1 if conversion is complete and the channel addressed by the "A" lines has not overflowed. (This is not according to CAMAC convention. (See description of the Fast Read Mode in Section 2.1.)

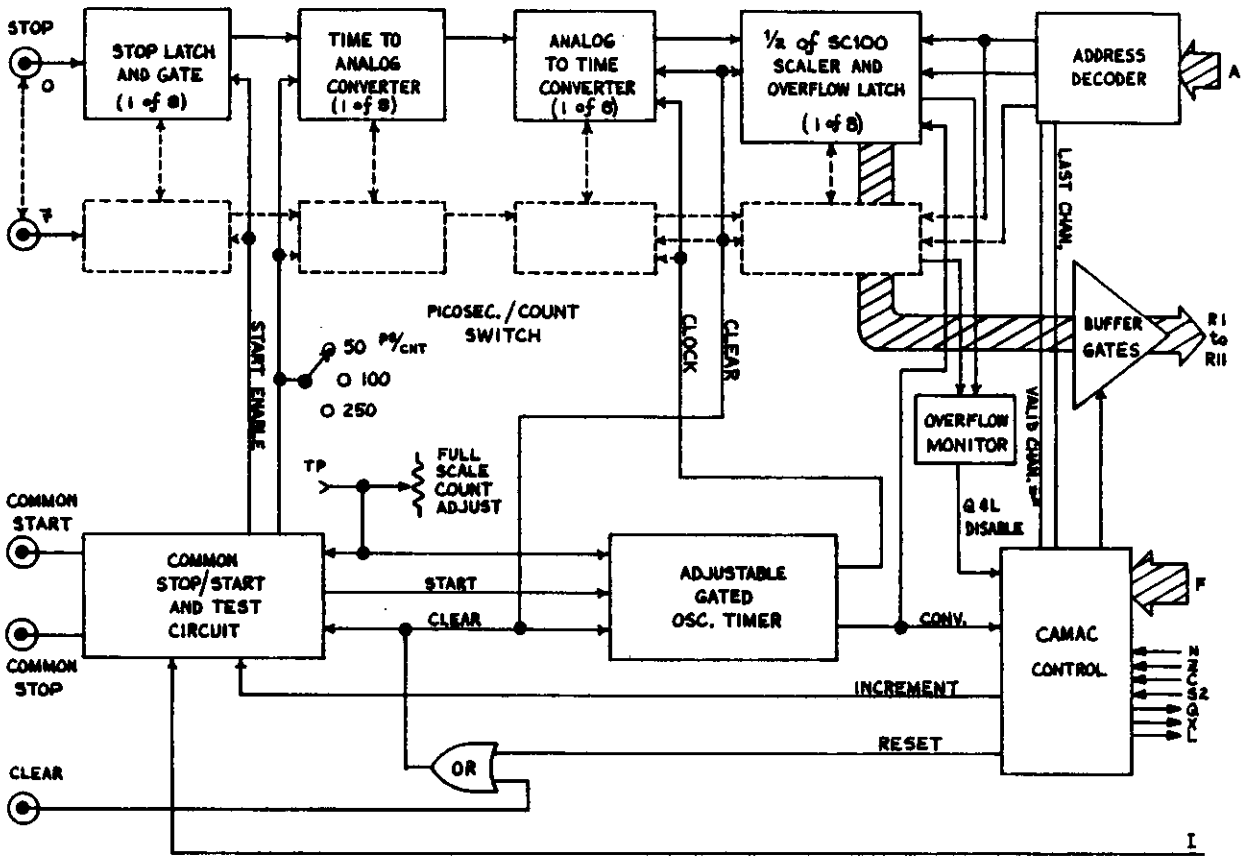
d. LAM = 0 always. This allows the user to turn off the LAM in cases where it is not desired without needing to send an F(24) to the unit each time it is turned on.

3.11 CAMAC Control

The decoding of CAMAC "F" lines F1, F2, F8 and F16 is done in an excess three gray code to decimal converter (7444). The useful outputs are OR'ed together and then AND'ed with $\overline{F4}$ and $\overline{A8}$ (valid channel). This signal is in turn AND'ed with N to produce the "Valid Command" signal that is used as CAMAC X. This signal also provides the read gate to output data onto the dataway and a gate (along with Z and C) for S2.

The CAMAC "A" lines A2 and A4 are decoded and gated with end of conversion and an OR'ed signal of F(0) and F(2) in a BCD to decimal decorder (7442). The output of this decoder provides the enable signal to the four SC100 scalers. The A1 line provides the select line to the scalers (selects which half of the SC100 is gating data out if it is enabled).

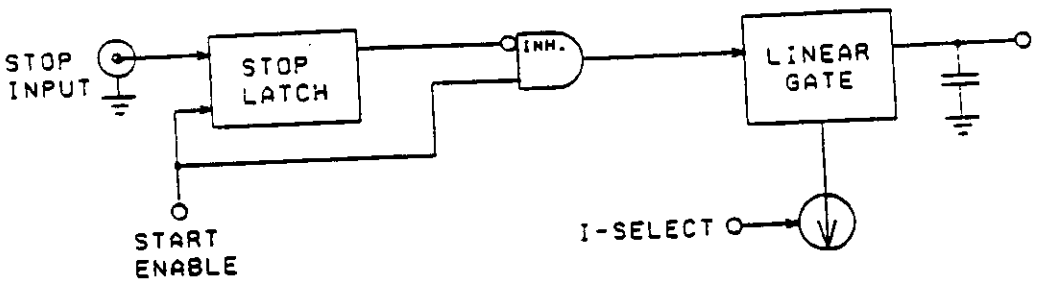
The A1, A2 and A4 lines also go to an 8 line to 1 line data selector (multiplexer) to examine the individual overflow signals. These signals are stored in the two quad latches (74175) and are OR'ed together by a 7430 8 input gate. These latches are clocked by the end of conversion signal (delayed through Q-26).



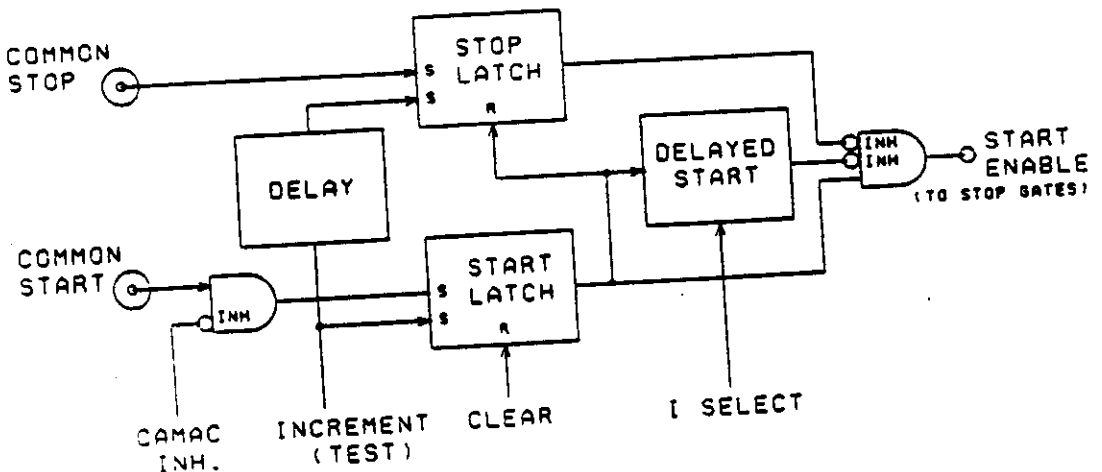
BLOCK DIAGRAM - MODEL 2228A

TIME-TO-DIGITAL CONVERTER

Figure 3.1



BLOCK DIAGRAM - STOP INPUT AND TAC SECTION



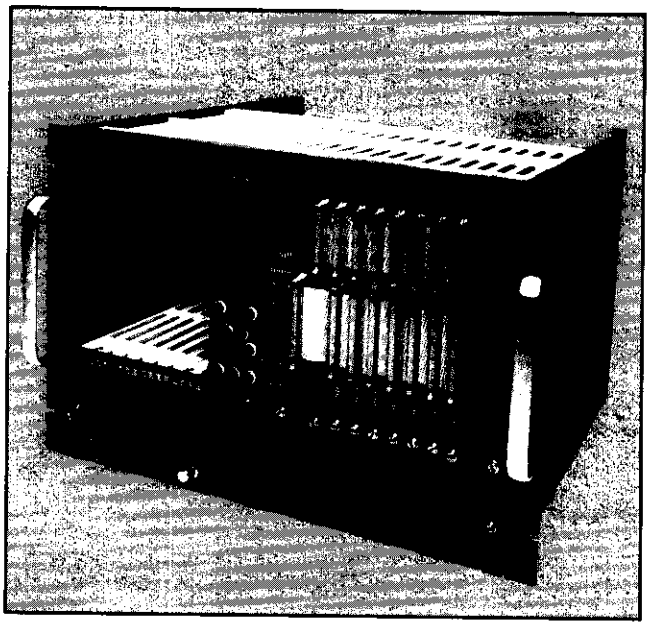
BLOCK DIAGRAM - COMMON START/STOP AND TEST CIRCUITS

Figure 3.2

APPLICATION NOTE

LeCroy

AN-33 INTRODUCTION TO CAMAC



Full power Crate with GPIB interface and waveform digitizer.

CAMAC is a modular data handling system used at almost every Nuclear Physics research laboratory and many industrial sites all over the world. It represents the joint specifications of the US NIM and the European ESONE Committees.

The primary application is data acquisition but CAMAC may also be used for remotely programmable trigger and logic applications (LeCroy ECLine family of programmable logic units). The CAMAC standard covers electrical and physical specifications for the modules, instrument housings or crates, and a crate backplane. Examples of crates include the LeCroy Model 1434A with 25 positions and the Model 8013A with 13 positions.

Individual crates are controlled by slave or intelligent controllers such as the LeCroy Model 4801. The controllers are tied together with a parallel Branch Highway that ends in a Branch Driver. The Branch Driver is interfaced directly to a data acquisition computer. Alternatively, tree or parallel data acquisition architectures may be created by connecting secondary CAMAC branches via an intelligent, programmable CAMAC Branch Driver Module, the Model 4805. This unit would reside in a crate on the primary CAMAC branch. See application note AN-35 for examples.

CAMAC crates may also be connected in a Local Area Fiber Optic Network via the LeCroy Model 5211 Fiber Optic Serial Link and a serial crate controller. Up to 62 crates separated by a maximum of 500 m can exchange data at transmission rates of 45 megabytes/sec.

LeCroy also offers crate controllers that interface directly with the GPIB or IEEE Std 488-1978 Bus. Therefore an entire CAMAC Crate may appear as a single instrument on this very popular laboratory instrument bus. The Model 8901A is a GBIP/CAMAC slave interface that operates as a "Talker/Listener" while the Model 4802 may be programmed to do computations and data compaction.

Timing and protocol specifications permit up to 1 megaword/sec transfers of 16 or 24-bit words for both the DATAWAY and CAMAC Branch. GPIB timing is usually limited by the host computer and typically runs at 500 kilobytes/sec.

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SECTION 1: INTRODUCTION

CAMAC is an international standard of modularized electronics as defined by the ESONE Committee of the JRC, Ispra. Its function is to provide a scheme to allow a wide range of modular instruments to be interfaced to a standardized multi-receptacle which, in turn, may be interfaced to a computer. In this way, additions to a data transfer and control system may be made by plugging in additional modules and making suitable software changes. Thus, CAMAC allows information to be transferred into and out of the instrument modules.

CAMAC modules may be plugged into a CAMAC Crate which has 25 *STATIONS*, numbered 1 through 25. Station 25, the rightmost station, is reserved for a CRATE CONTROLLER, whereas Stations 1 – 24 are *NORMAL STATIONS* used for CAMAC Modules (see figure below). Usually, Station 24 is also used by the controller in that most controllers are double width (#2 CAMAC). The purpose of the controller is to issue CAMAC *COMMANDS* to the modules and transfer information between a computer (or other digital device) and the CAMAC modules.

Data transfer, control functions, and module powering is affected via the *DATAWAY.* This is a series of bus and individual lines across the back of the crate. The DATAWAY lines include digital data transfer lines, strobe signal lines, and addressing lines and control lines. See Table 3 for a pin allocation chart.

In a typical DATAWAY operation, the crate controller issues a CAMAC *COMMAND* which includes specifying a station number (N), a subaddress (A), and function code (F) (see Table 1). In response, the subaddress of the module will generate valid command accepted (X response) and act on the command. If this command requires data transfer, the read (R) or write (W) lines will be used. Note that the terms Read and Write apply to the controller, not the module. For example, under a Read command, the controller reads data contained within a module.

SECTION 2: USE OF THE DATAWAY LINES

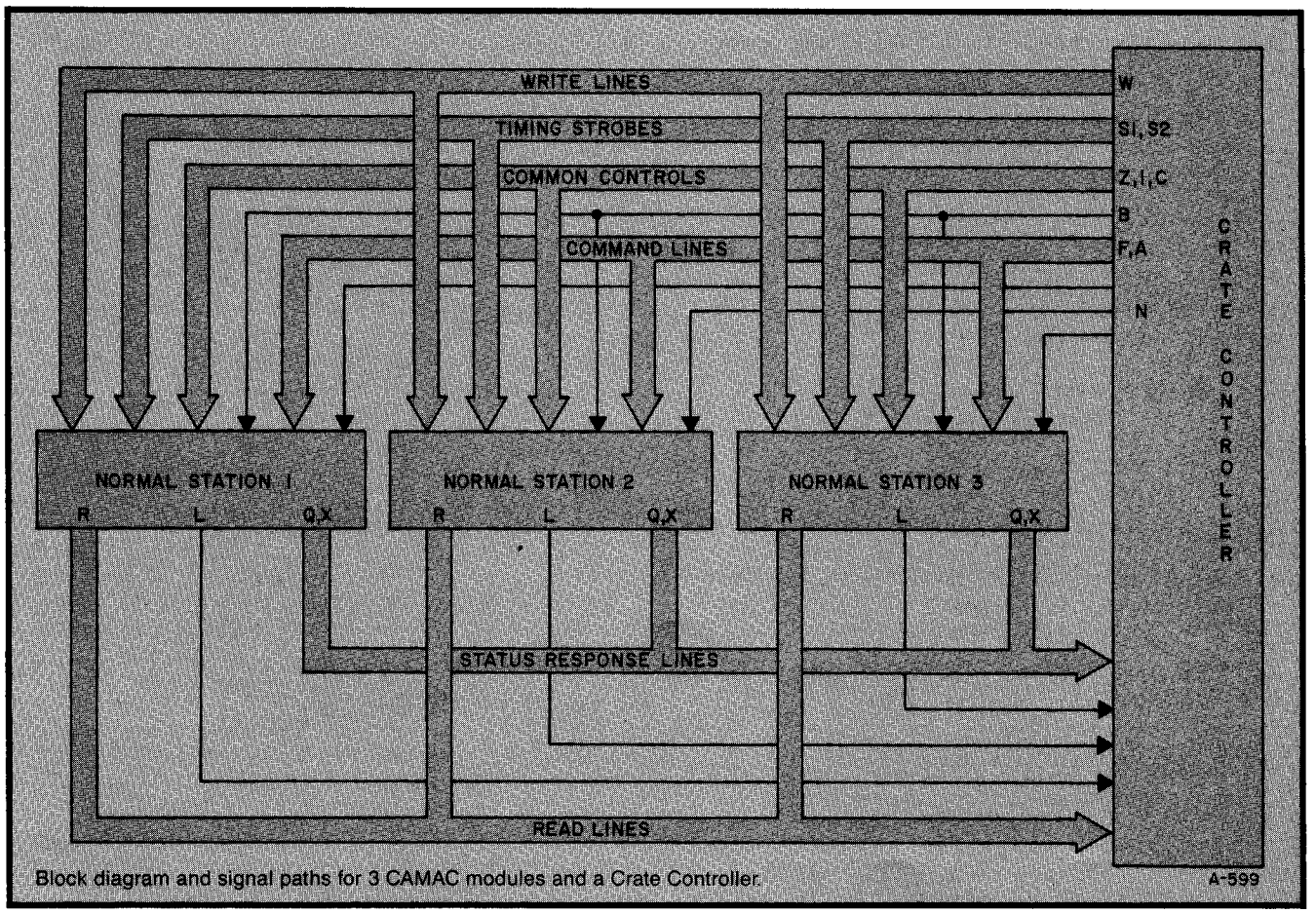
Communication with plug-in units takes place through the DATAWAY. This passive multi-wire highway is incorporated in the crate and links the 86-pin sockets to all stations. The bus lines link corresponding pins at all normal stations and, in some cases, the control station. Individual lines link one pin at a normal station to one pin at the control station. The patch pins have no specified DATAWAY wiring but can be connected to individual points to which patch leads may be attached.

During a DATAWAY operation the controller generates a command consisting of signals on individual Station Number lines to specify one or more modules, signals on the Subaddress bus lines to specify a sub-section of the module or modules, and signals on the Function bus lines to specify the operation to be performed. The command signals are accompanied by a signal on the Busy bus line, which is available at all stations to indicate that a DATAWAY operation is in progress.

When a module recognizes a Read command calling for a data transfer to the controller, it establishes data signals on the Read bus lines. When a controller recognizes a Write command calling for a data transfer to a module, it establishes data signals on the Write bus lines. In addition, regardless of whether there is transfer on the R or W lines, the module may transmit one bit of status information on the Response bus line.

Two timing signals, Strobes S1 and S2, are then generated in sequence on separate bus lines. The strobes are used to transfer data from the DATAWAY into modules (on Write commands) and into the controller (on Read commands). They may also initiate other actions within the controller and modules.

Whenever there is no DATAWAY operation in progress (indicated by the absence of the Busy signal) any module may generate a signal on its individual Look-at-Me line to indicate that it requires attention. Three common control signals are available



Block diagram and signal paths for 3 CAMAC modules and a Crate Controller.

A-599

at all stations, without requiring addressing by a command, in order to initialize all units (typically after switch-on), to Clear data registers, and to inhibit features such as data-taking.

2.1 DEFINITION OF COMMANDS

A command consists of signals on the DATAWAY lines which specify at least one module (by individual station number lines), a subsection of the module or modules (by the four subaddress bus lines), and the function to be performed (by the five function bus lines). The command signals are maintained for the full duration of the operation on the DATAWAY. They are accompanied by a signal on the Busy bus line which indicates to all units that a DATAWAY operation is in progress.

Station Number (N)

Each normal station is addressed by a signal on an individual station number line (N) which comes from a separate pin at the control station. The stations are numbered in decimal code from the lefthand end as viewed from the front, beginning with Station 1.

Subaddress (A8, A4, A2, A1)

Different sections of a module are addressed by signals on the four A bus lines. These signals are decoded in the module to select one of up to sixteen subaddresses, numbered in decimal from 0 to 15.

Function (F16, F4, F2, F1)

The function to be performed at the specified subaddress in the selected module or modules is defined by the signals on the five F bus lines. These signals are decoded in the module to select one of up to 32 functions, numbered in decimal from 0 to 31. The definitions of the 32 function codes are summarized in the DATAWAY Command Operations section.

Strobe Signals (S1 and S2)

Two strobe signals S1 and S2 are generated in sequence on separate bus lines. These signals are used to transfer information between plug-in units via the DATAWAY or to initiate operations within units. In either case the specific action is determined by the command present on the DATAWAY. Both strobes are generated during each DATAWAY command operation, and all plug-in units which accept information from the DATAWAY do so in response to these strobes. The first strobe S1 is used for actions which do not change the state of signals on the DATAWAY lines. All units which accept data from the DATAWAY in a Read operation, or in a Write operation do so in response to S1. The second strobe S2 is used to initiate any actions which may change the state of DATAWAY signals, for example, clearing a register whose output is connected to the DATAWAY.

2.2 DATA

A common parallel highway is used for all transfers. All information carried by the parallel highway is conveniently described as data, although it may be information concerned with status or control features in modules. Up to 24 bits may be transferred in parallel between the controller and the selected module. Independent lines (Read and Write) are provided for the two directions of transfer.

The Write Lines (W1-W24)

The controller or other common data source generates data signals on the W bus lines at the beginning of any "Write" operation. The W signals reach a steady state before S1, and are maintained until the end of the operation, unless modified by S2.

The Read Lines (R1-R24)

Data signals are set up on the R bus lines by the module as soon as a "Read" command is recognized. The R signals reach a steady state before S1, and are maintained for the full duration of the DATAWAY operation, unless the state of the data source is changed by S2. The controller or other common data receiver strobes the data from the R bus lines at the time of the Strobe S1.

2.3 STATUS INFORMATION

Status information is conveyed by signals on the Look-at-Me (L), Busy (B), and Response (Q) lines.

Look-at-Me (L)

This, like the N line, is an individual connection from each station to a separate pin at the control station. When there is no DATAWAY operation in progress (no B present) any plug-in unit may generate a signal on its L line to indicate that it requires attention. When B is present each L signal is gated off the DATAWAY line by the unit which generates it.

A Look-at-Me request can be reset by Clear Look-at-Me, initialize, or by the performance of the specific action which generated the request.

DATAWAY Busy (B)

The Busy signal is used to interlock various aspects of a system which can compete for the use of the DATAWAY. Specifically, it is generated during DATAWAY command or common control operations. Whenever N is present, B is present, and for the duration of B, all L signals are gated off the DATAWAY lines.

Response (Q)

The Q bus line is used during a DATAWAY operation to transmit a signal indicating the status of a selected feature of the module.

On all Read and Write commands the signal on the Q bus line remains static from the time the command is received until S2. For all other commands the signal on the Q bus line may change at any time.

2.4 COMMON CONTROLS

Common control signals operate on all modules connected to them without the need to be addressed separately by a command. In order to provide protection against spurious signals, the initialize (Z) and Clear (C) signals must be accompanied by Strobe S2.

Initialize (Z)

The initialize signal has absolute priority over all other signals or controls. It sets all units to a basic state by resetting all registers, whether data or control, to a defined state, and by resetting all L signals and disabling them where possible. Units which generate Z must also cause S2 and B to be generated. Modules which accept Z gate it with S2 as a protection against spurious signals on the Z line.

Inhibit (I)

The presence of this signal inhibits any activity (for example, data taking). It must either not change when B is present or have rise and fall times not less than 200 nsec.

Clear (C)

This command signal clears all registers or bistables connected to it. Units which generate C must also cause S2 and B to be generated. Modules which accept C gate it with S2 as a protection against spurious signals on the C line.

2.5 PRIVATE WIRING

Patch Leads (P1-P7)

Five pins (P1 to P5) on the 86-way socket at normal stations

are not prewired to DATAWAY lines but are freely available for local connections. At the control station, seven pins (P1-P7) are available. Signals on the patch pins must either remain static when B is present or have rise and fall times not less than 20 nsec.

2.6 DATAWAY COMMAND OPERATIONS

A Command is composed of signals on the Station Number line or lines, the Subaddress lines and the Function lines. It is accompanied by a signal on the Busy Line. In response to a command, data may be transferred on the Read or Write lines and one bit of status information on the Q line. The two Strobes S1 and S2 must be generated in each DATAWAY command operation to control its timing.

The order in which the commands are described below corresponds to the function codes set out in Table 1. In this table the term "register" is used for an addressable data source or receiver, without implying that it has a data storage property. The function codes allow the registers in a module to be divided into two distinct sets, known as Group 1 and Group 2. Thus it is possible to operate on more than the basic set of 16 registers selected by the four subaddress lines.

A common feature of all commands is that if the module has a Look-at-Me source which requests a specific command, then the performance of that command should reset the Look-at-Me source.

Read Commands (Function Codes 0-7)

Read commands are identified by the combination F16 = 0, F8 = 0 in the function code. They specify that information is to be transferred from a module to a controller via the R bus lines. Data signals are set up on the R bus lines by the module as soon as the "Read" command is recognized, and the appropriate status signal connected to the Q bus line. The R and Q signals reach a steady state before S1, and are maintained for the full duration of the DATAWAY command operation unless the state of the signal source is changed at S2. The controller or other common data receiver strobes the data from the R and Q bus lines at the time of the Strobe S1.

In order to facilitate reading by sequential addressing, all registers containing data (as opposed to control information) must have consecutive subaddresses starting at subaddress 0. At each of these subaddresses the module generates Q = 1 in response to the appropriate Read command. At the next subaddress in sequence (where there is not a data register) the response is Q = 0. At all remaining addresses the Q signal may be used to test any feature, subject to the general requirement that the Q signal must be static from the beginning of command until at least S2.

CODE 0, READ GROUP 1 REGISTER

This command selects, by subaddress, one register from the first group in the module and transfers the contents of this register to the controller. The contents of the register remain unchanged.

CODE 1, READ GROUP 2 REGISTER

Same as Code 0, except command selects register from the second group.

CODE 2, READ AND CLEAR GROUP 1 REGISTER

Same as Code 0, except the module register is cleared at time S2.

CODE 3, READ COMPLEMENT OF GROUP 1 REGISTER

Same as Code 0, except command transfers the complement of the contents of this register to the controller.

CODE 4-7

Unassigned at this time.

2.7 CONTROL COMMANDS (FUNCTION CODES 8-15)

Control commands are identified generally by F8 = 1 in the function code. They are divided into two groups by the state of F16, in this case F16 = 0. They specify that information is not transferred on either the R or W bus lines. However, information may be conveyed on the Q bus line in any of these commands. The signal on the Q bus line may change at any time but is strobed into the controller at time S1 and may (except in Code 8) be reset by Strobe 2.

CODE 8, TEST LOOK-AT-ME

This command selects a Look-at-Me source in the module and presents the state of this source on the Q bus line.

CODE 9, CLEAR GROUP 1 REGISTER

This command selects, by subaddress, a register from the first group in the module and clears the contents of this register.

CODE 10, CLEAR LOOK-AT-ME

Same as Code 8, except the Look-at-Me source is cleared at time S2.

CODE 11, CLEAR GROUP 2 REGISTER

Same as Code 9, except command selects register from the second group.

CODE 12-15

Unassigned at this time.

2.8 WRITE COMMANDS (FUNCTION CODES 16-23)

Write commands are identified by the combination F16 = 1, F8 = 0 in the function code. They specify that information is to be transferred from a controller to a module via the W bus line. The controller or other common data source generates data signals on the W bus lines at the beginning of the "Write" operation. The module connects the appropriate status signal to the Q bus line as soon as the command is recognized. The W and Q signals reach a steady state before S1 and are maintained for the full duration of the DATAWAY command operation unless the status of the signal source is changed at Strobe 2. In order to facilitate writing into registers by sequential addressing, all registers which are to contain data (as opposed to control information) have consecutive subaddress starting at subaddress 0. At each of these subaddresses, the module generates Q = 1 in response to the appropriate Write function. At the next subaddress in sequence (where there is not a data register), the response is Q = 0. At all remaining subaddresses the Q signal may be used to test any feature subject to the general requirement that the Q signal must be static from the beginning of the command until at least S2.

CODE 16, OVERWRITE GROUP 1 REGISTER

This command selects, by subaddress, one register in the first group in the module and sets the contents of this register to correspond with the data generated on the W bus lines by the controller.

CODE 17, OVERWRITE GROUP 2 REGISTER

Same as Code 16, except command selects a register in the second group.

CODE 18, SELECTIVE OVERWRITE GROUP 1 REGISTER

Same as Code 16, except a separate "mask" register defines which bits in the selected register are set.

CODE 19, SELECTIVE OVERWRITE GROUP 2 REGISTER

Same as Code 18, except command selects a register in the second group.

CODE 20 – 23

Unassigned at this time.

2.9 CONTROL COMMANDS (FUNCTION CODES 24-31)

Control commands are identified generally by F8 = 1 in the

function code. They are divided into two groups by the state of F16, in this case F16 = 1. They specify that information is not transferred on either the R or W bus lines. However, information may be conveyed by the Q bus line in any of these commands. The signal on the Q bus line is permitted to change at any time but is strobed into the controller at time S1 and may (except in Code 27) be reset by Strobe S2. Precautions must be taken to ensure that information is not lost due to Q signals appearing between S1 and S2.

CODE 24, DISABLE

This command selects, by subaddress, and disables a feature of the module; e.g., a Look-at-Me source or a data input.

CODE 25, INCREMENT PRESELECTED REGISTERS

This command adds one simultaneously to the contents of each register in one of 16 groups, defined by the subaddress.

CODE 26, ENABLE

This command enables the feature of the module selected by the subaddress, e.g., a Look-at-Me source or a data input.

CODE 27, TEST STATUS

This command selects, by subaddress, any feature of a module other than a source of a Look-at-Me request, and tests it by producing a response on the Q bus line.

CODE 28 – 31

Unassigned at this time.

CAMAC Reference Data

CAMAC FUNCTION CODES

CODE F( )	FUNCTION	FUNCTION SIGNALS F16	F8	F4	F2	F1	CODE F( )
0	Read Group 1 Register	0	0	0	0	0	0
1	Read Group 2 Register	0	0	0	0	1	1
2	Read and Clear Group 1 Register	0	0	0	1	0	2
3	Read Complement of Group 1 Register	0	0	0	1	1	3
4	Non-standard	0	0	1	0	0	4
5	Reserved	0	0	1	0	1	5
6	Non-standard	0	0	1	1	0	6
7	Reserved	0	0	1	1	1	7
8	Test Look-at-Me	0	1	0	0	0	8
9	Clear Group 1 Register	0	1	0	0	1	9
10	Clear Look-at-Me	0	1	0	1	0	10
11	Clear Group 2 Register	0	1	0	1	1	11
12	Non-standard	0	1	1	0	0	12
13	Reserved	0	1	1	0	1	13
14	Non-standard	0	1	1	1	0	14
15	Reserved	0	1	1	1	1	15
16	Overwrite Group 1 Register	1	0	0	0	0	16
17	Overwrite Group 2 Register	1	0	0	0	1	17
18	Selective Set Group 1 Register	1	0	0	1	0	18
19	Selective Set Group 1 Register	1	0	0	1	1	19
20	Non-standard	1	0	1	0	0	20
21	Selective Clear Group 1 Register	1	0	1	0	1	21
22	Non-standard	1	0	1	1	0	22
23	Selective Clear Group 2 Register	1	0	1	1	1	23
24	Disable	1	1	0	0	0	24
25	Execute	1	1	0	0	1	25
26	Enable	1	1	0	1	0	26
27	Test Status	1	1	0	1	1	27
28	Non-standard	1	1	1	0	0	28
29	Reserved	1	1	1	0	1	29
30	Non-standard	1	1	1	1	0	30
31	Reserved	1	1	1	1	1	31

TABLE 1

2.10 DIGITAL SIGNAL STANDARDS ON THE DATAWAY

The potentials for the binary digital signals on the DATAWAY lines have been defined to correspond with those for compatible current sinking logic devices (e.g., the TTL and DTL series). The signal convention has, however, been inverted to be negative logic. The high state (more positive potential) corresponds to logic '0' and the low state (near ground potential) corresponds to logic '1'. Intrinsic OR outputs are thus available from the manufacturers' standard product range, and disconnected inputs go to the '0' state.

It is an essential feature of the DATAWAY that many units may have their signal outputs connected to the Read and Response lines. Outputs onto these lines therefore require intrinsic OR gates. The same principle is extended to other lines (Command, Write, etc.) in order to allow more than one control-line unit in a crate. The Inhibit line may be an exception, since its signals are shaped with a slow rise and fall if they change during DATAWAY operations.

VOLTAGE STANDARDS FOR DATAWAY SIGNALS

All DATAWAY Signals must conform to the voltage levels as follows:

Pull-up current sources for all DATAWAY bus lines are located in the crate controller (occupying the control station and at least one other station) so as to insure that there is one and only one current source per line. The minimum pull-up current when the DATAWAY line is at + 3.5 V is defined as 2.5 mA. If the controller generates DATAWAY signals at time intervals near the permitted minima, the pull-up current sources should preferably provide not less than 6 mA when the lines are at this potential. The pull-up for the N signals is located in the unit generating the signals, and for the L signals in the unit receiving the signals, so that the individual lines may be joined or grouped within these units if desired.

The N and L lines are effectively individual lines joining two units (a module and a controller). The Q and R lines generally will have many units generating the signals (say 20) with a few units (maximum four) receiving the signals. The remaining lines (W, A, F, S, B, Z, I, C) will have relatively few units generating each signal (often only one) with the possibility of many units receiving the signals.

TIMING OF DATAWAY SIGNALS

The sequence of events during a single DATAWAY operation is shown in the Timing Diagram on the following page. The shaded areas indicate the permitted variation of each signal between an ideal square signal and a signal whose transition across the appropriate signal threshold (0.8 V or 2.0 V) satisfies the conditions shown. The signal waveforms for the command and data lines apply to those lines, if any, which take up the '1' state. Other command and data lines may, of course, be in the '0' state during the operation.

The signals on the Busy line and the various signals constituting the command need not occur in exact synchronism, provided their envelope lies within the shaded areas of the diagram. Similar variation is permitted between the signals constituting the data. The broken line indicates the earliest time at which the data signals may change in response to S2.

Key points on these waveforms are indicated by t_0 - t_9, with the following significance:

Points t_0, t_3, t_6 represent the initiation of the negative-going of the Command, Strobe 1, and Strobe 2 signals, respectively. They are the times at which the signals would be received from an ideal DATAWAY with no capacitative loading.

Points t_9, t_5, t_8 represent similarly the initiation of the positive-going edges of the same signals.

Points t_2, t_{11} are the latest time at which the data source is permitted to initiate the negative-going and positive-going edges of the data signals.

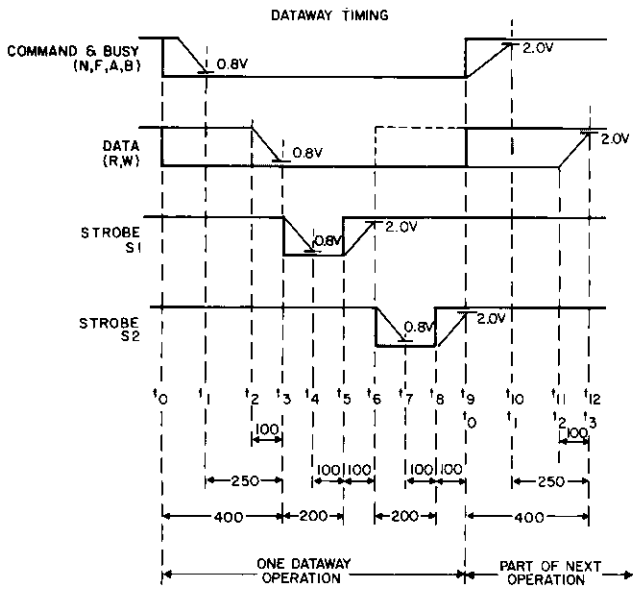
Points t_1, t_3, t_4, t_7 represent the latest times at which the received signals are permitted to reach a maintained '1' state, and therefore refer to the last negative-going transition across the + 0.8 V threshold.

Points t_6, t_9, t_{10}, t_{12} represent the latest times at which the received signals are permitted to reach a maintained '0' state, and therefore refer to the last positive-going transition across the + 2.0 V threshold.

Controllers must initiate the negative- and positive-going edges of the command and strobe signals at intervals not less than those defined by t_3, t_5, t_6, t_8, and t_9. Modules respond to the command within the most adverse value of (t_1 - t_2); i.e., 100 nsec. The electrical characteristics of the DATAWAY and connections from it into units must allow signals to rise and fall within the minimum times for (t_0 - t_1), (t_2 - t_3) etc.

The next DATAWAY operation must not start before t_9.

The extreme case is shown in the Timing Diagram below with the next operation starting at t_9; t_9 - t_{12} of one operation coincides with t_0 - t_3 of the next. The command and data signals of one operation may thus be removed while those of the next operation are being established. The Busy signal may be maintained continuously during a sequence of consecutive DATAWAY operations. Under suitable conditions any command or data signals of one operation may thus be removed while those of the next operation are being established. The Busy signal may be maintained continuously during a sequence of consecutive DATAWAY operations. Under suitable conditions any command or data signals which have the same state during successive operations may also be maintained. In the extreme case of successive operations with the same command and data, there could be a complete absence of signal transitions between t_0 and t_3.



Times given are maximum values in nsec timing of a Dataway operation.

SECTION 3: POWER SUPPLIES

The voltage tolerances and current loadings are specified in Table 2. The specified tolerances in voltage refer to the voltage measured at the contacts of the DATAWAY sockets and must be maintained under the worst combination of factors such as AC mains voltage and frequency, the maximum current loadings, temperature and the position in the crate of the socket under observation.

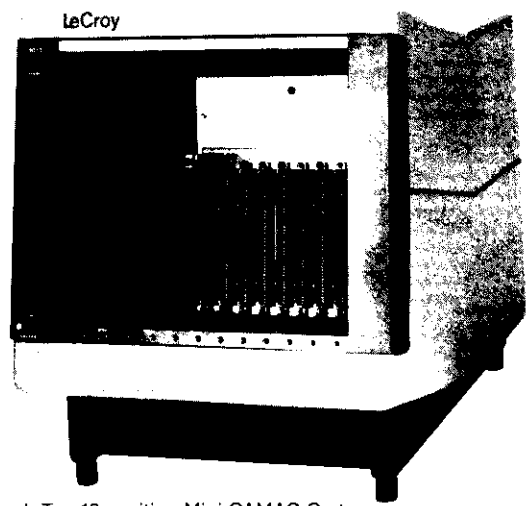
Note that the maximum currents stated in Table 2 below are subject to the overall restrictions as follows:

1. The current carried by any contact of the DATAWAY socket must not exceed 3 A.
2. The total power dissipated in a crate, without forced ventilation, must not exceed 200 W.
3. The power dissipation per single-width station should not, therefore, normally exceed 8 W. Under special circumstances, however, this rating may be increased to a maximum of 25 W, provided suitable precautions are taken to comply with total power dissipation and current loadings.

MAXIMUM CURRENT LOADS

SUPPLY VOLTAGE	VOLTAGE TOLERANCE	IN THE PLUG-IN (PER UNIT WIDTH) *See Notes 1 and 3 above.	IN THE CRATE *See Note 2 above
MANDATORY			
+24 V DC	±0.5%	1 A	6 A
+6 V DC	±2.5%	2 A	25 A
−6 V DC	±2.5%	2 A	25 A
−24 V DC	±0.5%	1 A	6 A
Additional (as required)			
+12 V DC	±0.5%		
+12 V DC			

Table 2



Bench Top 13 position Mini CAMAC Crate.

PIN ALLOCATION AT CONTROL STATION

(STATION 25)

Individual patch contact		P1	B	Busy	Bus line
Individual patch contact		P2	F16	Function	Bus line
Individual patch contact		P3	F8	Function	Bus line
Individual patch contact		P4	F4	Function	Bus line
Individual patch contact		P5	F2	Function	Bus line
Bus line	Command Accepted	X	F1	Function	Bus line
Bus line	Inhibit	I	A8	Subaddress	Bus line
Bus line	Clear	C	A4	Subaddress	Bus line
Individual patch contact		P6	A2	Subaddress	Bus line
Individual patch contact		P7	A1	Subaddress	Bus line
Bus line	Strobe 1	S1	Z	Initialize	Bus line
Bus line	Strobe 2	S2	Q	Response	Bus line
		L24	N24		
		L23	N23		
		L22	N22		
		L21	N21		
		L20	N20		
		L19	N19		
		L18	N18		
		L17	N17		
		L16	N16		
		L15	N15		
		L14	N14		
		L13	N13		
24 Individual Look-at-Me Lines		L12	N12	24 Individual Station	
L1 from Station 1, etc.		L11	N11	Number lines	
		L10	N10	N1 to Station 1, etc.	
		L9	N9		
		L8	N8		
		L7	N7		
		L6	N6		
		L5	N5		
		L4	N4		
		L3	N3		
		L2	N2		
		L1	N1		
	−12 V DC	−12	−24	−24 V DC	
		NC	−6	−6 V DC	
		NC	NC		
Power	Auxiliary −6 V supply	Y1	E	Clean Earth	Power
Bus lines	−12 V DC	+12	+24	+24 V DC	Bus lines
	Auxiliary +6 V supply	Y2	+6	+6 V DC	
	0 V (Power Return)	0	0	0 V (Power Return)	

TABLE 3a

PIN ALLOCATION AT NORMAL STATION

(STATIONS 1-24)

Bus line	Free Bus line	P1	B	Busy	Bus line
Bus line	Free Bus line	P2	F16	Function	Bus line
Individual patch contact		P3	F8	Function	Bus line
Individual patch contact		P4	F4	Function	Bus line
Individual patch contact		P5	F2	Function	Bus line
Bus line	Command Accepted	X	F1	Function	Bus line
Bus line	Inhibit	I	A8	Subaddress	Bus line
Bus line	Clear	C	A4	Subaddress	Bus line
Individual line	Station Number	N	A2	Subaddress	Bus line
Individual line	Look-At-Me	L	A1	Subaddress	Bus line
Bus line	Strobe 1	S1	Z	Initialize	Bus line
Bus line	Strobe 2	S2	Q	Response	Bus line
		W24	W23		
		W22	W21		
		W20	W19		
		W18	W17		
24 Write Bus Lines		W16	W15		
W1=LSB		W14	W13		
W24=MSB		W12	W11		
		W10	W9		
		W8	W7		
		W6	W5		
		W4	W3		
		W2	W1		
		R24	R23		
		R22	R21		
		R20	R19		
		R18	R17		
24 Read Bus Lines		R16	R15		
R1=LSB		R14	R13		
R24=MSB		R12	R11		
		R10	R9		
		R8	R7		
		R6	R5		
		R4	R3		
		R2	R1		
	−12 V DC	−12	−24	−24 V DC	
		NC	−6	−6 V DC	
		NC	NC		
Power	Auxiliary −6 V supply	Y1	E	Clean Earth	Power
Bus lines	−12 V DC	+12	+24	+24 V DC	Bus lines
	Auxiliary +6 V supply	Y2	+6	+6 V DC	
	0 V (Power Return)	0	0	0 V (Power Return)	

TABLE 3b

STANDARD DATAWAY USAGE

TITLE	DESIGNATION	CONTACTS	USE AT A MODULE
Command			
Station Number	N	1	Selects the module (Individual line from control station).
Sub-Address	A1, 2, 4, 8	4	Selects a section of the module.
Function	F1, 2, 4, 8, 16	5	Defines the function to be performed in the module.
Timing			
Strobe 1	S1	1	Controls first phase of operation. (Dataway signals may change).
Strobe 2	S2	1	Controls second phase (Dataway signals may change).
Data			
Write	W1-W24	24	Bring information to the module.
Read	R1-R24	24	Take information from the module.
Status			
Look-at-Me	L	1	Indicates request for service (Individual line to control station).
Busy	B	1	Indicates that a Dataway operation is in progress.
Response	Q	1	Indicates status of feature selected by command.
Command Accepted	X	1	Indicates that module is able to perform action required by the command.

TITLE	DESIGNATION	CONTACTS	USE AT A MODULE
Common Controls			Operate on all stations connected to them, no command required.
Initialize	Z	1	Sets module to a defined state. (accompanied by S2 and B).
Inhibit	I	1	Disables features for duration of signal.
Clear	C	1	Clears registers. (accompanied by S2 and B).
Non-Standard Connections			
Free bus-lines	P1, P2	2	For specified uses.
Patch contacts	P3-P5	3	For unspecified interconnections. No Dataway lines.
Mandatory Power Lines			
+24 V DC	+24	1	
+6 V DC	+6	1	
−6 V DC	−6	1	
−24 V DC	−24	1	
0 V	0	2	Power return
Additional Power Lines			Lines are reserved for the
+12 V DC	+12	1	following power supplies
−12 V DC	−12	1	Low current for indicators, etc.
Clean Earth	E	1	Reference for circuits requiring clean earth.
Reserved Y1, Y2	2		Reserved for future allocation.

TABLE 4

LeCroy

Innovators in Instrumentation

Corporate Headquarters
700 South Main Street
Spring Valley, NY 10977, USA
Tel: (914) 425-2000, TWX: 710-577-2832

West Germany: LeCroy GmbH (06221) 49162
France: LeCroy SARL 69.07.38.97
United Kingdom: LeCroy LTD (0865) 727275
Italy: LeCroy S.r.l. (06) 32.00.646
Switzerland: LeCroy SA (022) 82 33 55

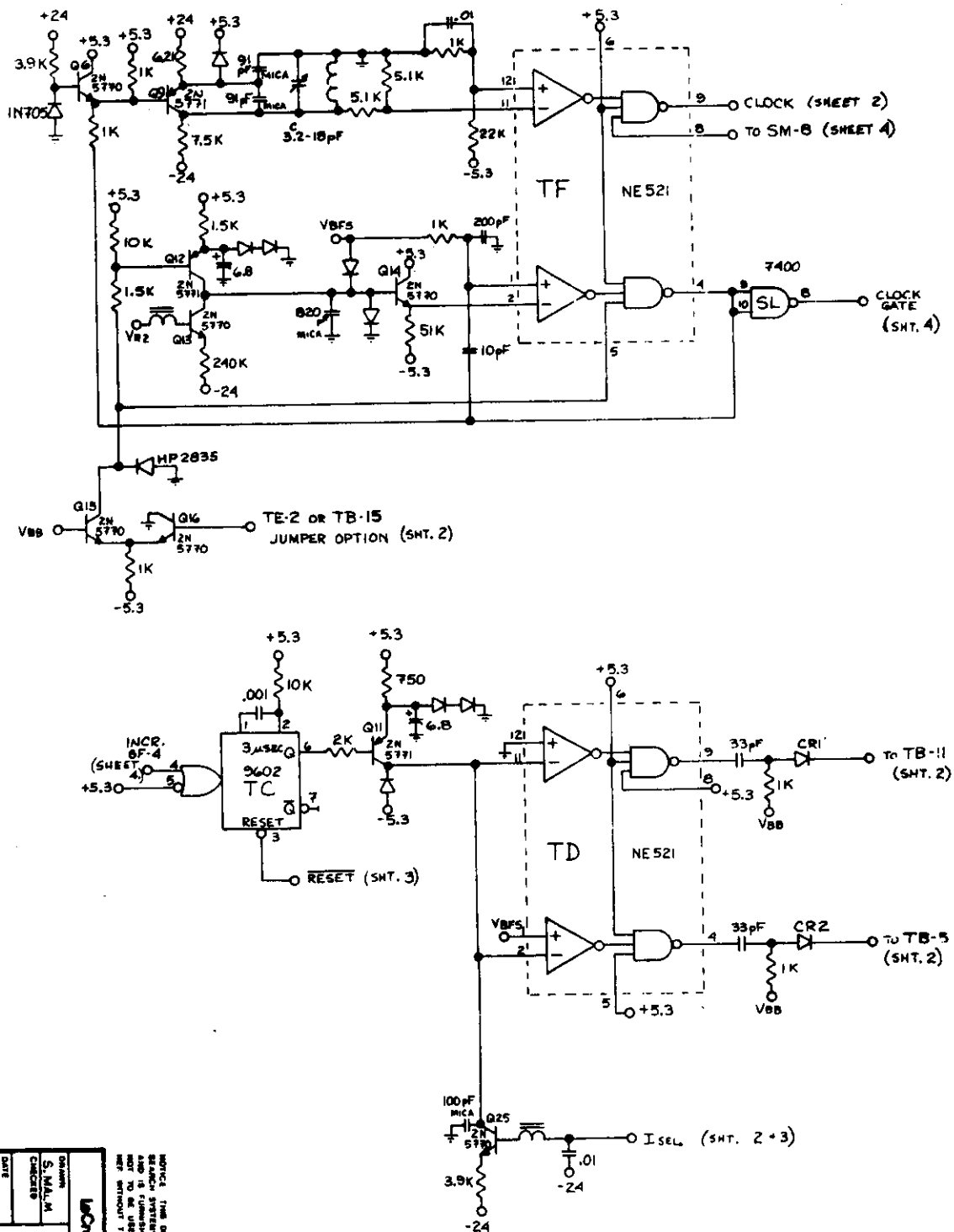
Japan: Toyo 03-279-0771
Benelux: Datalog 31-4904-15856
Australia: ETP Oxford Pty. Ltd. (02) 858-5122
Sweden: Alnor Instrument AB 0155-68050
Other sales and service representatives throughout the world.

PART NUMBER	DESCRIPTION	QUANTITY PER
102245103	CAP CERA DISC 25V .01 UF	52
102444101	CAP CERA DISC 100V 100 PF	3
102444330	CAP CERA DISC 100V 33 PF	18
102444750	CAP CERA DISC 100V 75 PF	1
102745102	CAP CERA DISC 500 .001 UF	1
102745201	CAP CERA DISC 500V 200 PF	1
102944100	CAP CERA DISC 1KV 10 PF	9
103626102	CAP CERA MONO 100 .001 UF	8
116000910	CAP DIP MICA SPECL 91 PF	2
116515101	CAP DIP MICA DM10 100 PF	1
116515151	CAP DIP MICA DM10 150 PF	8
116515241	CAP DIP MICA DM10 240 PF	1
116515560	CAP DIP MICA DM10 56 PF	1
116515680	CAP DIP MICA DM10 68 PF	1
116525821	CAP DIP MICA DM15 820 PF	1
142824685	CAP TANT DIP CASE 6.8 UF	28
158819001	CAP VARI CERA 3.5 - 18 PF	1
161030000	RES COMP ZERO OHMS	55
161225102	RES CARBON FILM 1 K	8
161225121	RES CARBON FILM 120 OHMS	3
161225220	RES CARBON FILM 22 OHMS	3
161225222	RES CARBON FILM 2.2 K	12
161225391	RES CARBON FILM 390 OHMS	5
161225751	RES CARBON FILM 750 OHMS	1
161335101	RES CARBON FILM 100 OHMS	18
161335102	RES CARBON FILM 1 K	31
161335103	RES CARBON FILM 10 K	4
161335121	RES CARBON FILM 120 OHMS	4
161335122	RES CARBON FILM 1.2 K	1
161335152	RES CARBON FILM 1.5 K	2
161335153	RES CARBON FILM 15 K	1
161335182	RES COMP 1/4W 5% 1.8 K	8
161335202	RES CARBON FILM 2 K	2
161335221	RES CARBON FILM 220 OHMS	4
161335222	RES CARBON FILM 2.2 K	4
161335223	RES CARBON FILM 22 K	3
161335241	RES CARBON FILM 240 OHMS	1
161335242	RES CARBON FILM 2.4 K	2
161335244	RES CARBON FILM 240 K	1
161335272	RES CARBON FILM 2.7 K	4
161335333	RES CARBON FILM 33 K	8
161335391	RES CARBON FILM 390 OHMS	1
161335392	RES CARBON FILM 3.9 K	3
161335510	RES CARBON FILM 51 OHMS	8
161335511	RES CARBON FILM 510 OHMS	36
161335512	RES CARBON FILM 5.1 K	25
161335513	RES CARBON FILM 51 K	2
161335622	RES CARBON FILM 6.2 K	1
161335681	RES CARBON FILM 680 OHMS	5
161335751	RES CARBON FILM 750 OHMS	3
161335752	RES CARBON FILM 7.5 K	1
168531413	RES PREC RN55D 1.62 K	8
168531681	RES PREC RN55D 1.00 MEG	8
181457501	RES VARI CERMET 500 OHMS	1

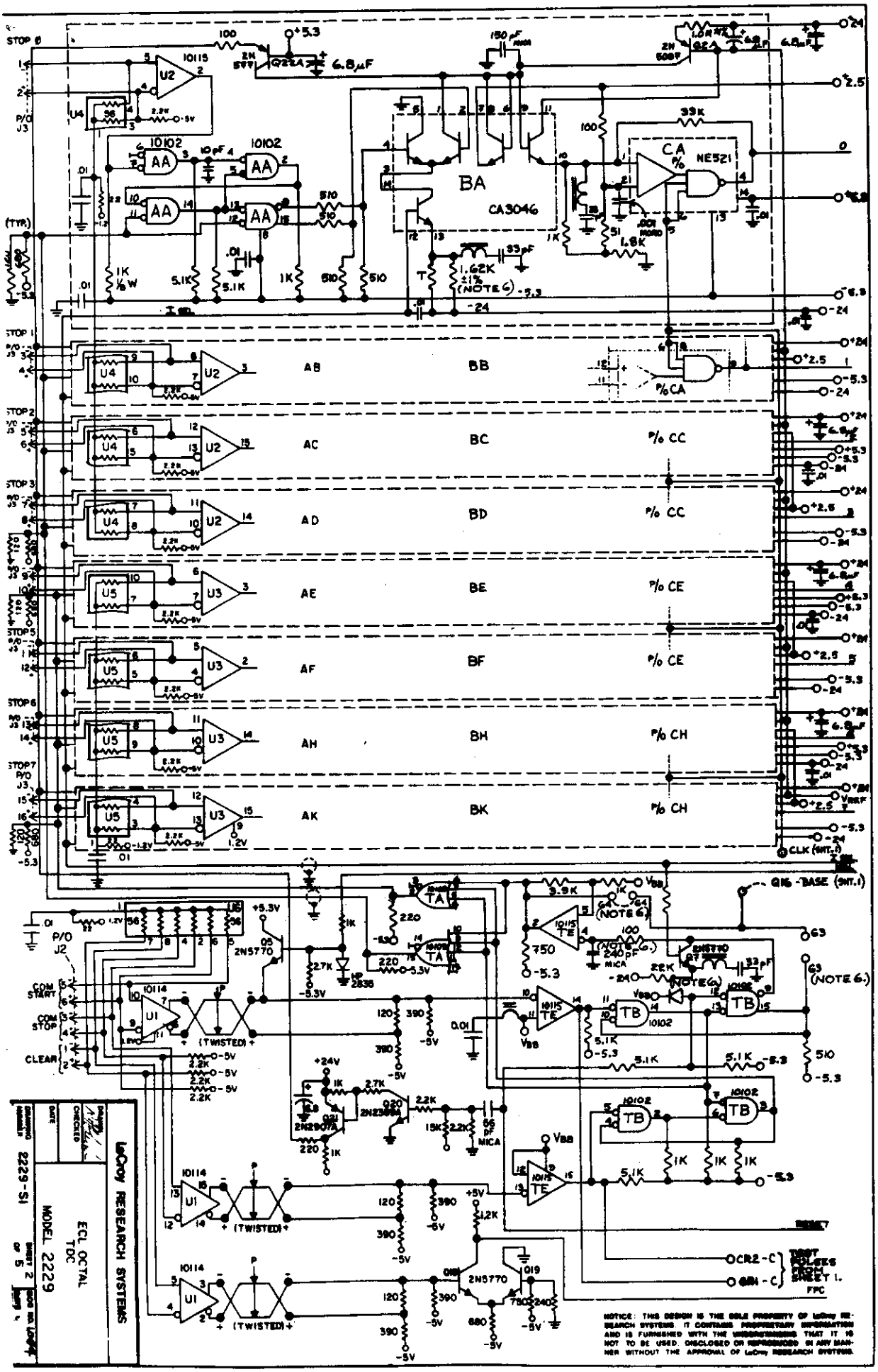
PART NUMBER	DESCRIPTION	QUANTITY PER
181457502	RES VARI CERMET 5 K	3
182537502	RES VARI CERMET 5 K	1
190042560	RESISTOR NETWORK 56 OHMS	2
190842560	RESISTOR NETWORK 56 OHMS	1
200031011	IC J-K FLOP SN7473N	1
200031028	IC 2-INPUT NAND SN74LS00N	3
200031033	IC 2-INPUT NAND SN7403N	4
200031046	IC HEX INVERTER SN74LS04N	2
200031047	IC 3-INPUT NAND SN74LS10N	1
200031051	IC 2-INPUT NOR SN74LS02N	3
200031052	IC 8-INPUT NAND SN74LS30N	2
200041020	IC DECODER SN74LS42N	1
200041049	IC D-TYP FLOP SN74LS175N	2
200041053	IC 3GRAY-DEC DECOD N7444B	1
200042002	IC MULTIVIBRATOR 9602PC	1
200081007	IC MULTIPLEXER SN74LS151	1
204042001	IC 4-5 OR/NOR GT MC10109P	1
204042002	IC NOR GATE MC10102P	9
204042003	IC LINE RECEIVER MC10115P	3
204042015	IC LINE RECEIVER MC10114P	1
208011003	IC SINGLE OP AMP LM301AN	3
208031003	IC VOLT COMPARATOR NE521A	6
208033001	IC TRANS ARRAY CA3046	8
230110005	DIODE SWITCHING 1N4448	12
235010005	DIODE RECTIFIER 1N4005	2
240225702	DIODE ZENER 2.6V 1N702A	1
240225705	DIODE ZENER 4.85V 1N705A	8
253010835	DIODE HOT CARRIER HP2835	2
270110001	TRANSISTOR NPN PN2369A	1
270170001	TRANSISTOR NPN 2N5770	12
275110001	TRANSISTOR PNP 2N2907A	1
275170001	TRANSISTOR PNP 2N5087	8
275170002	TRANSISTOR PNP 2N5771	12
300010001	BEAD SHIELDING FERRITE	19
300020001	BEAD SHIELDING "1/2" SIZE	1
300050001	CHOKE FERRITE SINGLE LEAD	5
302000001	INDUCTOR SPECIAL 1.00 UH	1
400010008	SOCKET IC ST DIP-8	3
400020014	SOCKET IC ST DIP-14	30
400030016	SOCKET IC ST DIP-16	20
405812002	SOCKET STRIP SOLDR 20 POS	9
408063005	W-W PIN, ONE SIDE, 1 WRAP	12
412141505	SWITCH ROTARY PC MTG 1P5T	3
433220002	FUSE PICO II 125V 3 AMP	2
454713016	HDR DIP SOLD TO MALE 16	2
468622002	TEST POINT (JACK) BLU	1
500510004	INSULATOR MICA FOR 8-PIN	3
540203001	SIDE COVER CAMAC STD(LIP)	1
540206078	RAIL CAMAC STD TOP W/LIP	1
540206178	RAIL CAMAC STD BOT W/LIP	1
540209101	REAR PANEL CAMAC SIZE 1	1
555430003	CAPTIVE SCREW ASSEMBLY	1
712229003	PC BD PREASS'Y 2229	1
732229003	FRONT PNL PREASS'Y 2229	1

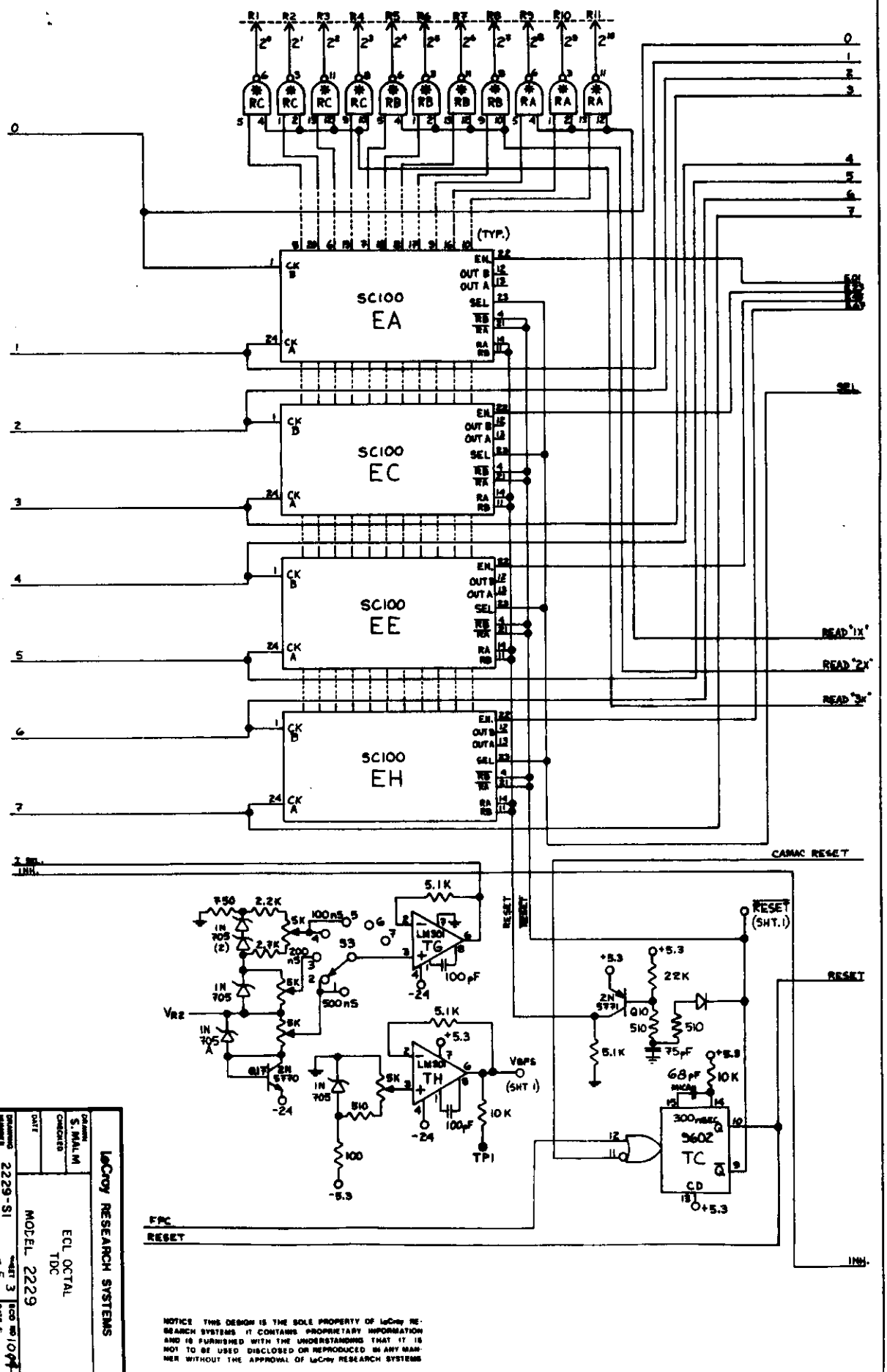
PART NUMBER	DESCRIPTION	QUANTITY PER
732229003	SIDE CAMAC LEFT 2229	1
SC100	IC 11-BIT SCALER SC100	4

End of report. 110 Details encountered.

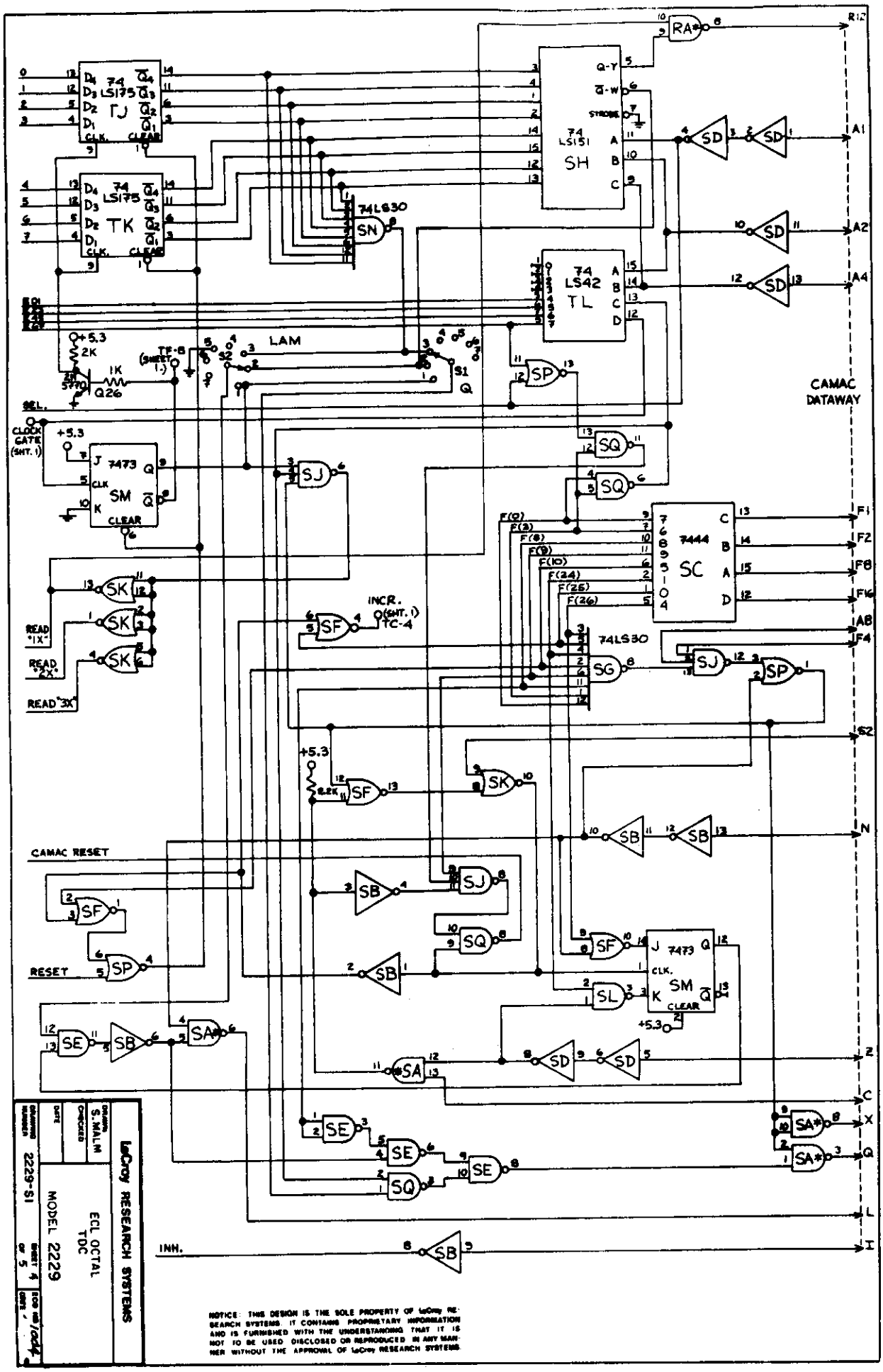


DRAWN	S. MALM	LeCroy RESEARCH SYSTEMS	
CHECKED			
DATE		ECL OCTAL TDC MODEL 2229 (GATED OSC. & TEST CIRCUIT)	
DRAWING NUMBER	2229-S1	SHEET 1 OF 5	SCR NO 1804
			DATE


BA
CA3046
CA
NE521
AB
BB
AC
BC
AD
BD
AE
BE
AF
BF
AH
BH
AK
BK
P/O CA
P/O CC
P/O CE
P/O CH
TA
TB
TE
U1
U2
U3
U4
U5
(TWISTED)
COM START
COM STOP
CLEAR
CLK (SHT. 1)
Q16 - BASE (SHT. 1)
CR2 - C
Q18 - C
TEST POINTS FROM SHEET 1.
RESET
ECL OCTAL TDC
MODEL 2229
LeCroy RESEARCH SYSTEMS
2229-SI
SHEET 2 OF 5
NOTICE: THIS DESIGN IS THE SOLE PROPERTY OF LeCroy RESEARCH SYSTEMS. IT CONTAINS PROPRIETARY INFORMATION AND IS FURNISHED WITH THE UNDERSTANDING THAT IT IS NOT TO BE USED, DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE APPROVAL OF LeCroy RESEARCH SYSTEMS.



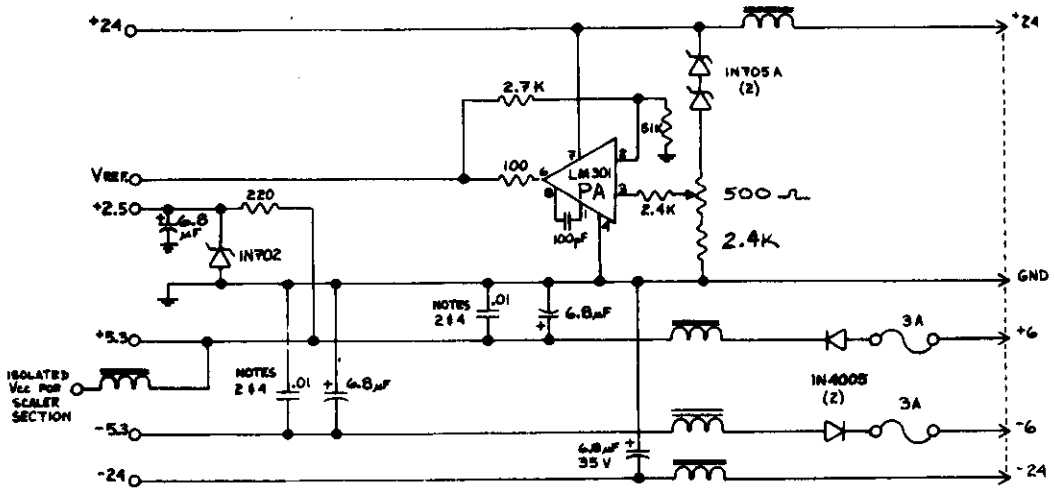
LeCroy RESEARCH SYSTEMS	DRAWN S. MALM	DATE	DRAWING NUMBER 2229-SI
	CHECKED		SHEET 3 OF 5
ECL OCTAL TDC MODEL 2229			ECO NO 10



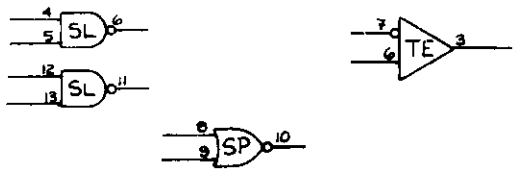
DRAWING NUMBER 2229-SI	DATE	DRAWN S. MALM CHECKED	LeCroy RESEARCH SYSTEMS
SHEET 4 OF 5 SHTS			MODEL 2229 ECL OCTAL TDC

INTEGRATED CIRCUITS, 2229

LeCroy #	I.C.	DESIGNATION	VOLTAGE PINS +24	+5.3	GND	-5.3	-24
200-031-028	SN74LS00	SE, SL, SQ		14	7		
200-031-051	SN74LS02	SF, SP, SK		14	7		
200-031-046	SN74LS04	SB, SD		14	7		
200-031-047	SN74LS10	SJ		14	7		
200-031-052	SN74LS30	SG, SN		14	7		
200-031-011	SN7473	SM		4	11		
200-031-033	SN7403	RA, RB, RC, SA		14	7		
200-041-020	SN74LS42	TL		16	8		
200-041-049	SN74LS175	TJ, TK		16	8		
200-041-053	SN7444	SC		16	8		
200-042-002	9602	TC		16	8		
200-081-007	SN74LS151	SH		16	8		
204-042-001	MC10109	TA			1,16	8	
204-042-002	MC10102	AA, AB, AC, AD, AE, AF, AH, AK, TB			1,16	8	
204-042-003	MC10115	TE			1,16	8	
208-011-003	LM301	TG, TH			7		4
208-011-003	LM301	PA	7		4		
208-031-003	NE521	CA, CC, CE, CH, TD, TF		14	7	13	



UNUSED DEVICES:



NOTES:

1) "T" DENOTES VALUE TO BE CHOSEN AT TEST.
2) ADDITIONAL .01 AND/OR 6.8µF CAPACITORS PLACED ALONG VOLTAGE BUS.
3) UNIDENTIFIED DIODES ARE IN4448.
4) * DENOTES OPEN-COLLECTOR OUTPUT.
5) SEE I.C. LIST ABOVE FOR SCHOTTKY DEVICES USED IN 2229
6) FOR MOD 200 (1,2,5 µsec FULL SCALE) MAKE THE FOLLOWING CHANGES:
   A. REPLACE 1.62K RES BETWEEN SA-13 TO -24 WITH A 16.2K 1% RES.
   B. REPLACE 240pF MICA CAP FROM TE-4 TO GND WITH A 2200pF CERA CAP.
   C. REPLACE 3.9K RES. OF Q25 EMITTER TO -24 WITH A 39K RES.
   D. MOVE JUMPER G-4 TO G-3
   E. REPLACE .001 CAP OFF PIN 2 OF TC TO .01µF. CHG TIME DESIG. FROM 3µS TO 30µS
   F. RES. AT Q-7 EMITTER (22K) MAY BE CHG ± 50% TO OBTAIN SIGNAL AT TE-2 THAT IS SLIGHTLY GREATER THAN 150% OF 1,2,5 SEC. FULL SCALE.

LeCroy RESEARCH SYSTEMS

S. MALIN

ECL OCTAL TDC

MODEL 2229

2229-81

SHEET 5 OF 5