CAMAC MODEL 2323

DUAL GATE AND DELAY GENERATOR

March, 1983

A T T E N T I O N

SEE POCKET IN BACK OF MANUAL FOR SCHEMATICS, PARTS LISTS, AND ADDITIONAL ADDENDA WITH ANY CHANGES TO MANUAL.

CRATE POWER SHOULD BE TURNED OFF DURING INSERTION AND REMOVAL OF UNIT TO AVOID POSSIBLE DAMAGE CAUSED BY MOMENTARY MISALIGNMENT OF CONTACTS.

AN INSTALLATION AND INSTRUMENT CHECKOUT PROCEDURE IS DESCRIBED IN SECTION 1.2

A T T E N T I O N

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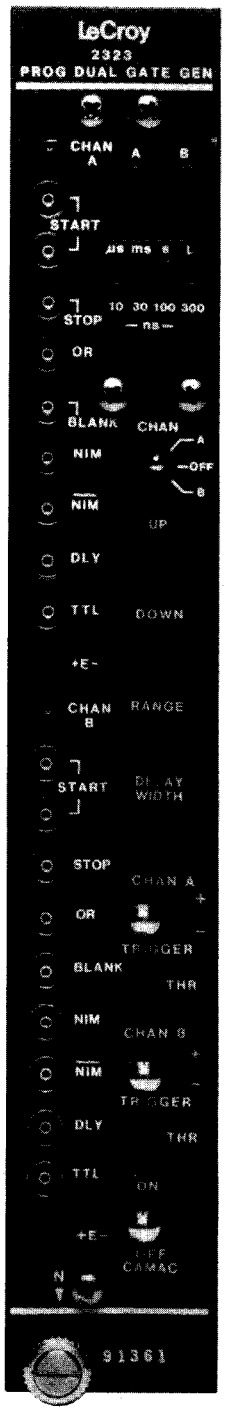
TECHNICAL DATA

LeCroy



CAMAC Model 2323

Programmable Dual Gate and Delay Generator

- **No dead time**
- **Programmable width**
- **Programmable delayed signal**
- **Accepts NIM, TTL or ECL inputs**
- **Range 50 nsec to 10 sec**
- **Manual or CAMAC control**

LeCroy's CAMAC Model 2323 is a fully programmable gate and delay generator packaged with two channels in a double width CAMAC module. Its gate duration is programmable over the range 100 nsec to 10 seconds, covering a dynamic range of eight orders of magnitude. Outputs as short as 50 nsec can be selected at the expense of accuracy and stability. All settings may be programmed under CAMAC control or via front panel switches. Under CAMAC control, settings are overwritten whereas they are incremented under manual control. The Model 2323 offers excellent stability and jitter properties with 0.2% of Full Scale accuracy in the gate setting.

The Model 2323 offers both Start and Stop inputs. This allows the output pulse width to be determined by the Start - Stop time difference in the latched mode or by the internal timer in the preset mode. A Blanking NIM input causes a notch to be taken out of the gate, equal in duration to the blanking input. This is especially useful to gate off data acquisition during spurious periods. Conversely, a NIM OR input causes all outputs to be set to true for the duration of the OR inputs.

The unit offers NIM and $\overline{\text{NIM}}$ outputs equal in duration to the gate width selected. In addition, a DELAY output is produced at the trailing edge of the Gate pulse. The Model 2323 also provides a differential ECL output and a TTL output capable of driving a NIM Bin Gate. Both the ECL and TTL outputs may be driven from either the Gate or Delay circuit. These options are selected by board mounted shorting plugs.

The gate duration and width of the Delayed output are programmable under CAMAC control. Each of the two channels may be set independently. All values which are loaded into the Model 2323 may also be read back via CAMAC. Programming of the delay involves a ten bit "mantissa" and a three bit "characteristic".

The Start input is normally configured to accept NIM signals. A bridged high impedance input is employed to allow the trigger of more than one channel of 2323. The front end of the Start input consists of a comparator circuit, factory adjusted to trigger at -400 ± 50 mV. A front panel accessed multiple turn potentiometer allows the user to adjust the threshold over the range -3 V to $+3$ V. This allows the unit to be triggered by NIM, ECL, TTL or other standard logic signals. A front panel accessed switch selects either the positive-going or negative-going edge as the trigger. The stop input accepts NIM standard pulses.

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SECTION 1

FUNCTIONAL DESCRIPTION

1.1 General Information

1.1.2 Introduction

The CAMAC Model 2323 is a fully programmable dual gate and delay generator. The Gate pulse output width is programmable via CAMAC or manual control over the range 100 nsec (50 nsec at reduced accuracy) to 10 seconds.

The Delay signal starts at the trailing edge of the Gate pulse. Its width is also programmable via CAMAC or manual control to values of 10 nsec, 30 nsec, 100 nsec, or 300 nsec. Settings of both Gate and Delay signals are overwritten under CAMAC control, whereas they are incremented under manual control. Values may be read back via CAMAC.

The Model 2323 is triggerable by either an external START pulse or by a CAMAC command. In the program-selectable Latched mode, the output pulse width is determined by the time between the START and STOP inputs or CAMAC commands.

The Model 2323 provides NIM outputs of the Gate and Delay and a complementary NIM output of the Gate signal. Also, jumper options allow selection of either an ECL Gate or Delay output and selection of either a TTL Gate or Delay output of either positive or negative polarity.

1.1.3 Front Panel Description

Displays

LED's are used to indicate:

1. The channel currently or last selected (A or B)
2. The Gate duration setting (3-1/2 Digit Display)
3. The Gate range setting (μsec, msec, sec, L (latched mode))
4. The Delay width (10, 30, 100, 300 nsec)
5. Channels currently triggered (CHAN A or CHAN B)

Controls:

1. The three position (MOM-OFF-MOM) CHAN switch is used to select either CHAN A or CHAN B. Settings can be changed manually only while the CHAN switch is depressed.

3. OR is a standard NIM input via a Lemo-type connector, with an impedance of 50 Ω. The OR signal produces a gate output for as long as it is asserted.

4. BLANK is a standard NIM input via a Lemo-type connector with an impedance of 50 Ω. The BLANK signal cancels the Gate outputs (including an OR signal) for as long as it is asserted.

Outputs:

1. NIM is a NIM-standard output via a Lemo-type connector. This signal goes low (-16 mA) for the Gate duration. The risetime is $\leq$ 2 nsec and falltime is $\leq$ 2.5 nsec.

2. Complementary NIM is a NIM-standard output via a Lemo-type connector. This signal goes high (0 mA) for the Gate duration. The risetime is $\leq$ 2 nsec and falltime is $\leq$ 2.5 nsec.

3. DLY is a NIM-standard output via a Lemo-type connector. This signal goes low (-16 mA) at the trailing edge of the gate signal for the delay duration (10, 30, 100, or 300 nsec). It will be reset high if the leading edge of a new gate occurs during the delay pulse. The risetime is $\leq$ 2 nsec and the falltime is $\leq$ 2.5 nsec.

4. TTL is an N-channel FET, open-drain output via a Lemo-type connector. This signal has the option of being normally off (+ polarity) and going high for the gate or delay duration, or normally on (- polarity) and going low for the gate or delay duration. Polarity and gate or delay options are selectable with shorting plugs*. Factory set for - Gate output. There is space available on the board for an optional 1/2 w pull up resistor to + 5 V (typically 50 Ω). Note: The 50 Ω pull up (to match 50 Ω cable) will enable operation with output pulse durations set for 30, 100 or 300 nsec. For 10 nsec operation use the NIM output discussed above.

5. +E- is an ECL differential pair output via a 2 - pin connector. The + (-) signal goes high (low) (-0.8 V (-1.7 V)) for either the gate or delay duration. These options are selectable with shorting plugs*. Factory set for Gate output

1.1.4 Options

The following options are made available to the user, see Figure 1. They are located at the front panel end of the main pc board. Note that there are two identical sections each taking up half of the board space. Channel A (B) is located at the top (bottom).

*early versions use wire wrap jumpers.

Should the user wish to terminate the START input with a resistor to ground (typically 50 Ω), space is available at the front panel side of U55 (U60), the AM685's, for an 1/8 w resistor.

Should the user wish to place a pull-up resistor to +5 V (typically 50 Ω on the open drain of the TTL output, space is available at the front panel side of Q26 (Q59), the metal can 2N6659 FET's, for a 1/2 w resistor.

The TTL and ECL outputs are factory set for the Gate output and the TTL polarity is negative (normally on). However, should the user wish to set either or both of these outputs for the delay output or change the TTL polarity, it can be done by moving the shorting plugs according to the table below. The wire wrap pins and shorting plugs are located between and in the vicinity of U58 (U63) and U59 (U64).

LOGIC	OUTPUT	CONNECTIONS
ECL	GATE	B-C *
ECL	DELAY	B-E
-TTL	GATE	Z-A, Y-C, S-W, T-V *
-TTL	DELAY	Z-D, Y-E, S-W, T-V
+TTL	GATE	Z-A, Y-C, S-V, T-W
+TTL	DELAY	Z-D, Y-E, S-V, T-W

*Connections made at factory

1.2 Installation

1.2.1 Inspection

Upon receipt of the 2323, it is recommended that a careful inspection be performed to insure that no damage occurred during transit.

The shipping box has been custom designed for this unit and should be saved should shipping be necessary. After removal from the box, the unit should be examined for physical damage to the body and front panel. Actuate the switches without power to assure physical integrity.

1.2.2 Instrument Check-out

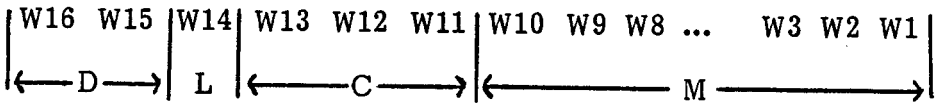
Place unit in a CAMAC crate. Switch power on and flip CAMAC switch off.

Push the CHAN switch to A and observe that the A indicator is on. Repeat for channel B.

CAMAC Commands:

F(1)•A(0)	-	READ CHANNEL A PROGRAMMING WORD
F(1)•A(1)	-	READ CHANNEL B PROGRAMMING WORD
F(9)•A(0)	-	STOP CHANNEL A OUTPUT
F(9)•A(1)	-	STOP CHANNEL B OUTPUT
F(17)•A(0)	-	WRITE CHANNEL A PROGRAMMING WORD
F(17)•A(1)	-	WRITE CHANNEL B PROGRAMMING WORD
F(25)•A(0)	-	START CHANNEL A OUTPUT
F(25)•A(1)	-	START CHANNEL B OUTPUT
C or Z	-	STOP CHANNELS A AND B OUTPUTS

The CAMAC programming word is 16-bits wide and is divided up into 4 segments.



The first 10-bits, W1 - W10, are the mantissa (M). This number, seen in the 3-1/2 digit display, ranges from 0 to 1023.

The next 3-bits, W11 - W13, are the characteristic (C). It sets the order of magnitude of the gate duration.

The next bit, W14, is the latch bit (L). When L=0, the gate duration equals $M \cdot 10^C$ nsec. When L=1, the gate duration equals the time between STOP and START.

The next 2-bits, W15 - W16, determine the delay width (D).

D	WIDTH
00	10 nsec
01	30 nsec
10	100 nsec
11	300 nsec

The CAMAC START and STOP commands perform the same function as the external START and STOP inputs.

The CAMAC C or Z commands shut down both outputs simultaneously.

NOTE: In the CAMAC mode, the TRIGGER switches and the threshold pots have no effect.

SECTION 2

TECHNICAL DESCRIPTION

2.1 Introduction

The Model 2323 consists of two identical wide-range timers in a number two CAMAC module. There are three sections to the 2323. The first section is the gate generator (two identical gate generators). The second section is the CAMAC decoders and buffers. The third and final section provides all manual controls. The gate and the CAMAC sections are on the main pc board and the manual controls are located on the auxiliary board.

2.2 Gate Generator Start Circuitry

The START signal is detected by a 685 comparator. The bias input is supplied by a multi-turn potentiometer (test point provided). The input range is at least ± 3 V. The outputs of the 685 are ORed with the TRIGGER switch. This disables one of the two 685 outputs by holding it high and is used to select the positive or the negative edge. The two outputs are differentiated and used as two of the three inputs to the OR gate (U57). The third input is the CAMAC trigger, F(25). A bias voltage is applied to the latch enable input, pin 6, of the 685 to provide about 50 mV of hysterisis.

The output of the start circuit is used to preset the busy flip-flop. The reset of the busy flip-flop is an emitter OR of the STOP pulse from the STOP level shifter and the interrupt signal from the CAMAC section (F(9) or C or Z). The clock input comes from the timing circuitry.

The Q output of the busy flip-flop is ORed with the output of the OR level shifter. The OR of these two signals is ANDed with the output of the BLANK level shifter. The output of this gate is the input to the NIM and -NIM drivers. The Q output of the busy flip-flop is used to trigger the Delay Pulse single shot. The output of the single shot is translated to a NIM level signal by Q24 and Q25. TTL and ECL drivers are triggered by either signal, depending upon the options selected. TTL polarity is determined by which transistor (Q28 or Q27) drives the gate of the FET (Q26).

The Q output of the busy flip-flop also goes to the busy LED driver. This is a two-stage pulse-stretcher designed to stretch a pulse of 50 ns to a pulse wide enough to provide a visible LED flash. For wider pulses the LED will appear to stay on.

The basic operation of the timing circuit, in the fastest range, is to switch the amount of current supplied to a capacitor so that it first charges to a programmed DAC voltage and then discharges to its starting condition (0 Volts). This constitutes one complete ramp cycle. The signal that comes at the end of each ramp cycle is used as a clock by a seven stage decade counter. A multiplexer is used to select the output from the proper stage to give either 1, 10, 100, etc., ramp cycles before turning off the busy flip-flop.

The delay pulse width monostable is composed of a programmable current source (U15, Q67, Q68, Q69), a current switch (Q1 and Q2), ramp circuitry (Q3 and Q4), a comparator (U56), and gates (U57). At the trailing edge of the gate pulse, the current switch is turned off and the programmed current source is allowed to charge up the ramp capacitor. The comparator switches when the ramp gets above a predetermined level. If the comparator has not switched yet and the busy flip-flop is still off, the 2323 will generate a delay pulse. (Note that the delay pulse will terminate as soon as the 2323 is retriggered. This will prevent the delay width pulses from overlapping).

2.3 CAMAC

The CAMAC decoding is primarily done by gates U11-1, U4, U9-11 and U9-6, and the decoder U1. The S2 pulse is differentiated and ANDed with the interrupt (F(9) or C or Z) and trigger (F(25)) decodes. The Write decodes (F(17)) are ANDed with S1. The Read decodes (F(1)) are ORed to provide the Read signal which enables the output gates, U7, U8, U12 and U13. The Write decodes are also ORed to provide a signal (WE) to enable the W line buffers, U5 and U6, and to disable the channel A and B status registers. Two signals, (X AND S1) and A(1) are passed to the manual control board to load the status register with the contents of the channel status register that is being addressed by CAMAC. Gates U2-6 and U2-11 are used to OR the channel display select information from the CAMAC section with the information from the manual control board. Gates U17-13 and U17-1 are used to OR the Write signals from the CAMAC section with the write signals from the manual control board.

2.4 Manual Controls

NOTE: Component designations used in the following description refer to the manual control board, except as noted.

The Channel Select and Enable switch is tied directly to the preset and reset inputs of the channel flip-flop (U24). The switch is also connected to gate U18-3 which serves as an OR gate and generates the manual override signal (MO). This signal is delayed through inverters U10-8 and U10-10 to generate the manual enable signal (ME). The output of gate U18-6 is a pulse just before the leading edge of the manual enable signal. When a channel is selected with the switch, the pulse from U18-6 is used to select and enable one channel's status register. This is done with the manual display signals MDA and MDB. The trailing edge of the pulse is used to load the display status register (LOAD signal). The manual enable signal (ME) is then used to output the display status register to the channel status registers. The manual ENABLE signal is then ANDed with the clock from U-12 to provide a manual write signal (either MWA or MWB). This manual write signal constantly updates the selected channel's status registers with the contents of the display status register. Any changes made manually are then transferred immediately to the channel status register. The outputs of U24 are also buffered and used to drive the channel lights.

Debouncing of the range and delay width switches is accomplished with the circuitry associated with U8. The pulses output from these comparators are used to increment the range counter and the delay width counter.

The display clock generator provides both a two-speed clock to the time up/down counter and the address lines to the digit select decoder. Before the up or down buttons are pushed, U1 and U2 are held reset. When one of the buttons is pushed the counter is enabled and every time U2 generates a carry-out signal one clock pulse from U11-11 is gated to the time up/down counter. The carry-out signal from U2 also allows U1 to increment. When U1 reaches a count of 8, and U2 generates a carry-out, the P enable inputs of U1 and U2 are disabled. This allows all the clock pulses from U11-11 to be sent to the time up/down counter. The two speeds are approximately 2 Hz and 32 Hz.

The display status register consists of the time up/down counter (U5, U6 and U7), the range counter (U4), the delay width counter (U3) and the display register tristate buffers (U13 and U15). The time up/down counter and the delay width counter are binary counters and the range counter is a decimal counter. Counts 8 and 9 are used for the latch mode.

The binary information in the mantissa up/down counter is supplied to the binary to BCD convertor (U20, U21, U22, U29, U30, and U31). The BCD output is passed to U27 and U28 which serve as a digit multiplexer. The multiplexer output is the input of U25, a BCD to 7-segment decoder which drives the segments of the digital display. The digit select lines decode the display address and use this information to drive the digits of the digit display (through the buffers of U35). The decoded digit information is also used to control the digit multiplexer and to provide the inputs to the decimal point decoder (U33). The most significant digit signal (MSD) is used to blank the leading digit if it is a zero. The latch signal, CRA3, is used to blank the display in the latch mode. The 4 most significant bits of the mantissa, CB6-9, are combined to provide an input to the decimal point driver that causes all of the decimal point segments to light if the mantissa is below 64. (This is a warning to the user to change to the next range down if possible).

A programmable Read Only memory is used to decode the range information and the delay width information and also drive the LEDs.

Transistors Q18, Q19, and Q20 form two 7 mA current sinks. One is connected to a current switch (Q22 and Q23); the other is connected to the current mirror consisting of transistors Q6, Q7, Q8, and Q9. This current mirror also divides the input current by two. The result of switching the 7 mA current sink and not the 3.5 mA current source onto the ramp capacitor is to alternately charge and then discharge the ramp capacitor. The ramp switch is controlled by the ramp flip-flop. Transistor Q21 is a common base stage used to make the current sink and current switch appear as a better current sink. The upper limit of the ramp is determined by the detector formed by transistors Q11, Q12, and Q13.

When the ramp goes more positive than the voltage on the Q13 emitter, Q12 turns on and presents an ECL "1" to U52. This signal, called "high trip", presets the ramp flip-flop and turns the current sink onto the ramp, causing it to ramp down.

The lower limit of the ramp is determined by the detector formed by transistors Q15, Q16 and Q17. These transistors form a differential amplifier with one input tied to the DAC reference ground. The collector of the opposite transistor is tied to its base which allows current to be switched into the ramp to satisfy the current sink. This stops the ramp from going down below ground. The signal developed at Q15 collector is the "low trip" signal. The "low trip" signal is gated with the "off" signal to reset the ramp flip-flop which causes the ramp to start going high again.

The "low trip" signal is also ANDed with the counter stop signal to provide a clock to the busy flip-flop to turn it off. The Q output, called "off", is ORed with the high trip signal to preset the ramp flip-flop. The "off" signal clamps the ramp to its low (ground) state.

The output of the gate combining the "off" and "low trip" signals is translated to a TTL level and used as the clock to the scalers for the longer time ranges.

The counter is a seven-stage decade counter with the terminal count output of each stage tied to a multiplexer. The multiplexer is controlled by the range select information stored in the status register for that channel. In the 1.0 microsecond full scale range (range 0) the multiplexer always presents a low at U45 pin 6 which generates a counter-stop signal. In the latch range (range 8) the multiplexer always presents a high at U45 pin 6 and no counter stop is ever generated. For all other ranges, the counter stop signal is generated during the final ramp cycle.

The upper ramp limit, and therefore the ramp cycle time, is determined by a 10 bit DAC. The DAC is programmed by the lower 10 bits of the status word, B0 to B9. A potentiometer for trimming the input voltage to the reference input of the DAC is used for gain adjustment. Another potentiometer is used to provide an offset adjustment by providing extra current to U18, an operational amplifier used as a summing amplifier.

Hold the CHAN switch at A and push and hold the UP switch. The display advances at about 2 Hz for the first eight counts and then changes to a faster rate. Push and hold the DOWN switch and observe that the display counts down at the same rate as above.

Repeat for channel B.

Note that all decimal points are lit for values from 0 to 63 and only one is lit for values thereafter.

Advance the range setting by pushing the RANGE switch. The decimal point and the range indicators show that the unit is advancing from .XXX μsec to X.XX sec. The next two increments are the Latched mode, during which the display blanks and the L indicator comes on.

Advance the delay width setting by pushing the DELAY WIDTH switch. The delay width indicators advance in the following order: 10, 30, 100, 300 nsec.

Note that with the CHAN switch in the off position, the UP, DOWN, RANGE, and DELAY WIDTH switches have no effect.

1.3 Operating Instructions

1.3.1 Manual Operation

With the CAMAC switch off, the 2323 responds only to the front panel switches and inputs. Any Gate duration and Delay width can be programmed manually into the 2323 and can be changed only manually.

After setting all values, one sets the trigger threshold for the START signal, selects the positive or negative-going edge with the TRIGGER switch, and applies the START signal to generate an output. Since the factory presets the trigger threshold to -400 + 50 mV, a NIM pulse makes a convenient START signal. In this case, one of the two START inputs should be terminated in 50 Ω, unless daisy chaining is desired.

It is possible to generate one output pulse (or a train of output pulses) without a START signal by flipping the TRIGGER switch.

1.3.2 CAMAC Operation

With the CAMAC switch on, the 2323 responds to the CAMAC Commands listed below. The unit responds to the front panel switches, but anything programmed in manually will be overwritten immediately should a CAMAC WRITE command be executed. The unit will respond also to the front panel inputs in this mode.

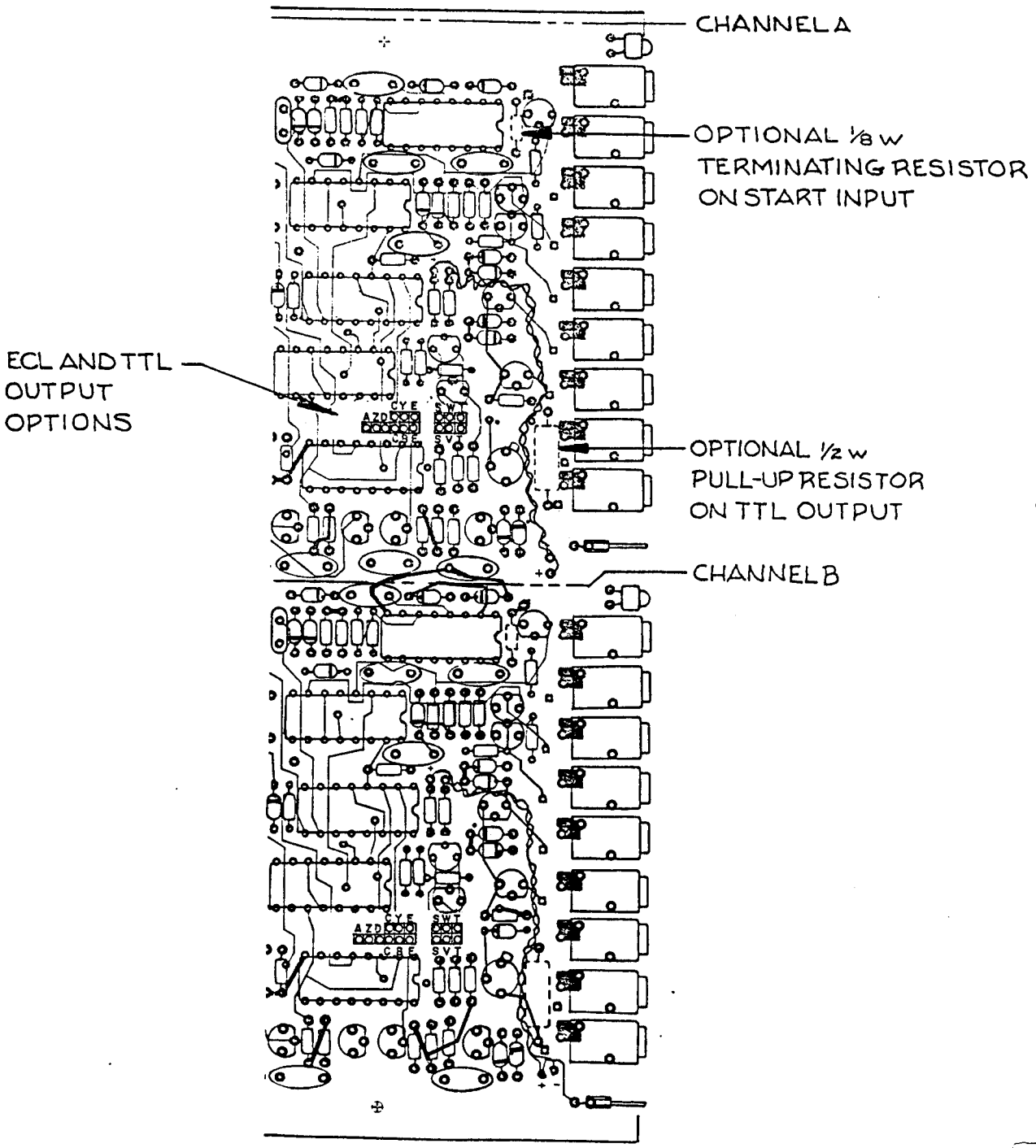

CHANNEL A
OPTIONAL 1/8 W
TERMINATING RESISTOR
ON START INPUT
ECL AND TTL
OUTPUT
OPTIONS
OPTIONAL 1/2 W
PULL-UP RESISTOR
ON TTL OUTPUT
CHANNEL B

Figure 1

2. The push button UP (DOWN) switch is used to increment (decrement) the display setting. The display increments (decrements) at about 2 Hz for the first eight counts and then changes to a faster rate.

3. The push button RANGE switch selects the order of magnitude of the gate setting and advances the decimal point and the range setting indicators accordingly. The indicators advance from μsec to sec and then the display goes blank for two increments as the L indicator comes on. This is the Latched mode.

4. The push button DELAY WIDTH switch selects the width of the Delay pulse and advances the Delay width indicators accordingly.

5. The two position, locking TRIGGER switches (one for each channel) select either the positive-going (+) or the negative-going (-) edge of the START pulse as the trigger.

6. The front panel accessed multi-turn potentiometers and test points (one for each channel) are used to set the threshold above which the START pulse will trigger the unit. The range is -3 V to +3 V. Operates in conjunction with the polarity selecting trigger control described in 5 above.

7. The two-position, locking CAMAC switch selects either manual control (OFF) or CAMAC control (ON). Manual controls work with CAMAC ON as long as they are not overwritten by a CAMAC write command.

Inputs:

1. START is a bridged, high impedance pair of inputs via two Lemo-type connectors, allowing for the possibility of daisy-chaining START signals. The input threshold level is factory adjusted to -400 $\pm$ 50 mV to accept NIM inputs and is adjustable over a range of $\pm$ 3 V via the front panel potentiometer. The positive or negative-going edge (selected by the TRIGGER switch) of the START signal initiates the timing cycle. A 50 Ω terminator should be employed in the unused START input. Alternatively, there is space available on the board for an optional 1/8 W, 50 Ω terminating resistor.

2. STOP is a standard NIM input via a Lemo-type connector, with an impedance of 50 Ω. In the latched or the preset mode, the STOP signal terminates the timing cycle.

SPECIFICATIONS
CAMAC Model 2323
DUAL PROGRAMMABLE GATE AND DELAY GENERATOR

Gate Width

Range: 100 nsec to 10 sec; pulses to 50 nsec at reduced accuracy and stability
Accuracy: ±0.2% of full scale (mantissa)
Temperature Stability: <200 ppm/°C
Jitter: <0.2% of setting
Resolution: 0.1% of full scale (mantissa)

Delay Width

Range: 10 nsec to 300 nsec
Width Options: 10 nsec, 30 nsec, 100 nsec, 300 nsec
Accuracy: ±20%

Inputs

START: Bridged high impedance pair. Lemo-type connectors. Input trigger level adjustable over the range ±3 V via front panel potentiometer. As supplied, the input is set to trigger at −400±50 mV with a negative going edge. Action of the input is to initiate the timing cycle.

STOP: Standard NIM. Impedance 50 Ω. Lemo-type connectors. Action of the input is to terminate the timing cycle in the latched mode. Active in both latched and preset modes. The delay is <20 nsec.

OR: Standard NIM input via Lemo-type connector. Input impedance 50 Ω. Produces NIM, $\overline{\text{NIM}}$, ECL, and TTL outputs as long as the OR signal is asserted.

BLANK: Standard NIM input via Lemo-type connector. Input impedance 50 Ω. Cancels NIM, $\overline{\text{NIM}}$, ECL, and TTL outputs as long as the BLANK signal is asserted. Overrides OR input.

Outputs

BUSY LED: Indicates unit is active; duration stretched to 1 msec minimum.

NIM: Standard NIM (−16 mA) signal via a Lemo-type connector. Goes low for gate duration. Risetime ≤2 nsec. Falltime ≤2.5 nsec.

$\overline{\text{NIM}}$: Standard NIM (−16 mA) signal via a Lemo-type connector. Goes high for gate duration. Risetime ≤2 nsec. Falltime ≤2.5 nsec.

ECL: One per section. Complementary ECL levels via a 2-pin connector. PC mounted shorting plug allows this output to be logically identical to the GATE or DELAY pulse or their complements.

TTL: One per section. An FET open drain output (+35 V Max, 250 mA, 0.5 W Max). PC mounted shorting plug allows this output to be logically identical to the GATE or DELAY pulse or their complements.

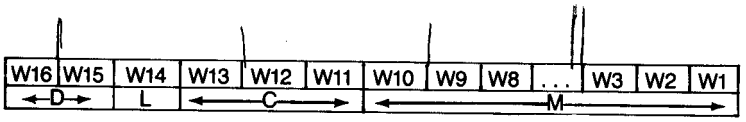
DELAY: Standard NIM (−16 mA). Lemo-type connector. Delayed from start of NIM by the gate width. (Goes low at trailing edge of gate). Programmable for 10, 30, 100 or 300 nsec duration. Risetime ≤2 nsec.

CAMAC COMMANDS

F(1) • A(0)	Read channel A programming word.
F(1) • A(1)	Read channel B programming word.
F(9) • A(0)	Stop channel A gate.
F(9) • A(1)	Stop channel B gate.
F(17) • A(0)	Write channel A programming word.
F(17) • A(1)	Write channel B programming word.
F(25) • A(0)	Start channel A gate.
F(25) • A(1)	Start channel B gate.
C or Z	Stops channels A and B gates.

Programming Word

M = mantissa
C = characteristic
L = latch bit
D = delayed pulse width



Programmable mode: (L=0). Duration = M•10^{C} nsec. (For 100≤M≤1023). Settings of 50≤M<100 at reduced accuracy and stability.

Latched mode: (L=1). Duration = time between STOP and START inputs.

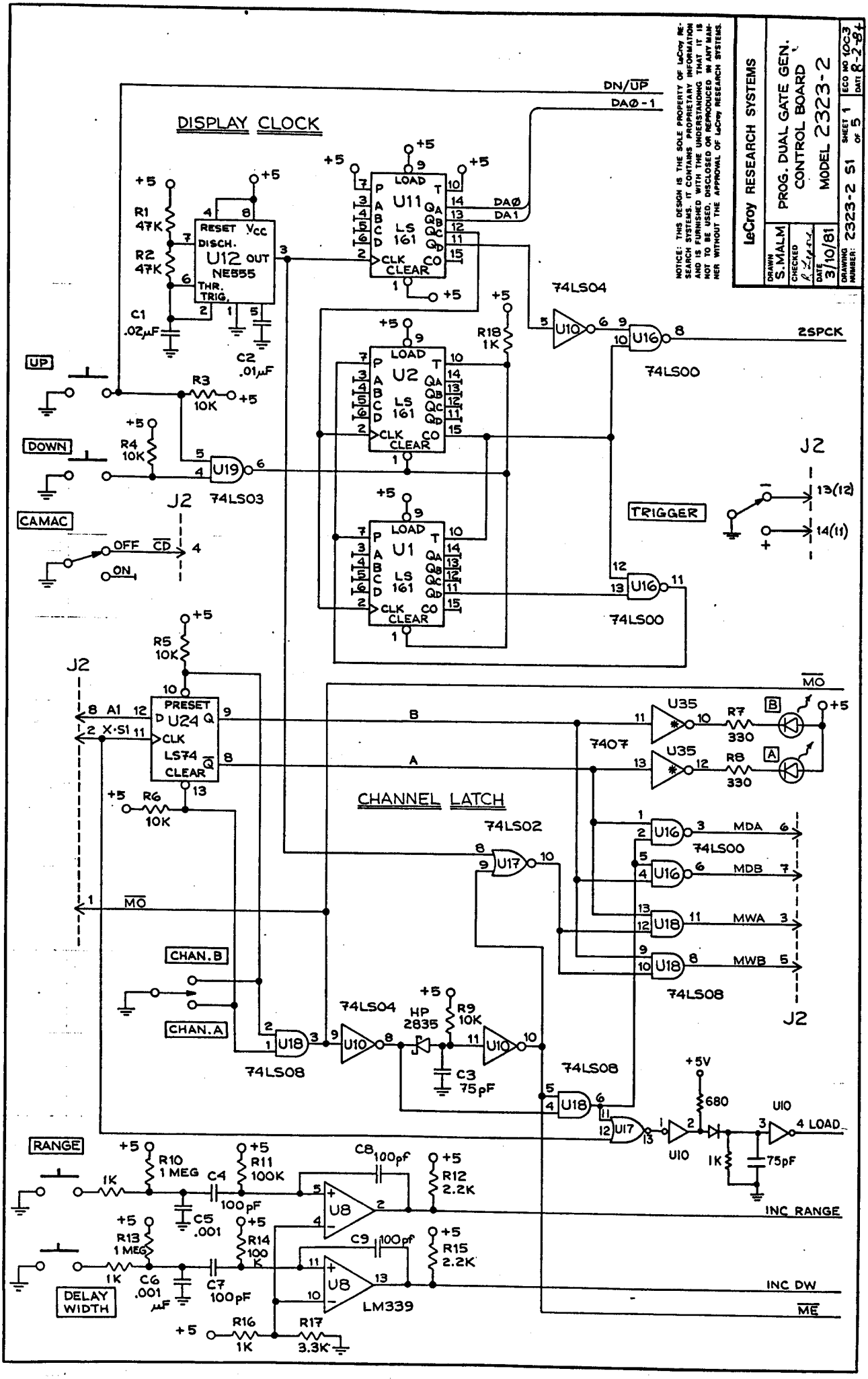
Delay Options:

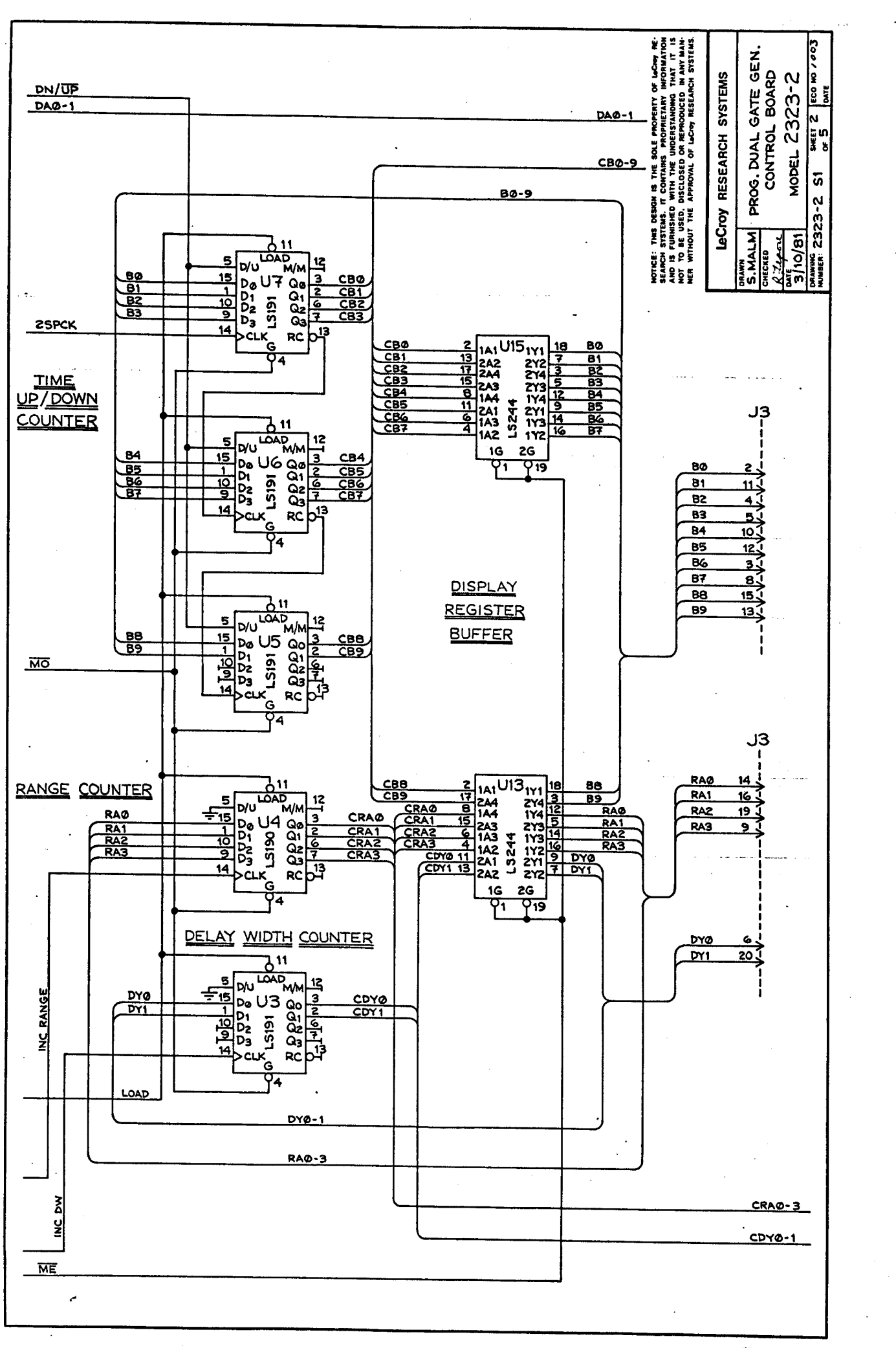
D	Width
00	10 nsec
01	30 nsec
10	100 nsec
11	300 nsec

General

Input-Output Delay: 24 nsec (Start input to NIM output).
Recovery time: None. The unit may be retriggered any time after the timing cycle has been completed.
Packaging: Double width module in conformance with CAMAC standard for nuclear modules. (ESONE Report EUR4100 or IEEE Report #583.). RF shielded CAMAC #2 module.
Power Consumption:
1.8 A @ +6 V
1.3 A @ −6 V
50 mA @ +24 V
75 mA @ − 24 V

SPECIFICATIONS SUBJECT TO CHANGE


DISPLAY CLOCK
DN/UP
DA0-1
DA0
DA1
LeCroy RESEARCH SYSTEMS
PROG. DUAL GATE GEN. CONTROL BOARD MODEL 2323-2
DRAWN S.MALM
CHECKED
DATE 3/10/81
DRAWING NUMBER: 2323-2 S1
SHEET 1 OF 5
ECO NO 1003
DATE R-2-84
NOTICE: THIS DESIGN IS THE SOLE PROPERTY OF LeCroy RESEARCH SYSTEMS. IT CONTAINS PROPRIETARY INFORMATION AND IS FURNISHED WITH THE UNDERSTANDING THAT IT IS NOT TO BE USED, DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE APPROVAL OF LeCroy RESEARCH SYSTEMS.
R1 47K
R2 47K
C1 .02μF
C2 .01μF
U12 NE555
RESET DISCH. THR. TRIG. OUT Vcc
U11 LS 161
LOAD CLK CLEAR
74LS04
U10
U16
74LS00
2SPCK
R18 1K
U2
U1
UP
DOWN
CAMAC
OFF ON CD
R3 10K
R4 10K
U19
74LS03
J2
TRIGGER
13(12)
14(11)
R5 10K
U24 LS74
PRESET CLK CLEAR
MO
U35
7407
R7 330
R8 330
B
A
CHANNEL LATCH
74LS02
U17
R6 10K
MDA
MDB
MWA
MWB
74LS08
U18
CHAN.B
CHAN.A
HP 2835
R9 10K
C3 75pF
+5V
680
1K
75pF
4 LOAD
RANGE
R10 1 MEG
R11 100K
C4 100pF
C5 .001
C8 100pF
R12 2.2K
INC RANGE
R13 1 MEG
R14 100K
C6 .001 μF
C7 100pF
C9 100pF
R15 2.2K
INC DW
DELAY WIDTH
U8
LM339
R16 1K
R17 3.3K
ME


DN/UP
DA0-1
DA0-1
CB0-9
B0-9
2SPCK
TIME
UP/DOWN
COUNTER
U7
U6
U5
U4
U3
LS191
LS190
U15
U13
LS244
DISPLAY
REGISTER
BUFFER
J3
J3
RANGE COUNTER
DELAY WIDTH COUNTER
MO
INC RANGE
INC DW
LOAD
ME
DY0-1
RA0-3
CRA0-3
CDY0-1
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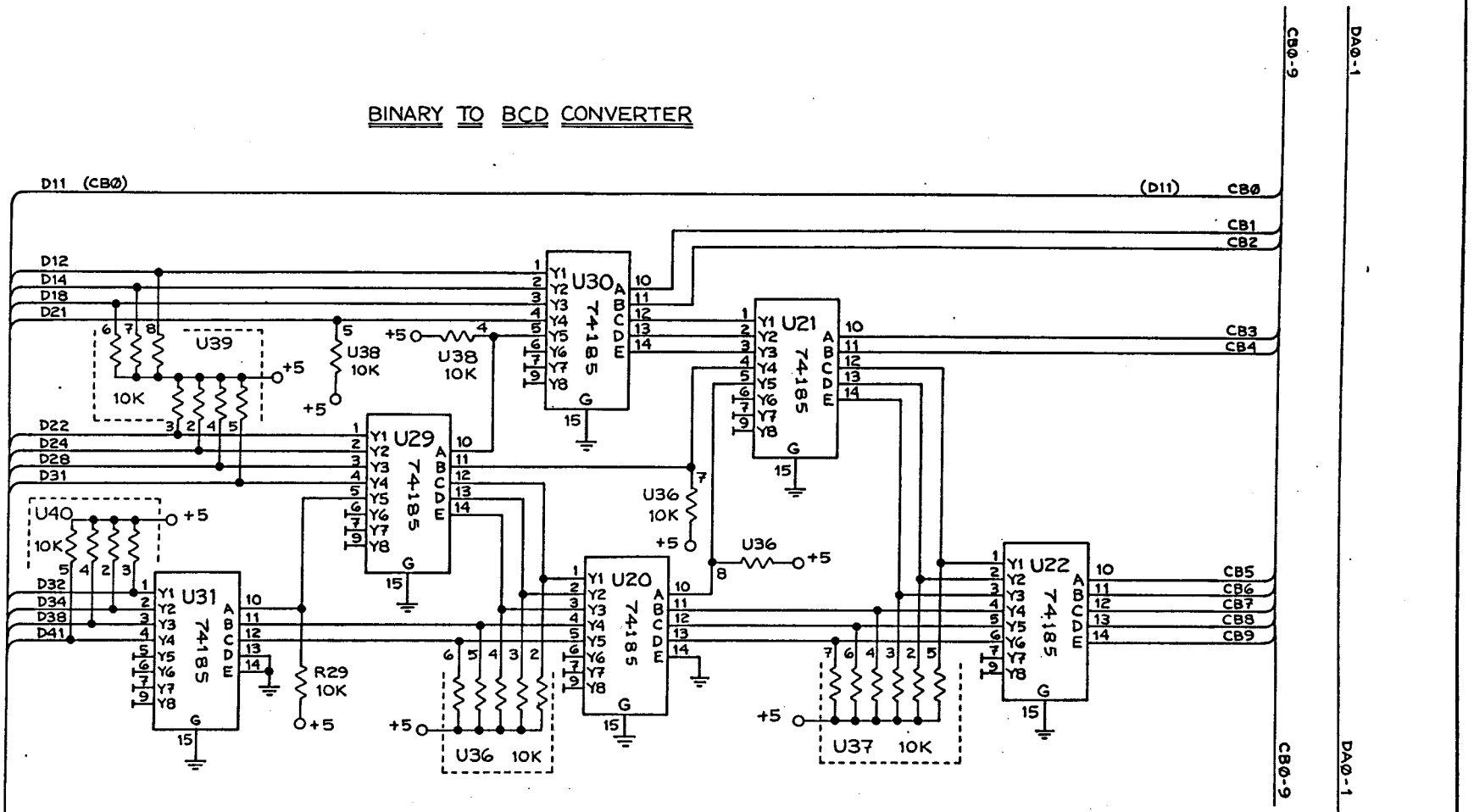
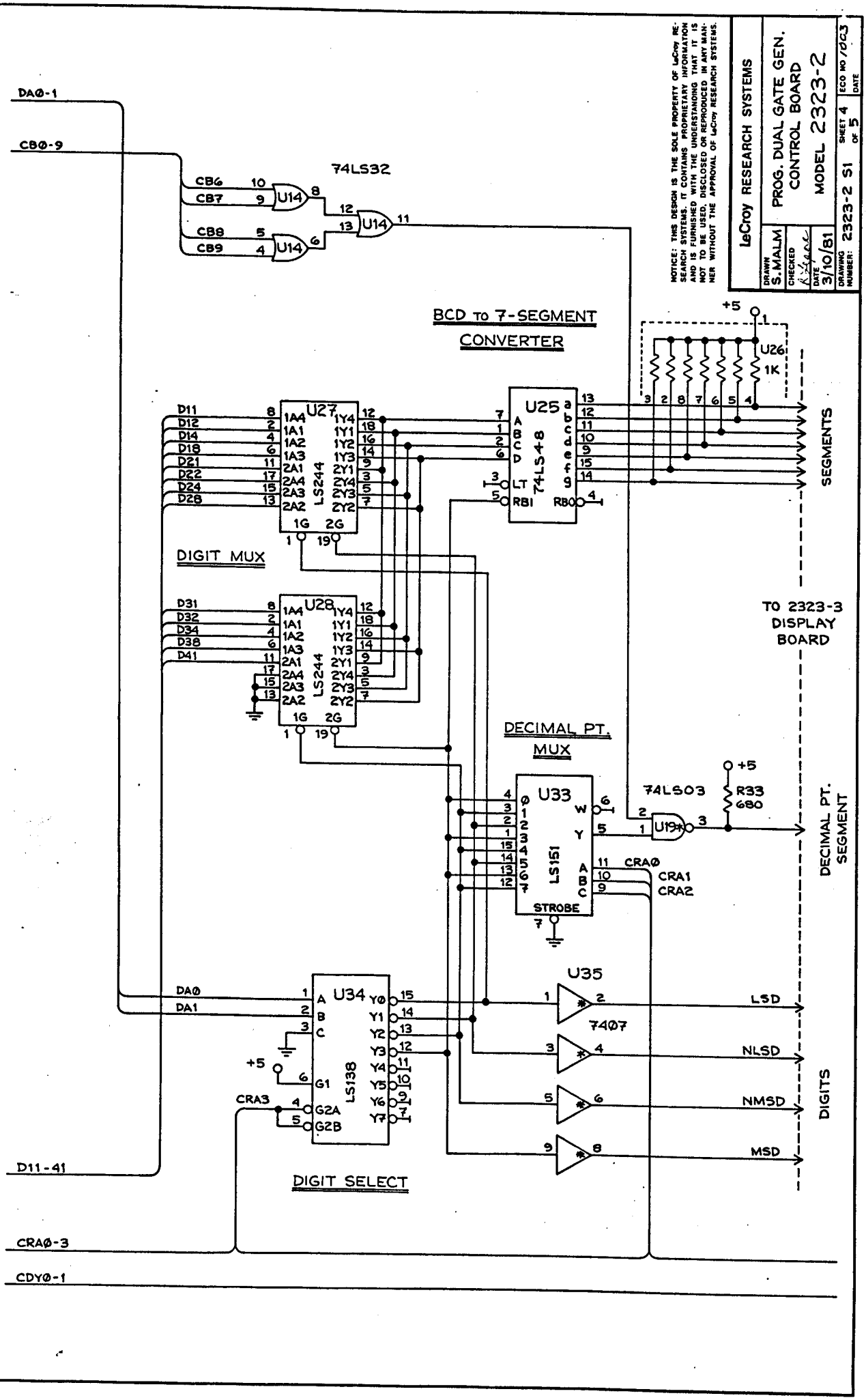
LeCroy RESEARCH SYSTEMS
DRAWN S.MALM
CHECKED
DATE 3/10/81
PROG. DUAL GATE GEN. CONTROL BOARD
MODEL 2323-2
DRAWING NUMBER: 2323-2 S1
SHEET 2 OF 5
ECO NO 1003
DATE

BINARY TO BCD CONVERTER



LeCroy RESEARCH SYSTEMS

DRAWN S. MALM	PROG. DUAL GATE GEN. CONTROL BOARD
CHECKED	MODEL 2323-2
DATE 3/10/81	
DRAWING NUMBER: 2323-2 S1	SHEET 3 OF 5
ECO NO 1003	DATE


NOTICE: THIS DESIGN IS THE SOLE PROPERTY OF LeCroy RESEARCH SYSTEMS. IT CONTAINS PROPRIETARY INFORMATION AND IS FURNISHED WITH THE UNDERSTANDING THAT IT IS NOT TO BE USED, DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE APPROVAL OF LeCroy RESEARCH SYSTEMS.
LeCroy RESEARCH SYSTEMS
PROG. DUAL GATE GEN. CONTROL BOARD
MODEL 2323-2
DRAWN S.MALM
CHECKED
DATE 3/10/81
DRAWING NUMBER: 2323-2 S1
SHEET 4 OF 5
ECO NO 1063
DATE
DA0-1
CB0-9
74LS32
CB6
CB7
CB8
CB9
U14
BCD TO 7-SEGMENT CONVERTER
+5
U26
1K
U25
74LS48
RBI
RBO
SEGMENTS
U27
LS244
D11
D12
D14
D18
D21
D22
D24
D28
DIGIT MUX
U28
D31
D32
D34
D38
D41
TO 2323-3 DISPLAY BOARD
DECIMAL PT. MUX
U33
LS151
STROBE
74LS03
U19
R33
680
CRA0
CRA1
CRA2
DECIMAL PT. SEGMENT
U34
LS138
DA0
DA1
CRA3
G1
G2A
G2B
U35
7407
LSD
NLSD
NMSD
MSD
DIGITS
D11-41
DIGIT SELECT
CRA0-3
CDY0-1

	DEVICE	DESIGNATION	+5	GND
	74LS00	U9, U16	14	7
	74LS02	U17	14	7
*	74LS03	U19	14	7
	74LS04	U10	14	7
*	7407	U35	14	7
	74LS08	U18	14	7
	74LS32	U14	14	7
	7448	U25	16	8
	74LS74	U24	14	7
	74LS138	U34	16	8
	74LS151	U33	16	8
	74LS161	U1, 2, 11	16	8
	74LS185	U20, 21, 22, 29, 30, 31	16	8
	74LS190	U4	16	8
	74LS191	U3, 5, 6, 7	16	8
	74LS244	U13, 15, 27, 28	20	10
	LM339	U8	3	12
	NE555	U12	8	1
	18SA22	U32	20	10
	SPARE	U23		

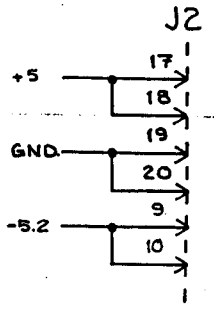
LeCroy RESEARCH SYSTEMS

PROG. DUAL GATE GEN. CONTROL BOARD

MODEL 2323-2

DRAWN S.MALM | CHECKED | DATE 3/10/81

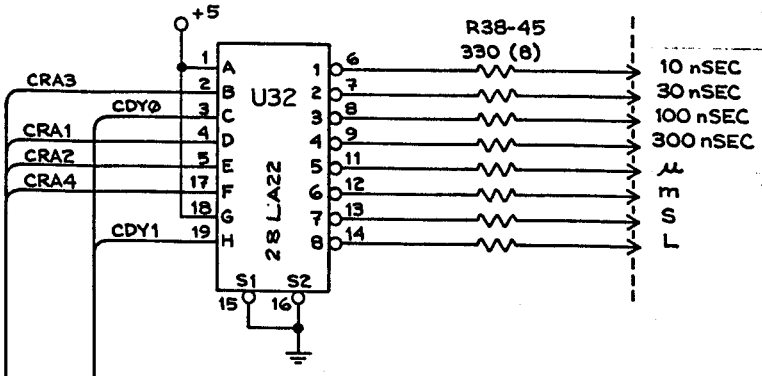
DRAWING NUMBER: 2323-2 S1 | SHEET 5 OF 5 | ECO NO/DCO 3 | DATE



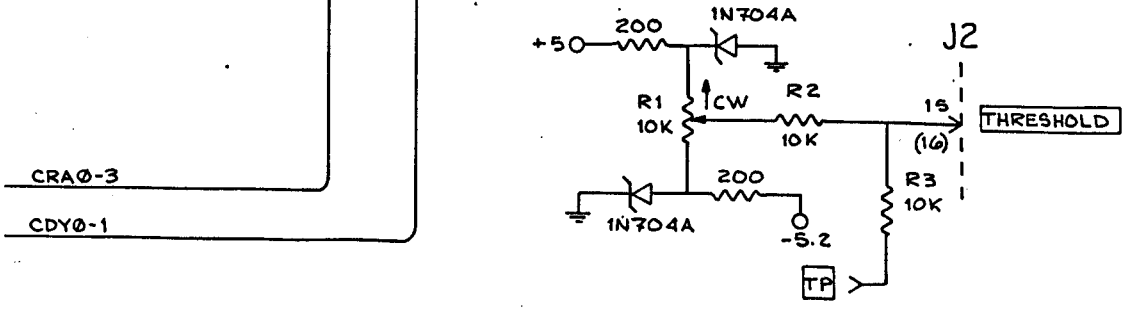
NOTES:
1) UNMARKED DIODES ARE 1N4448.
2) * DENOTES OPEN-COLLECTOR OUTPUTS.
3) ADDITIONAL .01μF AND/OR 6.8μF CAPACITORS, NOT SHOWN, MAY BE USED ON VOLTAGE LINES.
4) REFERENCE DESIGNATIONS:

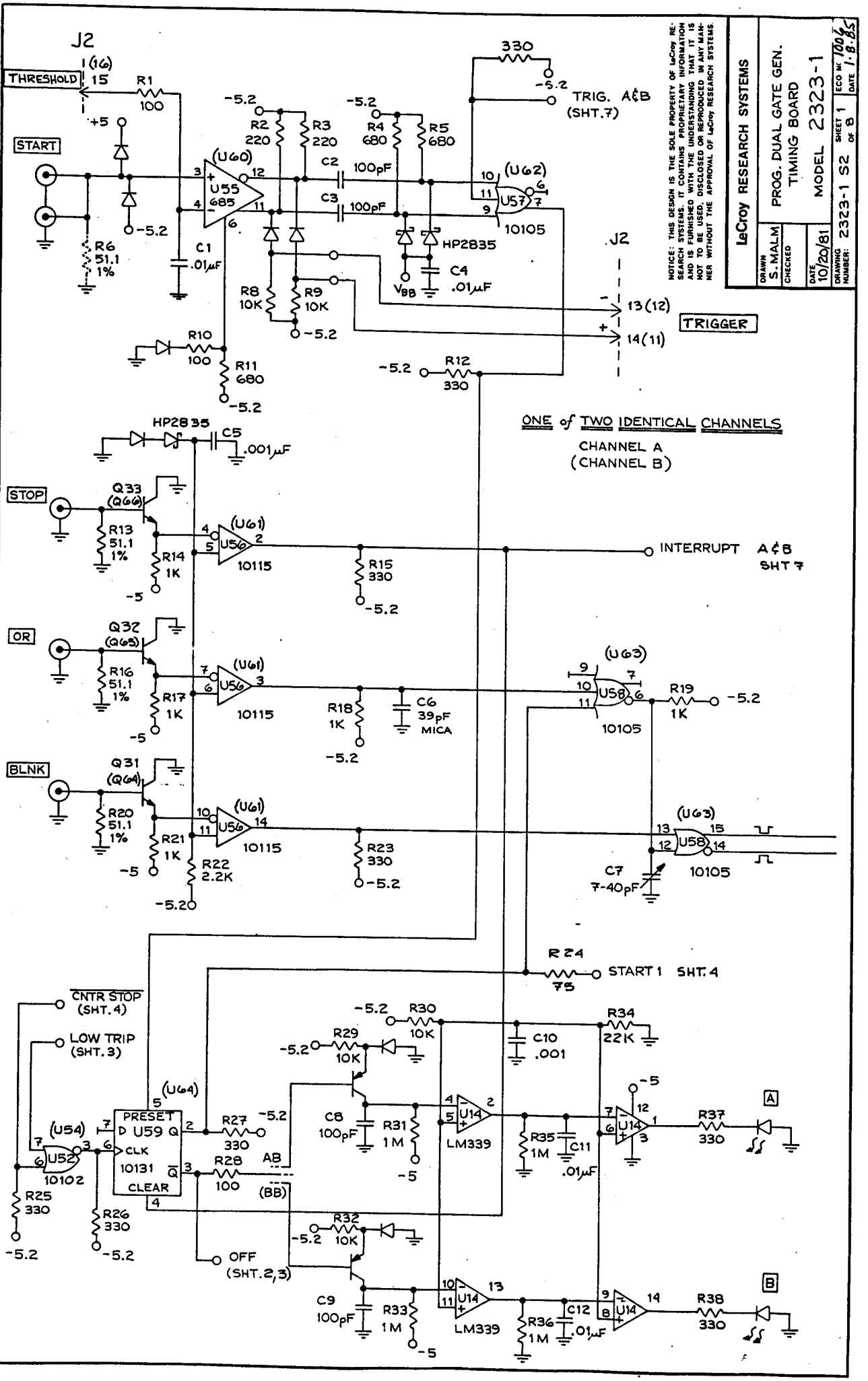
SHT. #	USED	OMITTED
1	R1-20, C1-9	R21-24, C10-12
2		R25-28, C13-15
3	R29	R30-32, C16-18
4	R33,	R34-37, C19-21
5	R38-45,	R46-, C22-

TO 2323-3 DISPLAY BOARD



TIME AND DELAY WIDTH RANGE DECODER





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LeCroy RESEARCH SYSTEMS

PROG. DUAL GATE GEN. TIMING BOARD

MODEL 2323-1

DRAWN S.MALM

CHECKED

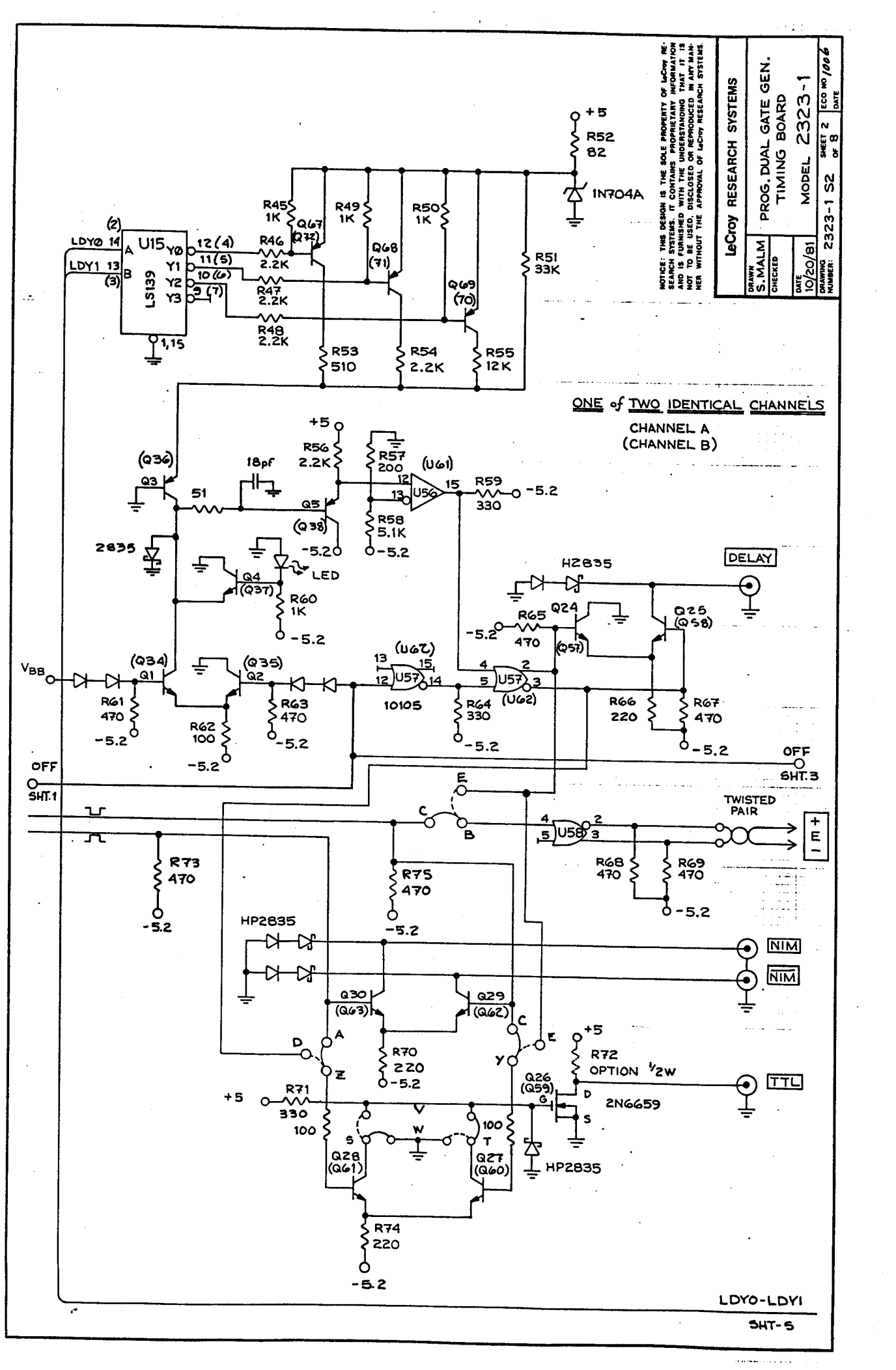
DATE 10/20/81

DRAWING NUMBER: 2323-1 S2

SHEET 1 OF 8

ECO # 1006

DATE 1.8.85


LeCroy RESEARCH SYSTEMS
PROG. DUAL GATE GEN. TIMING BOARD
MODEL 2323-1
DRAWN S.MALM
CHECKED
DATE 10/20/81
DRAWING NUMBER: 2323-1 S2
SHEET 2 OF 8
ECO NO 1006
DATE
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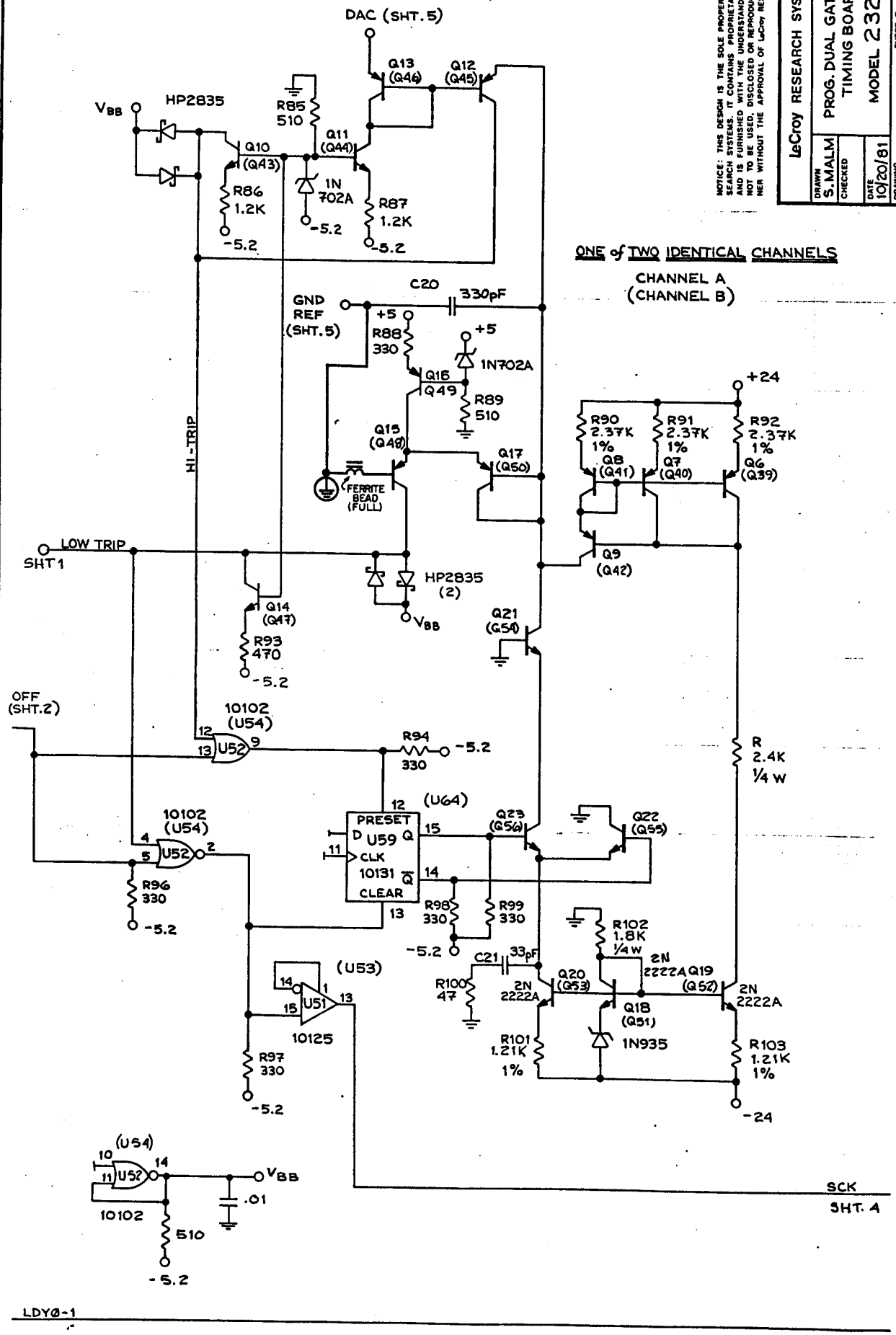
ONE of TWO IDENTICAL CHANNELS
CHANNEL A
(CHANNEL B)
LDY0 14
LDY1 13
U15
LS139
R45 1K
R46 2.2K
R47 2.2K
R48 2.2K
R49 1K
R50 1K
R51 33K
R52 82
1N704A
+5
R53 510
R54 2.2K
R55 12K
Q67 (Q72)
Q68 (Q71)
Q69 (Q70)
Q36 (Q3)
Q37 (Q4)
Q38 (Q5)
18pf
51
R56 2.2K
R57 200
R58 5.1K
R59 330
-5.2
U61 (U56)
LED
2835
R60 1K
Q34 (Q1)
Q35 (Q2)
R61 470
R62 100
R63 470
U62 (U57)
10105
R64 330
R65 470
Q24 (Q51)
Q25 (Q58)
HP2835
DELAY
R66 220
R67 470
OFF SHT.1
OFF SHT.3
VBB
TWISTED PAIR
U58
R68 470
R69 470
R73 470
R75 470
NIM
NIM
Q30 (Q63)
Q29 (Q62)
R70 220
R71 330
100
R72 OPTION 1/2W
TTL
Q26 (Q59)
2N6659
Q28 (Q61)
Q27 (Q60)
R74 220
LDY0-LDY1
SHT-5


DAC (SHT. 5)
Q13 (Q46)
Q12 (Q45)
R85 510
Q11 (Q44)
Q10 (Q43)
HP2835
V_{BB}
R86 1.2K
1N 702A
R87 1.2K
-5.2
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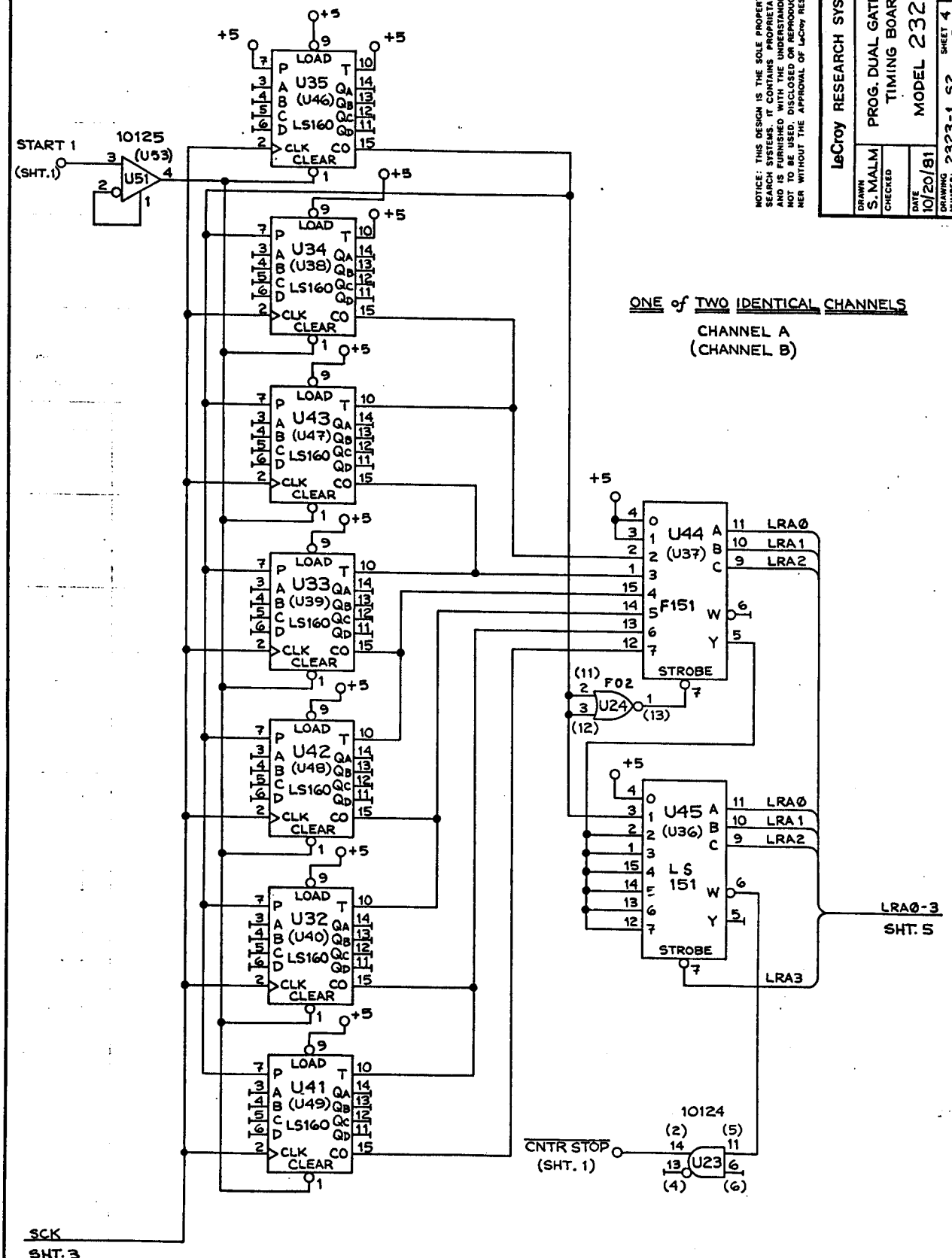
LeCroy RESEARCH SYSTEMS
PROG. DUAL GATE GEN. TIMING BOARD
MODEL 2323-1
DRAWN S.MALM
CHECKED
DATE 10/20/81
DRAWING NUMBER: 2323-1 S2
SHEET 3 OF 8
ECO NO 1006
DATE
ONE of TWO IDENTICAL CHANNELS
CHANNEL A
(CHANNEL B)
C20 330pF
GND REF (SHT. 5)
+5
R88 330
1N702A
Q16 Q49
R89 510
Q15 (Q48)
Q17 (Q50)
FERRITE BEAD (FULL)
HI-TRIP
+24
R90 2.37K 1%
R91 2.37K 1%
R92 2.37K 1%
Q8 (Q41)
Q7 (Q40)
Q6 (Q39)
Q9 (Q42)
LOW TRIP SHT 1
HP2835 (2)
Q14 (Q47)
R93 470
Q21 (Q54)
OFF (SHT. 2)
10102 (U54)
U52
R94 330
R 2.4K ¼ W
(U64)
PRESET
D U59 Q
CLK
10131
CLEAR
Q23 (Q56)
Q22 (Q55)
R96 330
R98 330
R99 330
R102 1.8K ¼W
C21 33pF
2N 2222A
Q20 (Q53)
Q19 (Q52)
Q18 (Q51)
R100 47
R101 1.21K 1%
1N935
R103 1.21K 1%
-24
(U53)
U51
10125
R97 330
(U54)
U52
10102
.01
510
SCK SHT. 4
LDY0-1


LeCroy RESEARCH SYSTEMS
PROG. DUAL GATE GEN.
TIMING BOARD
MODEL 2323-1
DRAWN S.MALM
CHECKED
DATE 10/20/81
DRAWING NUMBER: 2323-1 S2
SHEET 4 OF 8
ECO NO 1006
DATE
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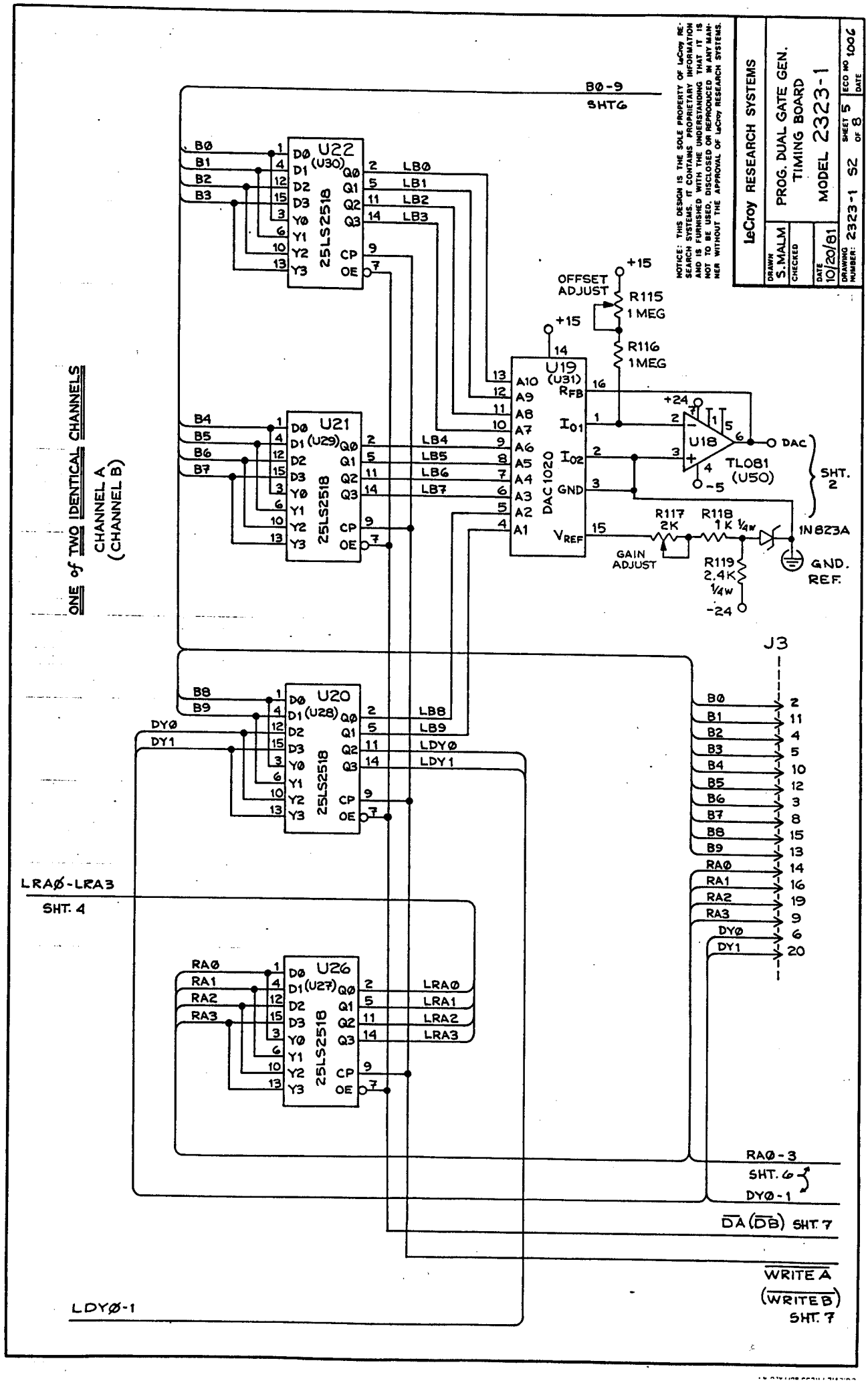
ONE of TWO IDENTICAL CHANNELS
CHANNEL A
(CHANNEL B)
START 1
(SHT. 1)
10125
(U53)
U51
U35 (U46) LS160
U34 (U38) LS160
U43 (U47) LS160
U33 (U39) LS160
U42 (U48) LS160
U32 (U40) LS160
U41 (U49) LS160
LOAD
CLK
CLEAR
U44 (U37) F151
U45 (U36) LS 151
STROBE
F02
U24
LRA0
LRA1
LRA2
LRA3
LRA0-3
SHT. 5
10124
U23
CNTR STOP
(SHT. 1)
SCK
SHT. 3
LDY0-1


LeCroy RESEARCH SYSTEMS
PROG. DUAL GATE GEN.
TIMING BOARD
MODEL 2323-1
DRAWN S.MALM
CHECKED
DATE 10/20/81
DRAWING NUMBER: 2323-1 S2
SHEET 5 OF 8
ECO NO 1006
DATE
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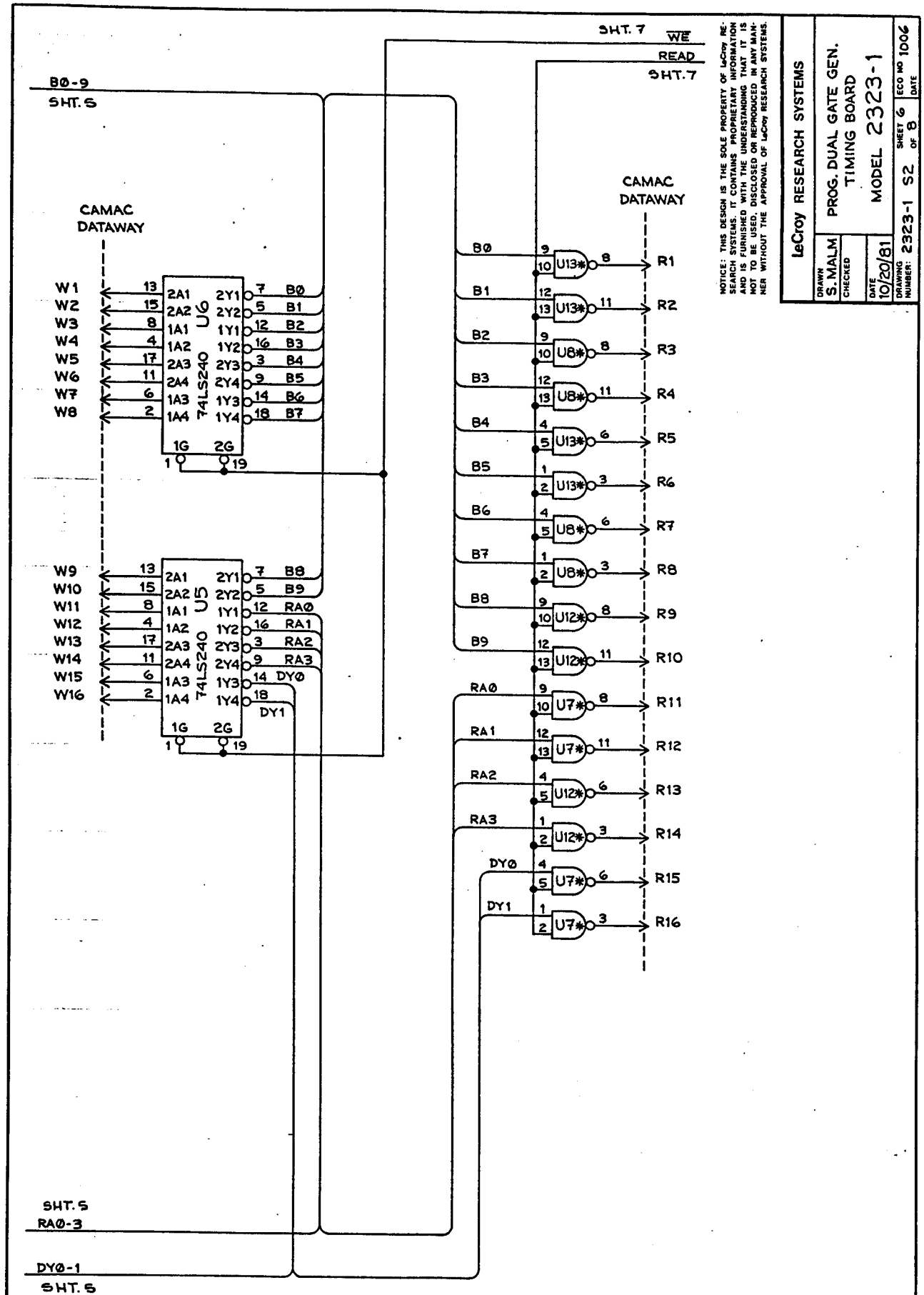
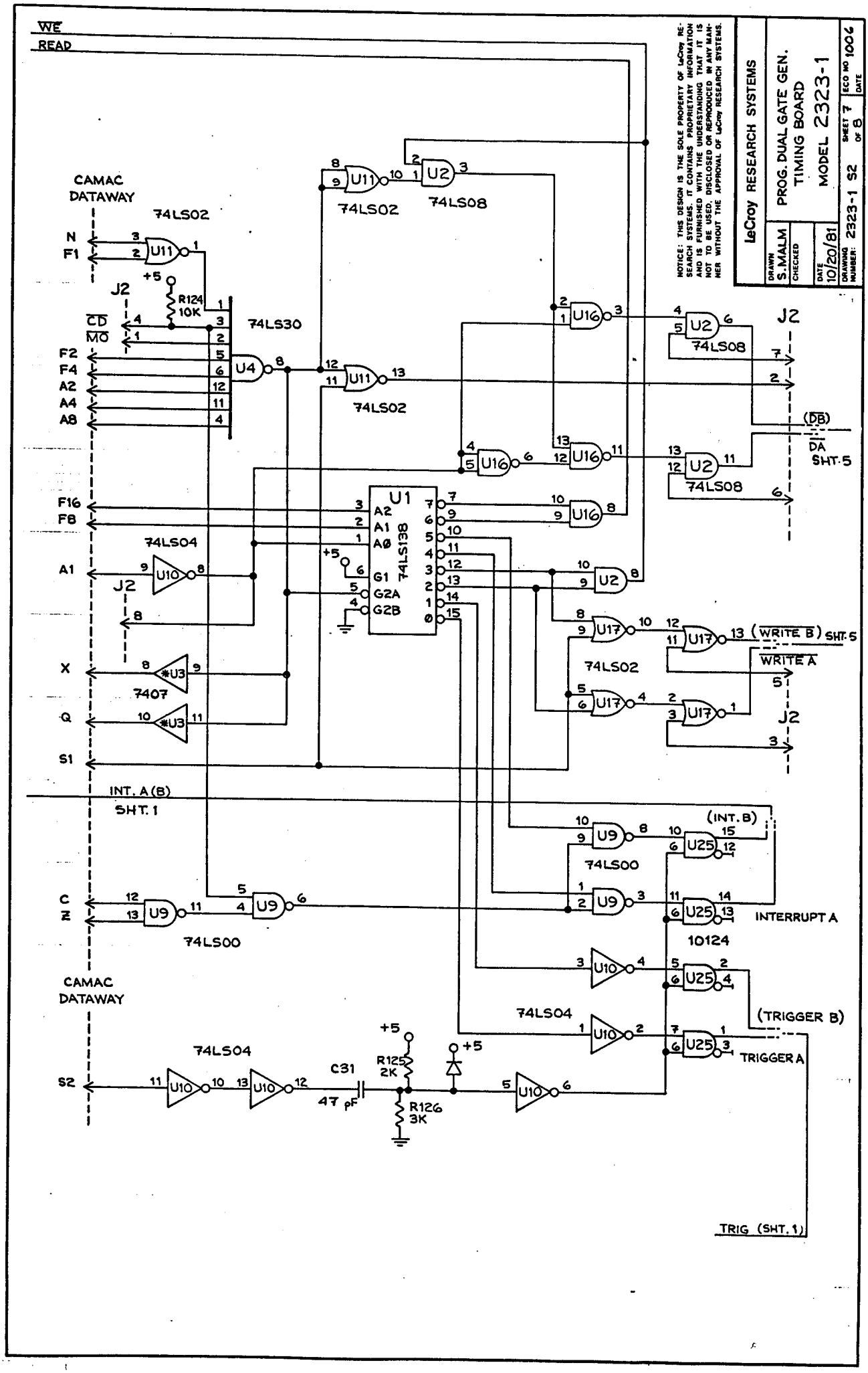
ONE of TWO IDENTICAL CHANNELS
CHANNEL A
(CHANNEL B)
B0-9
SHT 6
U22 (U30)
U21 (U29)
U20 (U28)
U26 (U27)
25LS2518
B0
B1
B2
B3
B4
B5
B6
B7
B8
B9
DY0
DY1
RA0
RA1
RA2
RA3
LB0
LB1
LB2
LB3
LB4
LB5
LB6
LB7
LB8
LB9
LDY0
LDY1
LRA0
LRA1
LRA2
LRA3
LRA0-LRA3
SHT. 4
LDY0-1
U19 (U31)
DAC 1020
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
RFB
IO1
IO2
GND
VREF
+15
OFFSET ADJUST
R115
1 MEG
R116
1 MEG
U18
TL081
(U50)
+24
-5
DAC
SHT. 2
R117
2K
GAIN ADJUST
R118
1 K 1/4W
1N823A
GND. REF.
R119
2.4K
1/4W
-24
J3
RA0-3
SHT. 6
DY0-1
DA (DB) SHT 7
WRITE A
(WRITE B)
SHT. 7



LeCroy RESEARCH SYSTEMS

PROG. DUAL GATE GEN.
TIMING BOARD
MODEL 2323-1

DRAWN: S. MALM
CHECKED:
DATE: 10/20/81
DRAWING NUMBER: 2323-1 S2
SHEET 6 OF 8
ECO NO 1006
DATE


WE
READ
CAMAC DATAWAY
74LS02
74LS08
74LS30
74LS04
74LS00
74LS138
7407
N
F1
J2
+5
R124 10K
CD
MD
F2
F4
A2
A4
A8
F16
F8
A1
X
Q
S1
INT. A (B) SHT. 1
C
Z
S2
U1
A2
A1
A0
G1
G2A
G2B
*U3
C31
47 pF
R125 2K
R126 3K
(DB)
DA
SHT. 5
(WRITE B) SHT. 5
WRITE A
(INT. B)
INTERRUPT A
10124
(TRIGGER B)
TRIGGER A
TRIG (SHT. 1)
LeCroy RESEARCH SYSTEMS
PROG. DUAL GATE GEN. TIMING BOARD
MODEL 2323-1
DRAWN S.MALM
CHECKED
DATE 10/20/81
DRAWING NUMBER: 2323-1 S2
SHEET 7 OF 8
ECO NO 1006
DATE
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DEVICE	DESIGNATION	+24	+15	+5	GND	-5	-24
10102	U52,54				1,16	8	
10105	U57,58,62,63				1,16	8	
10115	U56,61				1,16	8	
10124	U23,25			9	16	8	
10125	U51,53			9	16	8	
10131	U59,64				1,16	8	
25LS2518	U20,21,22,26,27,28,29,30			16	8		
74LS00	U9			14	7		
74LS02	U11,17,24			14	7		
74LS04	U10,16			14	7		
7407	U3			14	7		
74LS08	U2			14	7		
74LS30	U4			14	7		
74LS38	U7,8,12,13			14	7		
74LS138	U1			16	8		
74LS151	U36,37,44,45			16	8		
74LS160	U35,32,33,34,38,39,40,41,42,43,46,47,48,49			16	8		
74LS240	U5,6			20	10		
AM685	U55,60			2	1,16	8	
DAC1020	U19,31		14		3		
LM339	U14				3	12	
TL081	U18,50	7				4	
74LS139	U15			16	8		

LeCroy RESEARCH SYSTEMS

PROG. DUAL GATE GEN.
TIMING BOARD
MODEL 2323-1

DRAWN S.MALM
CHECKED
DATE 3/30/81
DRAWING NUMBER: 2323-1 S1
SHEET 8 OF 8
ECO NO 1006
DATE

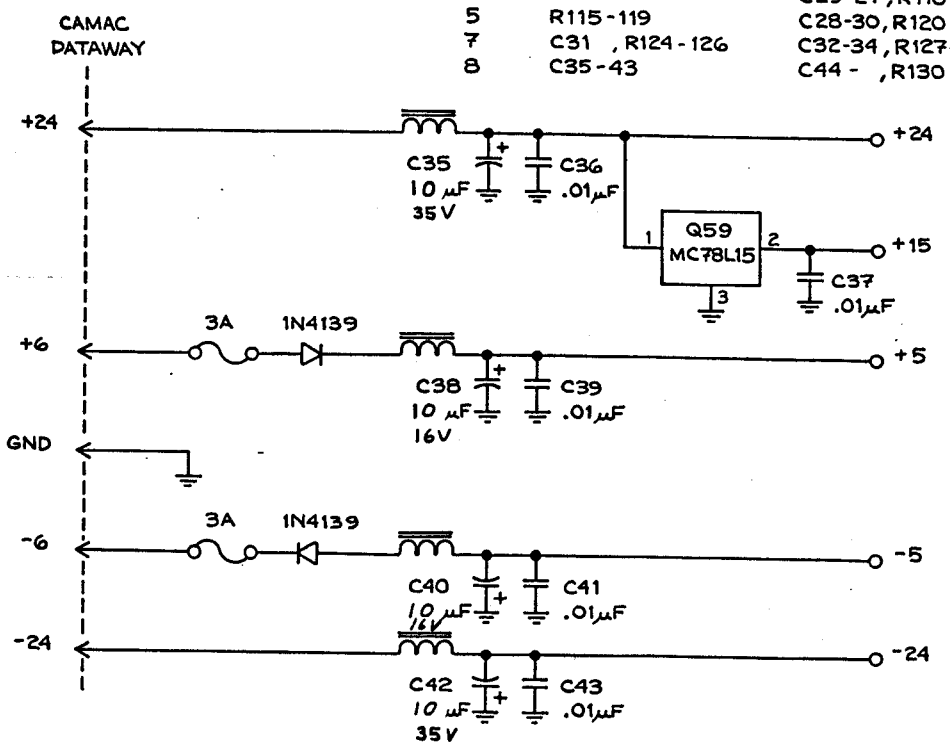
J2

-5.2 — 9, 10
+5 — 17, 18
GND. — 19, 20

NOTES:
1) ALL UNMARKED DIODES ARE 1N4448
2) * DENOTES OPEN-COLLECTOR OUTPUTS
3) ALL RESISTORS ARE 1/8W, 5% UNLESS OTHERWISE SPECIFIED.
4) REFERENCE DESIGNATIONS:

5) ALL NPN'S ARE 2N5770,
ALL PNP'S ARE 2N5771, UNLESS
OTHERWISE SPECIFIED.

SHT. #	USED:	OMITTED:
1	C1-12, R1-38	C13-16, R39-44
2	, R45-75	C17-19 R76-84
3	C20-21, R85-103	C22-24, R104-109
4		C25-27, R110-114
5	R115-119	C28-30, R120-123
7	C31, R124-126	C32-34, R127-129
8	C35-43	C44-, R130-



MODEL NO 2323-5 MECH SUBASSY 2323 PRINTED 29-Apr-85
ECON 1002 REV DATE 17-Feb-82
MCN 4 MCN DATE 08-Dec-83
FAN HIST. NO 2002 FAN HIST. DATE

LRS	PART NO	DESCRIPTION			QTY
521	**0 **4	SPACER HEX	2-56X.417	STEEL 3/16 HEX/DO NOT SUBSTITUTE	4
521	400 **4	SPACER ROUND #4	1/8		4
521	440 *20	SPACER HEX	4-40X5/8		4
524	440 **6	SPACER MALE/FEM	9/16 LG	5/16 STUD STAINLESS STEEL 3/16 HEX	4
540	203 **1	SIDE COVER CAMAC STD(LIP)			1
540	206 *78	RAIL CAMAC STD TOP W/LIP		FLANGE REMOVED 1.5" & 2.5" AT ENDS	1
540	206 178	RAIL CAMAC STD BOT W/LIP		FLANGE REMOVED 1.5" & 2.5" AT ENDS	1
540	209 *22	REAR PANEL CAMAC SIZE #2		NO CUTOUT/2 SLOTS	1
555	430 **3	CAPTIVE SCREW ASSEMBLY		MOD: KNOB .500 LONG	1
560	256 **5	SCREW PHILIPS	2-56X5/16		4
568	256 **2	SCREW FLAT PHIL	2-56X1/8		4
575	470 **5	WASHER FLAT SIZE #4 NYLON		9/32 OD 3/64 THK	8
722	323 **3	FRONT PNL PREASS'Y	2323	540202502(1) PER DWG 2323-M1	1
732	323 **3	SIDE CAMAC LEFT	2323	540203245(1)	1
753	512 **3	SPECIAL MOD FP LENS	3512	390412030(0)	1

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MODEL NO 2323-3 PROG DUAL GATE GEN PRINTED 29-Apr-85
ECON 1000 REV DATE 25-Sep-81
MCN 0 MCN DATE 00-XXX-00
FAN HIST. NO 2000 FAN HIST. DATE

LRS	PART NO	DESCRIPTION	QTY
256	233 209	DIODE LED (RED) TIL209A	10
257	253 414	DISPLAY LED RED 7-SEGMENT 4-DIGIT W/RIGHT DECIMAL POINT	1
405	812 **3	SOCKET STRIP WW 20 POS	1
408	*30 103	WIREWRAP PIN .025 SQUARE	12
521	440 *11	SPACER HEX 4-40X11/32	3
712	323 *33	PC BD PREASS'Y 2323-3	1

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454 710 *20 HDR DIP SOLD TO MALE    20 .100 CTRS/RT ANGLE/NO EARS/.110-.318     2
454 712 **2 HDR DIP SOLD TO MALE     2 .100 CTRS/RT ANGLE/NO EARS/.110-.318     2
500 120 **2 TRANSIPAD          "LARGE"                                          3
712 323 *13 PC BD PREASS'Y      2323-1 MULTI-LAYER                              1
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MODEL NO 2323-1 PROG DUAL GATE GEN PRINTED 29-Apr-85
ECON 1006 REV DATE 08-Jan-85
MCN 5 MCN DATE 10-Jan-85
FAN HIST. NO 2006 FAN HIST. DATE

LRS PART NO DESCRIPTION QTY

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MODEL NO 2323-2 PROG DUAL GATE GEN PRINTED 29-Apr-85
ECON 1003 REV DATE 02-Aug-84
MCN 2 MCN DATE 02-Aug-84
FAN HIST. NO 2005 FAN HIST. DATE

LRS	PART NO	DESCRIPTION			QTY
102	245 103	CAP CERA DISC 25V .01 UF	PT-FDCL-1/32 LEADS 3/8 AWG 22		22
102	444 101	CAP CERA DISC 100V 100 PF	10% S3N		2
102	745 102	CAP CERA DISC 500 .001 UF	PT-FDCL-1/32 LEADS 3/8 AWG 22	#	2
116	515 101	CAP DIP MICA DM10 100 PF			2
116	515 750	CAP DIP MICA DM10 75 PF			2
125	545 203	CAP POLYCARB FILM .02 UF	50V 5%		1
161	225 102	RES CARBON FILM 1 K	1/8W 5%		5
161	225 103	RES CARBON FILM 10 K	1/8W 5%		9
161	225 104	RES CARBON FILM 100 K	1/8W 5%		2
161	225 105	RES CARBON FILM 1 MEG	1/8W 5%		2
161	225 201	RES CARBON FILM 200 OHMS	1/8W 5%		2
161	225 222	RES CARBON FILM 2.2 K	1/8W 5%		2
161	225 331	RES CARBON FILM 330 OHMS	1/8W 5%		10
161	225 332	RES COMP 1/8W 5% 3.3 K	1/8W 5%		1
161	225 473	RES CARBON FILM 47 K	1/8W 5%		2
161	225 681	RES CARBON FILM 680 OHMS	1/8W 5%		2
182	537 103	RES VARI CERMET 10 K	3/4W 10%		2
190	842 102	RES NETWORK 1 K	SIP-8		1
190	842 103	RESISTOR NETWORK 10 K	SIP-8		5
200	*31 *28	IC 2-INPUT NAND SN74LS00N	DIP-14	74LS00	1
200	*31 *32	IC HEX BUFF/DRIV SN7407N	DIP-14/HI-VOLT/OPEN COLL	7407	1
200	*31 *46	IC HEX INVERTER SN74LS04N	DIP-14	74LS04	1
200	*31 *49	IC D-TYP FLOP SN74LS74N	DIP-14/DUAL PKG/EDG-TRIG	74LS74	1
200	*31 *51	IC 2-INPUT NOR SN74LS02N	DIP-14/QUAD PKG	74LS02	1
200	*31 *73	IC 2-IN POS OR SN74LS32N	DIP-14/QUAD PKG	74LS32	1
200	*31 *75	IC 2-INPUT NAND SN74LS03N	DIP-14/QUAD PKG/OPEN COLL	74LS03	1
200	*31 *86	IC 2-INPUT AND SN74LS08N	DIP-14/QUAD PKG	74LS08	1
200	*41 *26	IC 4-BIT CTR SN74LS161N	DIP-16	74LS161	3
200	*41 *42	IC UP/DN COUNT SN74LS191N	DIP-16	74LS191	4*
200	*41 *62	IC DEC/DEMULTP SN74LS138N	DIP-16	74LS138	1
200	*41 185	IC BINARY-TO-BCD SN74185A	DIP-16	74185	6
200	*41 190	IC UP/DN COUNT SN74LS190N	DIP-16	74LS190	1
200	*71 **7	IC BUFFER SN74LS244N	DIP-20/OCTAL PKG/3-STATE	74LS244	4
200	*81 **7	IC MULTIPLEXER SN74LS151	DIP-16	74LS151	1
200	141 *48	IC DECODER/DRIVR SN74LS48	DIP-16/BCD-TO-7-SEGM	74LS48	1
208	*11 **4	IC TIMER NE555	DIP-8	555	1
208	*31 *10	IC QUAD DIFF COMP LM339N	DIP-14	339	1
227	573 470	IC PROM DSPY2323	227571470(1) -PROGRAMMED-	28LA22	1
230	110 **5	DIODE SWITCHING 1N4448			1
240	225 704	DIODE ZENER 4.1V 1N704A	250MW		2
253	*10 835	DIODE HOT CARRIER HP2835	H-P CASE 15		1
400	*10 **8	SOCKET IC ST DIP-8	.300 SEP/.160" PINS/NO INLAY		1
400	*20 *14	SOCKET IC ST DIP-14	.300 SEP/.160" PINS/NO INLAY		9
400	*30 *16	SOCKET IC ST DIP-16	.300 SEP/.160" PINS/NO INLAY		17
400	170 *20	SOCKET IC ST DIP-20	.300 SEP/.160" PINS/NO INLAY		5
403	111 *26	HEADER ASSEMBLY 26-PIN			1
409	132 101	SWITCH TOGGLE PC MTG SPDT	ON-NONE-ON/LOCKING/RT ANGLE		3

MODEL NO 2323-2 PROG DUAL GATE GEN PRINTED 29-Apr-85
ECON 1003 REV DATE 02-Aug-84
MCN 2 MCN DATE 02-Aug-84
FAN HIST. NO 2005 FAN HIST. DATE

LRS	PART NO	DESCRIPTION	QTY
409	152 300	SWITCH TOGGLE PC MTG SPDT MOM-OFF-MOM/RT ANGLE/STD TOGGLE/UNTH	1
416	132 **8	SWITCH PUSHBUT (MOM) SPDT RT ANGLE/PC TERM/NON-THRD/SM BLK CAP	4
454	710 *20	HDR DIP SOLD TO MALE 20 .100 CTRS/RT ANGLE/NO EARS/.110-.318	2
468	622 **2	TEST POINT (JACK) BLU SIMILAR TO MIL-C-39024/11A	2
712	323 *23	PC BD PREASS'Y 2323-2	1

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MODEL NO 2323-1 PROG DUAL GATE GEN PRINTED 29-Apr-85
ECON 1006 REV DATE 08-Jan-85
MCN 5 MCN DATE 10-Jan-85
FAN HIST. NO 2006 FAN HIST. DATE

LRS	PART NO	DESCRIPTION			QTY
200	*41 *62	IC DEC/DEMULTP SN74LS138N	DIP-16	74LS138	1
200	*41 *73	IC 4-BIT CNTR SN74LS160N	DIP-16/SYNCH/DIRECT CLR	74LS160	14
200	*41 139	IC DEC/MULTIPL SN74LS139N	DIP-16/DUAL PKG/2-TO-4LINE	74LS139	1
200	*41 518	IC 4-BIT REG 25LS2518PC	DIP-16/QUAD PKG	25LS2518	8
200	*71 **1	IC 8 X BUFFER SN74LS240	DIP-20/3-STATE OUTPUTS	74LS240	2
200	*81 **7	IC MULTIPLEXER SN74LS151	DIP-16	74LS151	2
200	330 **2	IC 2-IN NOR GATE 74F02	DIP-14/QUAD PKG	74F02	1
204	*42 **2	IC NOR GATE MC10102P	DIP-16/QUAD PKG	10102	2
204	*42 **3	IC LINE RECEIVER MC10115P	DIP-16/QUAD PKG	10115	2
204	*42 **4	IC 2-3-2-IN GATE MC10105P	DIP-16***DO NOT SUB***	10105	4
204	*42 **5	IC TYP D FL-FL MC10131P	DIP-16/DUAL PKG	10131	2
204	*42 **7	IC QUAD TRANSL MC10124P	DIP-16/MTTL-TO-MECL	10124	2
204	*42 **8	IC QUAD TRANSL MC10125P	DIP-16	10125	2
207	340 151	IC FAST 8-IN MPX 74F151	DIP-16	74F151	2
208	*11 *12	IC OP AMP TL081CP	DIP-8/J-FET INPUT	081	2
208	*31 *10	IC QUAD DIFF COMP LM339N	DIP-14	339	1
208	*44 **1	IC VOLT COMPARATOR AM685	DIP-16	685	2
208	141 *20	IC 10-BIT BINARY DAC 1020	DIP-16	1020	2
208	164 **2	IC VOLT REG POS MC78L15CG	TO-39/+15V	78L15	1
230	110 **5	DIODE SWITCHING 1N4448			29
235	*50 **1	DIODE RECTIFIER 1N4139			2
240	225 702	DIODE ZENER 2.6V 1N702A	250MW		4
240	225 704	DIODE ZENER 4.1V 1N704A	250MW		2
240	405 823	DIODE ZENER 6.2V 1N823A	400 MW/TEMP COMPENSATED/DO-7 CASE		2
240	525 935	DIODE ZENER 9.0V 1N935	500MW DO-7 CASE		2
253	*10 835	DIODE HOT CARRIER HP2835	H-P CASE 15		24
256	233 209	DIODE LED (RED) TIL209A			2
256	270 405	DIODE LED (MTG BLOCK) RED	CORNER AT CATHODE BEVELED		2
270	110 **3	TRANSISTOR NPN 2N2222A	TO-18		6
270	170 **1	TRANSISTOR NPN 2N5770	TO-92		36
275	170 **2	TRANSISTOR PNP 2N5771	TO-92		30
280	130 **2	TRANSISTOR FET "N" 2N6659	TO-39		2
300	*10 **1	BEAD SHIELDING FERRITE			2
300	*50 **1	CHOKE FERRITE SINGLE LEAD			4
400	*10 **8	SOCKET IC ST DIP-8	.300 SEP/.160" PINS/NO INLAY		2
400	*20 *14	SOCKET IC ST DIP-14	.300 SEP/.160" PINS/NO INLAY		14
400	*30 *16	SOCKET IC ST DIP-16	.300 SEP/.160" PINS/NO INLAY		46
400	170 *20	SOCKET IC ST DIP-20	.300 SEP/.160" PINS/NO INLAY		2
402	112 **1	CONN PC MTG LEMO NICKEL			18
408	*63 **5	W-W PIN, ONE SIDE, 1 WRAP	.025 SQUARE		22
433	220 **2	FUSE PICO II 125V 3 AMP			2
454	170 **2	NOW USE 454 370 002			10

MODEL NO 2323-1 PROG DUAL GATE GEN PRINTED 29-Apr-85
ECON 1006 REV DATE 08-Jan-85
MCN 5 MCN DATE 10-Jan-85
FAN HIST. NO 2006 FAN HIST. DATE

LRS PART NO	DESCRIPTION		QTY
102 245 103	CAP CERA DISC 25V .01 UF PT-FDCL-1/32 LEADS 3/8 AWG 22		54
102 745 102	CAP CERA DISC 500 .001 UF PT-FDCL-1/32 LEADS 3/8 AWG 22	#	3
116 515 101	CAP DIP MICA DM10 100 PF		6
116 515 180	CAP DIP MICA DM10 18 PF		2
116 515 330	CAP DIP MICA DM10 33 PF		2
116 515 331	CAP DIP MICA DM10 330 PF		2
116 515 390	CAP DIP MICA DM10 39 PF		2
116 515 470	CAP DIP MICA DM10 47 PF		1
146 424 106	CAP MINI ALUM 20% 10 UF 16V/RADIAL LEADS/.06 CTRS/.157X.295		2
146 634 106	CAP MINI ALUM 20% 10 UF 35V/RADIAL LEADS/.10 CTRS/.248X.295		2
158 849 **6	CAP VARIABLE 7-45 PF YELLOW CASE .189 HI .236 DIA		2
161 225 101	RES CARBON FILM 100 OHMS 1/8W 5%		12
161 225 102	RES CARBON FILM 1 K 1/8W 5%		18
161 225 103	RES CARBON FILM 10 K 1/8W 5%		8
161 225 105	RES CARBON FILM 1 MEG 1/8W 5%		6
161 225 122	RES CARBON FILM 1.2 K 1/8W 5%		4
161 225 123	RES CARBON FILM 12 K 1/8W 5%		2
161 225 201	RES CARBON FILM 200 OHMS 1/8W 5%		2
161 225 202	RES CARBON FILM 2 K 1/8W 5%		1
161 225 221	RES CARBON FILM 220 OHMS 1/8W 5%		10
161 225 222	RES CARBON FILM 2.2 K 1/8W 5%		12
161 225 223	RES CARBON FILM 22 K 1/8W 5%		1
161 225 302	RES CARBON FILM 3 K 1/8W 5%		1
161 225 331	RES CARBON FILM 330 OHMS 1/8W 5%		34
161 225 333	RES CARBON FILM 33 K 1/8W 5%		2
161 225 470	RES CARBON FILM 47 OHMS 1/8W 5%		2
161 225 471	RES CARBON FILM 470 OHMS 1/8W 5%		18
161 225 510	RES CARBON FILM 51 OHMS 1/8W 5%		8
161 225 511	RES CARBON FILM 510 OHMS 1/8W 5%		8
161 225 512	RES CARBON FILM 5.1 K 1/8W 5%		2
161 225 681	RES CARBON FILM 680 OHMS 1/8W 5%		6
161 225 750	RES CARBON FILM 75 OHMS 1/8W 5%		2
161 225 820	RES CARBON FILM 82 OHMS 1/8W 5%		2
161 335 102	RES CARBON FILM 1 K 1/4W 5%		2
161 335 182	RES COMP 1/4W 5% 1.8 K 1/4W 5%		2
161 335 242	RES CARBON FILM 2.4 K 1/4W 5%		4
168 531 401	RES PREC RN55D 1.21 K		4
168 531 429	RES PREC RN55D 2.37 K		6
181 457 105	RES VARI CERMET 1 MEG 1/2W 10%		2
181 457 202	RES VARI CERMET 2 K 1/2W 10%		2
200 *31 *28	IC 2-INPUT NAND SN74LS00N DIP-14	74LS00	2
200 *31 *32	IC HEX BUFF/DRIV SN7407N DIP-14/HI-VOLT/OPEN COLL	7407	1
200 *31 *46	IC HEX INVERTER SN74LS04N DIP-14	74LS04	1
200 *31 *51	IC 2-INPUT NOR SN74LS02N DIP-14/QUAD PKG	74LS02	2
200 *31 *52	IC 8-INPUT NAND SN74LS30N DIP-14/SINGLE PKG	74LS30	1
200 *31 *86	IC 2-INPUT AND SN74LS08N DIP-14/QUAD PKG	74LS08	1
200 *32 *10	IC 2-INPUT NAND 74LS38PC DIP-14/QUAD PKG/OPEN COLL	74LS38	4

MODEL NO 2323
ECON 2006
MCN 4

PROG DUAL GATE GEN

PRINTED 29-Apr-85
REV DATE 08-Jan-85
MCN DATE 10-Jan-85

LRS	PART NO	DESCRIPTION		QTY
802	323 **1	SUBASS'Y CABLE	20-PIN	PL:2323-4H1 1
802	323 **2	SUBASS'Y CABLE	20-PIN	PL:2323-4H2 1
812	323 *11	PC BD SUBASS'Y	2323-1	PL:2323-1 1
812	323 *21	PC BD SUBASS'Y	2323-2	PL:2323-2 1
812	323 *31	PC BD SUBASS'Y	2323-3	PL:2323-3 1
842	323 *53	MECH SUBASS'Y	2323-5	PL:2323-5 1

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