

LeCroy
RESEARCH SYSTEMS

LRB
2341A
16 FOLD
REGISTER

CAMAC Model 2341A 16-Channel Coincidence Register

NEW!
**Inputs respond
to signals as low as
-100 mV!**

- **16 channels in single-width module** . . . less space than that required by other designs.
- **Summing outputs** provide fast trigger capability . . . organized in two groups of eight registers for use in multiplicity decisions.
- **Fast clear input** . . . permits use of loose pretrigger (so summing output can participate in final logic decision) without deadtime generating dataway clearing operation.
- **Narrow coincidence widths** . . . High speed design permits coincidence width as narrow as 1 nsec.
- **Input double-pulse resolution <10 nsec** . . . assures high efficiency even in high count rate applications.
- **Accepts input amplitudes as low as -100 mV** . . . permits triggering even after substantial attenuation from long cable delays.

The LeCroy Model 2341A Coincidence Register ("pattern unit") offers fast storage functions in computer-compatible CAMAC standard packaging. The integrated circuit design affords high density packaging, permitting 16 complete channels in one CAMAC single-width module.

The 2341A operates from standard NIM logic levels. The logic channels, which seek a coincidence between each input and a common fast gate input, employ MECL III integrated circuits and provide coincidence resolving times under 2 nsec. Logical "1" data levels, representing the time coincidence between the common gate and the 16 inputs, are stored in a 16-bit fast buffer register for later readout under CAMAC commands. The facility of performing majority logic is provided by two rear-panel summing outputs which are each driven by 8 logic channels. The output current of the summing circuit is proportional, in increments of 4 mA per register bit, to the number of coincidences stored in the register. Bridged high impedance outputs permit cascading any number of summing outputs. Other operating features include a front-panel clear input which responds to negative logic levels and a built-in test mode.

The Model 2341A Coincidence Register is a member of LeCroy's CAMAC Series, a growing line of instruments which combine high performance with the flexibility and computer compatibility of the CAMAC standard.

November 1977

Innovators in Instrumentation

GENERAL DESCRIPTION

The LeCroy Model 2341S Coincidence Register ("pattern unit") offers fast storage functions in computer-compatible CAMAC standard packaging. The integrated circuit design affords the highest density packaging, permitting 16 complete channels in one CAMAC single-width module without exceeding CAMAC power limits.

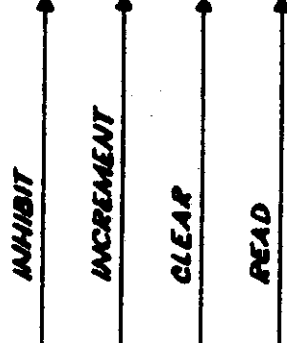
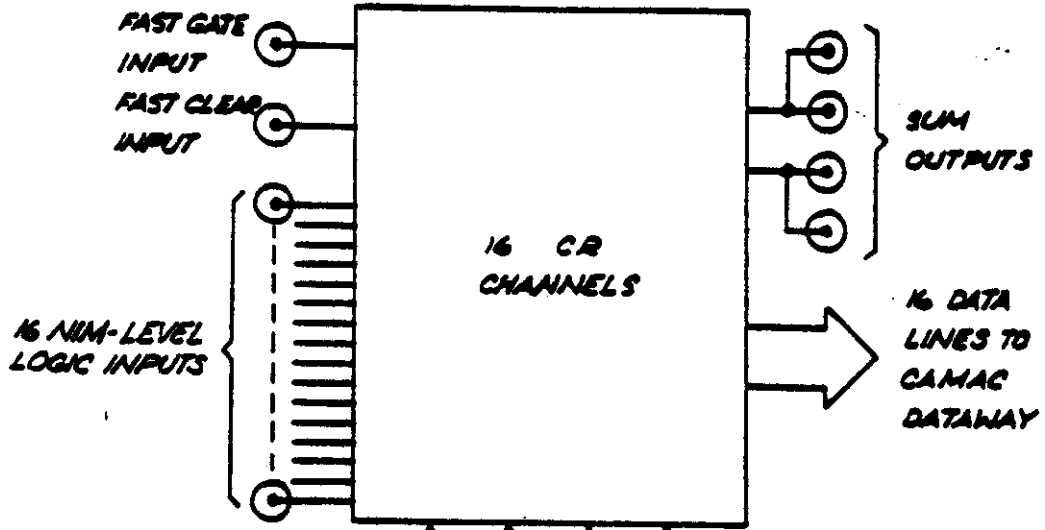
The 2341S operates from standard NIM logic levels. The logic channels, which seek a coincidence between each input and a common fast gate input, employ MECL III integrated circuits and provide coincidence resolving times under 2 ns. They represent the state-of-the-art in coincidence logic design and performance. The time coincidence between the common gate input and the 16 inputs are stored in a 16 bit fast buffer register for later readout under CAMAC commands. The facility for performing majority logic is provided by two rear-panel summing outputs which are each driven by 8 logic channels. The output current of the summing circuit is proportional, in increments of 4 mA per register bit, to the number of coincidences stored in the register. Bridged high impedance outputs permit cascading any number of summing outputs.

The Model 2341S Coincidence Register is a member of LeCroy's CAMAC Series, a growing line of instruments which combine high performance with the flexibility and computer compatibility of the CAMAC standard.

GENERAL

- Coincidence Width:** 1 ns up, determined by input and gate pulse durations.
- CAMAC Commands:**
Z or C: Clears register, requires S_2 .
Q: A Q=1 response is generated in recognition of valid "read" (F0 or F2). An optional jumper allows both F25 and F9 to generate Q for a valid "N" and "A0".
I: Gate Input is inhibited for duration of CAMAC inhibit command.
- CAMAC Function Codes:**
F0: Read group 1 register; requires "N" and "A0".
F2: Read and Clear group 1 register; requires "N", "A0", and " S_2 ".
F9: Clear Group 1 register; requires "N", "A0" and " S_2 ".
F25: Increment (test mode latches all channels); requires "N" and " S_2 ".
- Packaging:** CAMAC single-width module. Conforms to ESONE Report EUR 4100e standards.
- Power Requirements:** Less than 16 watts, ± 6 V, -24 V.

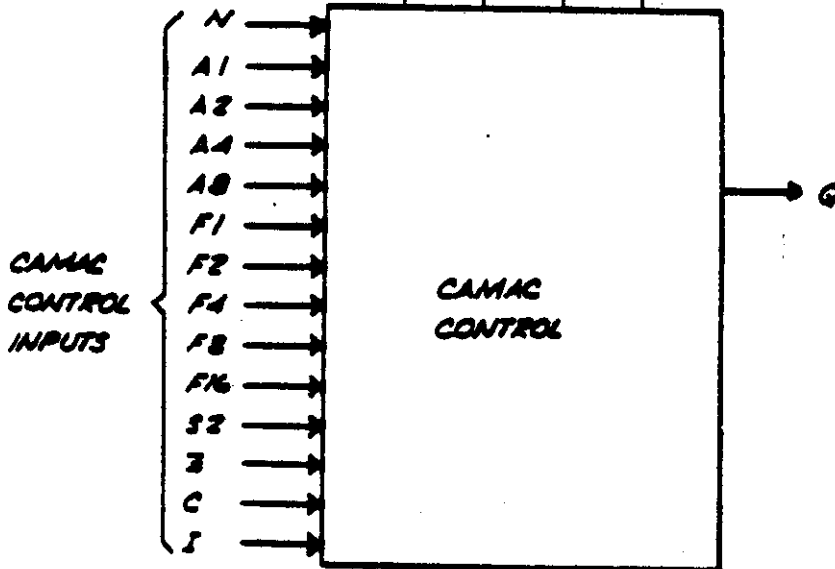
FUNCTIONAL DESCRIPTION



General Block
Diagram:

Model 2341
16-Channel

Coincidence-
Register



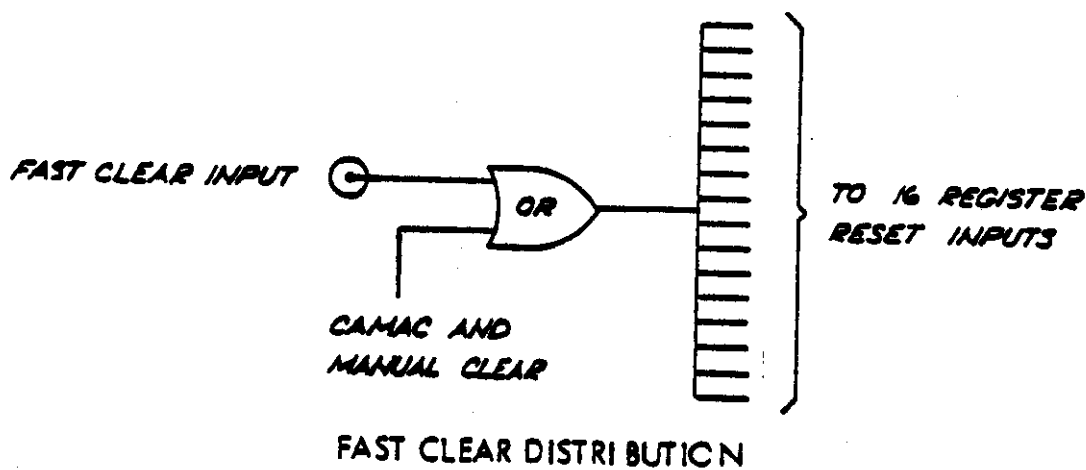
FUNCTIONAL DESCRIPTION

shifter to one input of a MECL III two-fold coincidence gate (AND gate). The other input of the coincidence gate is a pulse common to all channels. An input pulse that occurs during the common gate pulse sets a MECL II register (passing through a simple diode OR gate). The register then stores a "1" bit until it is cleared by the common clear line. The register output is delivered to a buffer circuit which provides two outputs: (1) a TTL signal for gating onto the CAMAC dataway, and (2) a 2.0 mA current level which is introduced onto a summing line for multiplicity determination. For testing purposes, the register can also be set to its "1" state by means of the CAMAC increment command.

FUNCTIONAL DESCRIPTION

CLEAR FAN-OUT

The NIM level clear signal from the front panel is buffered by means of a differential stage, and the output of the differential stage is distributed by printed wiring to the reset inputs of the 16 registers. (Refer to Block Diagram following.) The opposite base of the differential stage is driven by the clear signal from the CAMAC control section.



CIRCUIT DESCRIPTION

The signal input drives one input of the single section of a Quad MECL III AND gate, MC1662 via a direct-coupled series diode level-shifting network. The second input of the AND gate is provided by the gate fan-out.

The output of the coincidence gate is connected directly to the set input of an MC1014 register. A diode connected to this line permits a positive-going pulse from the control section to set the MC1014 in the same manner as the coincidence gate output as required for the coincidence test function (increment). The register is cleared by means of common pulse supplied from the clear circuitry which is described separately.

The Q and \bar{Q} outputs of the register drive both bases of a 4 mA differential stage. The positive-going collector of the differential stage provides a TTL level which drives one input of a readout gate whose output is connected to a CAMAC data line. The negative-going collector is tied in common with the corresponding collectors of seven other channels to provide a current sum output for multiplicity detection purposes. The sum output is linear up to approximately one volt, making possible discrimination of up to 10 levels when driving a 25 Ω load comprised of a doubly-terminated 50 Ω coax. The output impedance of the current sources is extremely high and an almost unlimited number of 8-channel sections may be connected in parallel on the same coaxial daisy-chain. The delay between the input coincidence and the leading edge of the current sum output is approximately 15 ns.

CIRCUIT DESCRIPTION

ground. A measure of over-voltage protection is provided by a series $51\ \Omega$ resistor and diode clamps. The base of Q4 is driven by a positive-going clear pulse from the control section. This pulse switches the differential stage, turning Q5 on and resetting the registers in the same manner as the NIM input.

CAMAC CONTROL SECTION

Function decoding of the 5 function lines is accomplished using a SN74154 4-line to 16-line decoder. All the CAMAC input lines use negative logic notation (logical "1" equals zero volts; logical "0" equals +4 volts; see CAMAC appendix at rear of manual). The logical "0" condition of F4 is always required, so it and the N line cause the SN74154 to be enabled. The four outputs generated by the SN74154 are the F0·N, F2·N, F9·N, and F25·N functions.

F0·N and F2·N are ORed together and subsequently ANDed with A0 to form the readout strobe. A0 is generated directly from the 4 NAND gate. The final strobe level out of the CAMAC control section is quiescently at zero volts, and goes to 5 volts during the time defined by $F0 \cdot N \cdot A0$ or $F2 \cdot N \cdot A0$.

F2·N and F9·N are ORed together and subsequently ANDed with A0 to form a clear command. This command and CAMAC common control lines C and Z are all ORed together and subsequently ANDed with S2 to form the final clear signal. The clear level is quiescently held at zero volts, and in this condition a 1N914 diode decouples the clear line reference from the level