

Levey

NSCL-ELECTRONIC

NIM MODEL 364AL/365AL
DUAL 4-FOLD MAJORITY
LOGIC GATE WITH VETO

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ANY APPLICATION OR USE QUESTIONS, which will enhance your use of this instrument will be happily answered by a member of the LeCroy staff. Please address your request or correspondence to:

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A T T E N T I O N

SEE POCKET IN BACK OF MANUAL FOR
SCHEMATICS, PARTS LISTS, AND ADDITIONAL
ADDENDA WITH ANY CHANGES TO MANUAL.

A T T E N T I O N

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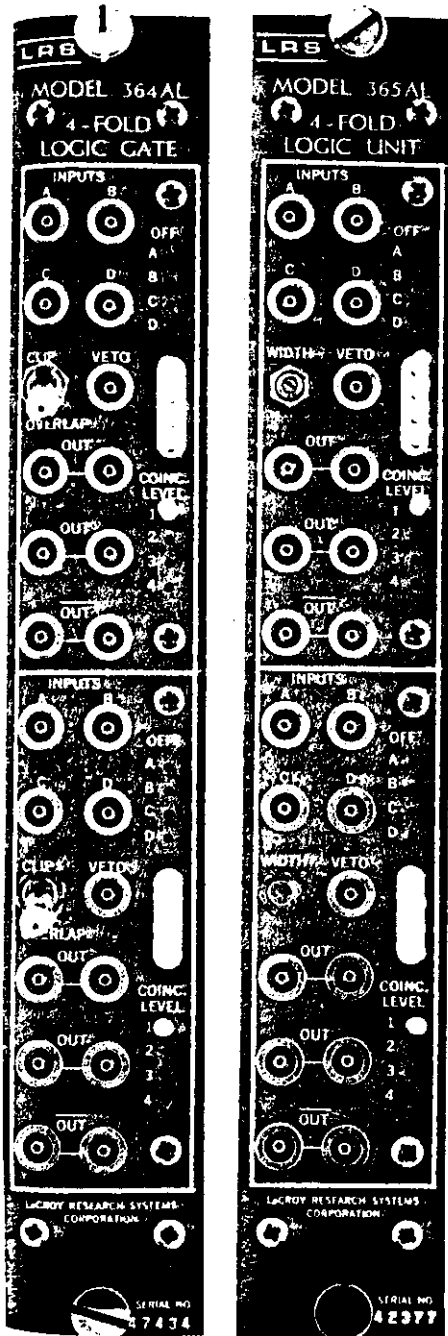
Addenda

Rear Pocket

LeCroy

NIM Models 364AL and 365AL

Dual 4-Fold Majority Logic Units with Veto



The Models 364AL and 365AL offer an unmatched combination of flexibility, compactness, and performance at a reasonable cost. Both modules provide the functions of fan-in, coincidence, inhibit, and majority logic with high fan-out capability along with 150 MHz operation. The two models differ in that the 364AL has overlap or fixed output width, and the 365AL provides an updating timing stage with front-panel width control. Each of the two identical channels accepts standard NIM logic signals at each of the four logic inputs and one veto input. Front-panel selectors allow programming of one to four simultaneous negative input signals required for an output and provide the ability to disable the separate logic inputs without removing cables. Separate veto inputs are provided for inhibiting the unit regardless of the state of the other inputs. Except in the overlap mode of the Model 364AL, the inhibit need only overlap the leading edge of the coincidence. A single output pulse is produced regardless of input amplitude or duration (no multiple pulsing). The output pulse duration of the Model 364AL is front-panel switch-selected to be either the time overlap of the input signals or to be a clipped 3.8 nsec duration. The output pulse duration of the Model 365AL may be continuously set from 3.8 nsec to 50 nsec by a multiturn front-panel potentiometer. The duration is independent of input overlap time, amplitude, and rate. Because it is updating, it may be retrigged even before the end of an output pulse that is already present. Both units provide two sets of dual (32 mA) negative outputs and one set of dual complementary outputs, each of which may be fanned out to two later inputs or be used as a means of cable clipping or reverse terminating.

March 1980

Innovators in Instrumentation

SPECIFICATIONS

NIM Models 364AL and 365AL

DUAL 4-FOLD MAJORITY LOGIC UNITS WITH VETO

INPUT CHARACTERISTICS

Logic Inputs:

4 LEMO-type connectors; 50 Ω impedance; NIM level input requirements; each input can be separately enabled or disabled.

Veto Input:

LEMO-type connector; 50 Ω impedance; NIM level input requirements. Model 364AL requires 3 ns minimum prompt leading edge overlap in fixed width position; complete overlap in overlap position. Model 365AL requires 3 ns minimum width delayed 3 ns from leading edge of input.

In Gate:

Via rear connector; clamp to ground from +4 volts inhibits; rise and fall times < 50 ns.

OUTPUT CHARACTERISTICS

Outputs:

Three; two negative (quiescently 0 mA, -32 mA during output), one positive (quiescently -32 mA, 0 mA during output).

In-Out:

6 fold, if each output drives two 50 Ω loads. (Any used output pair should drive 25 Ω for proper amplitude and shape.)

Duration:

Model 364AL: switch-selected to be either fixed 3.8 \pm 0.3 ns with inputs > 5 ns or equal to time overlap. Non-updating.
Model 365AL: continuously adjustable from less than 4 ns to greater than 50 ns by means of front-panel screwdriver-adjustable potentiometer. Updating.

Output Rise and Fall Times:

1.2 ns typical. (Fall time of 365AL is slightly longer except at minimum width.)

GENERAL

Functions:

AND; OR; Majority Logic; Leading Edge Inhibit; Complement; Pulse standardization without multiple pulsing; coincidence level determined by front-panel selector.

Coincidence Width:

1 ns up, determined by input pulse durations.

Rate:

150 MHz minimum.

Input-Output Delay:

Model 364AL: approximately 6 ns;
Model 365AL: approximately 10 ns.

Multiple Pulse Resolution:

Typical 5 ns; (6.5 ns for triple pulses).

Packaging:

NIM single-width module; LEMO-type connectors used for all inputs and outputs.

Power Requirements:

<u>Model 364AL</u>	<u>Model 365AL</u>
+12 V at 55 mA*	+12 V at 55 mA*
-12 V at 145 mA	-12 V at 165 mA
115 V AC at 70 mA	-24 V at 22 mA
	115 V AC at 70 mA

*Increases to 120 mA if both channels in 4-fold coincidence.

GENERAL DESCRIPTION

The Model 364 AL and 365 AL are dual 4-fold logic gates which offer the functions of fan-in, coincidence, leading edge inhibit, majority logic, and pulse standardization. Each of two identical channels accepts standard NIM logic signals at each of the four logic inputs and one veto input. All inputs are terminated in 50 Ω . Lemo-type connectors are used.

A front-panel selector allows programming the number of simultaneous negative inputs required for an output. With its majority logic capability, the unit may be used to perform voter coincidence such as 1 of 1, 2, 3, 4 (logic fan-in), 2 of 3, 4, or 3 of 4 as well as the standard coincidences of 2 of 2, 3 of 3, 4 of 4. Any of the input serves as an inhibit input when driven with a complementary logic signal. A separate veto input is provided for inhibiting the output regardless of the state of other inputs.

Both channels of the 364 AL and 365 AL may be gated off by means of the NIM bin gate. The bin gate enters the module via the rear multipin power connector and a rear-panel On-Off switch. Quiescently at +5 volts, the bin gate must be clamped to ground to inhibit the logic unit. The bin gate is direct-coupled, and has rise and fall times of approximately 50 ns for the 365 AL and 20 nsec for the 364 AL.

A front-panel selector is provided for programming the participating inputs. Inserting the programming pins in any of the designated Off positions disables that input and eliminates the necessity of removing input cables. A separate storage location is provided for holding the programming pins not in use.

Once the input coincidence conditions have been satisfied, the Model 364 AL and 365 AL generates three double-amplitude NIM fast logic outputs. Each output is provided with two paralleled connectors to enable the signal to be clipped, back-terminated, or fanned-out to two 50 Ω loads. The positive output, or complement ($\overline{\text{OUT}}$) is quiescently at a logical one state (-32 mA) and switches to 0 mA (or 0 volts) for the duration of the output. The two negative outputs (OUT) are quiescently at zero and switch to -32 mA (-800 mV if both connectors drive 50 Ω loads) during an output.

The output duration of each channel of the 364 AL is either the time overlap of the signals satisfying the coincidence conditions, or a fixed 3.5 ns.

The output duration of each channel of the 365 AL is adjustable by means of a front-panel potentiometer from 3.5 ns to 50 ns.

The minimum pulse pair separation of the Model 364 AL/365 AL is under 6 ns for an equivalent CW rate of greater than 160 MHz.

The Model 365 AL is a deadtimeless circuit and will respond to input signals even when an output is already present. The minimum pulse pair separation is under 6 ns for an equivalent CW rate of greater than 150 MHz. If a second coincidence is detected during the time the output from a first coincidence is being produced, the unit will extend the output duration to reflect the occurrence of the second signal. The net output pulse, being the logical sum of two standard output pulses, is of standard amplitude and retains the time information contained in the input signals.

The Model 364 AL/365 AL offers non-multiple-pulsing operation to assure unambiguous response to input pulses regardless of their amplitude or duration. The 364 AL/365 AL will not produce multiple pulses even with input pulses that substantially exceed the output pulse in duration.

SPECIFICATIONS

Number of Channels: Two, both identical.

Input Levels: NIM logic levels: logical 0, 0 mA \pm 2 mA; logical 1, 16 mA \pm 2 mA.

Input Impedance: 50 Ω \pm 5%; value of impedance is constant up to the limit of input protection for negative inputs.

Input Protection: \pm 5 volt protection for pulses. DC overload characteristics are determined by the 250 mW dissipation limit of the 50 Ω input terminating resistor.

Input Coupling: Direct; coupling is independent of input risetime, duration and rate.

Input Reflections: Dependent upon input risetime; less than 10% for input signal of 2 ns risetime or greater.

Gate: Logic unit may be inhibited by application of NIM Bin Gate. Bin Gate enters module via pin of rear multipin connector. Switch located on back panel disconnects Model 364 AL/365 AL from Bin Gate line. Clamping Bin Gate to ground from +5 volts inhibits. Clamping circuit must sink 3 mA per module. Bin Gate circuit is direct-coupled. Rise and fall times are \leq 50 ns for 365 AL and \leq 20 nsec for 364 AL.

Negative Outputs: Two, both with paralleled connectors driven by common high impedance current source. Quiescently, 0 mA, current source switches to -32 mA during output.

Positive Output: One, complimentary, paralleled connectors, quiescently -32 mA (-1.6V into 50 Ω load), switching to zero volts during an output.

Output Duration: Equal to time overlap of input signals or fixed 4.0 ns max., (3.5 ns typical) switch selected for Model 364 AL.

4 ns FWHM to 50 ns, continuously adjustable by means of front-panel width control for Model 365 AL.

Output Rise and Fall Times: 1.2 ns typical, 10% to 90%; fall time slightly longer on wider widths.

Output Duration Stability: Less than 0.1%/°C from 20°C to 60°C.

Coincidence Width: 1 ns up, determined by input pulse duration.

Double Pulse Resolution: Minimum separation to resolve two pulses is typically under 6 ns.

Maximum Rate: 160 MHz typical, input and output; defined for input signals of -600 mV, 3 ns FWHM.

Functions: ANDing, ORing, Majority, Inhibit and Complementary logic.
<20 ps rms.

Multiple Pulsing: None, one and only one output pulse is produced for each input pulse regardless of input pulse amplitude or duration.

Power Requirements: +12 volts at 115 mA, -12 volts at 150 mA, 120 VAC at 33 mA for Model 364 AL.

3.8 watts total; +12 volts at <120 mA, -12 volts at 165 mA, -24 volts at 22 mA, 120 VAC 33 mA; voltages must be regulated to +0.1% for Model 365 AL.

Counting Efficiency: Deadtimeless operation; recovery time is less than output pulse duration; there is no deadtime following output pulse at output durations greater than 8 ns; output duration will update to reflect new input if retriggered while output pulse is present. (Model 365 AL only)

Packaging: The Model 364 AL/365 AL are packaged in conformance with AEC standard for nuclear modules (AEC Report TID 20893 Rev.) Completely compatible physically and electrically with LRS Power Chassis Model 108P, and with any other AEC standard power bin of any manufacturer. Model 364 AL/365 AL is a single-width module using Lemo-type connectors and Model 364 AL/365 AL is a double-width module using BNC-type connectors.

CIRCUIT DESCRIPTION

The Model 364 AL Dual 4-Fold Logic Gate is composed of five basic sections as indicated on the block diagram: a current switch for each input, a set of selectable current sources to set coincidence level, a current summing buffer, a pulse OR ing section, and the output buffers. The Model 365 AL employs a tunnel-diode based trigger stage to provide standardized pulses to the timing stage.

The current switch at each input provides input buffering with proper termination and On-Off control, and causes an 8.6 mA current to be subtracted from the coincidence level current for the duration of the input pulse. The current switch is composed of a MC 1664 non-inverting AND gate. The input may be disabled by shorting the second input of the gate to ground causing the signal input to be ignored. Quiescently, the output of the 1664 gate is "high" (0 volts) and is supplying the current to the 523 Ω resistor which serves as the 8.6 mA current source. An input signal level (\sim 600 mV or greater) causes the open emitter of the output of the 1664 gate to go low, allowing the MBD-101 diode to conduct the 8.6 mA. Since the anodes of the four MBD-101's are connected as a current summing point, each input signal causes 8.6 mA to be subtracted from the coincidence level current source.

The coincidence level current source supplies from 14.3 mA to 40.1 mA depending upon the coincidence level selected. In the "singles" position, the current source supplies 10 mA for the current source buffer, plus 4.3 mA, or 1/2 of an input current switch unit. Each additional level selected over a singles requirement increases the available current by 8.6 mA. The amount of a current available is supplied by the collectors of two transistors connected in a Darlington configuration. The emitters are held at a constant voltage equal to the reference voltage generated by the coincidence level selector. The actual current is determined by the voltage across the two paralleled 432 Ω resistors at the transistor emitters. Any difference between the emitter voltage and the reference voltage is detected by the 741 operational amplifier which adjusts the Darlington input to provide the correct output. This circuit provides stable currents independent of temperature and transistor characteristics.

The current summing buffer section of the 364 AL provides the impedance matching and level shifting required to drive both an inverter and the OR ing stage. It is composed of an emitter follower to decouple the MC1660 input capacitance from the summing point, a 47 Ω resistor to provide the proper DC level, and several current source resistors to provide proper current biasing. The emitter follower directly drives the OR ing section, and drives a MC 1660 inverter.

The inverter can be turned off by switching the front panel switch to Overlap. When switched to Clipped, the inverter supplies a complemented pulse with 1.5 ns inherent delay, which is further delayed by a 2 ns printed circuit delay line which is also supplied to the OR ing section.

The OR ing section of the 364 AL is used to drive the output stage or to completely inhibit the output signals if either veto or bin gate signals are present. The overlap of the normal and delayed complementary signals cause the 1660 gate to provide a clipped, 3.5 ns wide pulse which is independent of the duration of input signal overlap as long as the overlap is greater than 3.5 ns. If either a veto input signal or a bin gate level is present during the overlap, the 1660 will ignore the overlap and no output will be generated. (In Clipped mode, the veto or bin gate need only be present during the first 3.5 ns.) Both the veto input and the bin gate input use MC 1010 NAND gates as inverter/buffers. The outputs of these gates use source terminated printed circuit busses to provide fast, reflection-free connections from the MC 1010 outputs to the MC 1660 inputs.

The tunnel diode section of the 365 AL provides a fast-rise, fixed amplitude pulse anytime the inputs equal or exceed the coincidence level selected. Quiescently, the tunnel diode is in its low voltage state, being supplied with approximately 8.4 mA from the 510 Ω resistor to the -5 volt supply. When the current from the input current switch exceeds that which is available from coincidence level current source, the voltage at the current summing junction drops. This is transmitted through the differential stage (Q3, Q4) to the 10 mA tunnel diode, causing the tunnel diode to switch to its high voltage state. This in turn allows I.C. AB pin 14 to switch to its positive state. This transition is passed onto the next section of I.C. AB through the 43 ohm resistor, in addition to driving a 2 ns printed circuit delay line. After the 2 nsec delay the emitter of Q5 is switched from approximately -1.5 volts to -.8 V thereby back biasing the FD777 diode allowing the current in the tunnel diode to drop to a level just sufficient to keep the diode in its high voltage state. When the input coincidence condition is removed the differential stage switches back to its quiescent state and allows the T.D. to switch back to its low level state.

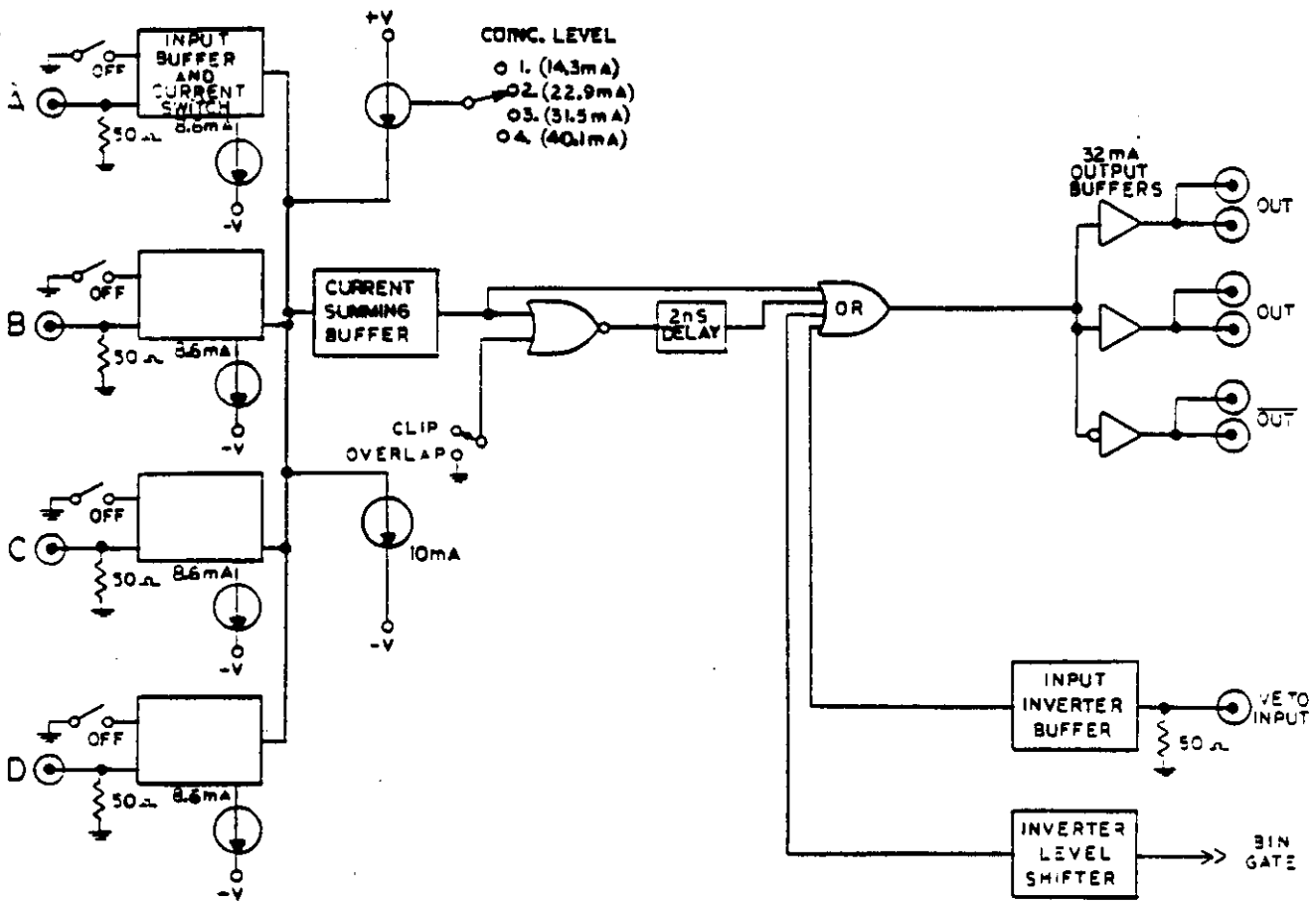
The output of the delay line also drives one input of the veto gate I.C. AB (pins 12, 13 & 15), which provides a delayed signal at its output. The overlap of the normal and delayed signals cause I.C. AB-3 to provide a 2 nsec wide current pulse which is independent of the duration of input signal overlap. If either a veto input signal or a bin gate level is present during the 2 nsec overlap the overlap will be ignored and no output will be generated. The 2 nsec current pulse is supplied to the pulse forming section which generates the desired width output pulse.

The pulse-forming section of the 365 AL, each time a current pulse is received, generates a standardized pulse with a width that is set by the front-panel 2 K Ω width potentiometer. The actual width is determined by a ramp and a comparator. The ramp is generated by raising a capacitor to a fixed voltage using the output of I.C. AB pin 3, and discharging it with an adjustable current source. The comparator is composed of the last section of I.C. AB which generates an output signal whose width is equal to the amount of time the ramp is above an adjustable threshold. The threshold and the adjustable current source are both determined by the front-panel-mounted width potentiometer. Coupling the threshold and ramp slope in this manner permits stable control of the output width over a 4.0 - 50 ns range. Deadtimeless operation is inherent in this design because anytime a pulse is received at I.C. AB pin 3, the capacitor is again raised to the initial rundown voltage. The resulting output thus reflects the receipt of the additional coincidence by extending the output width.

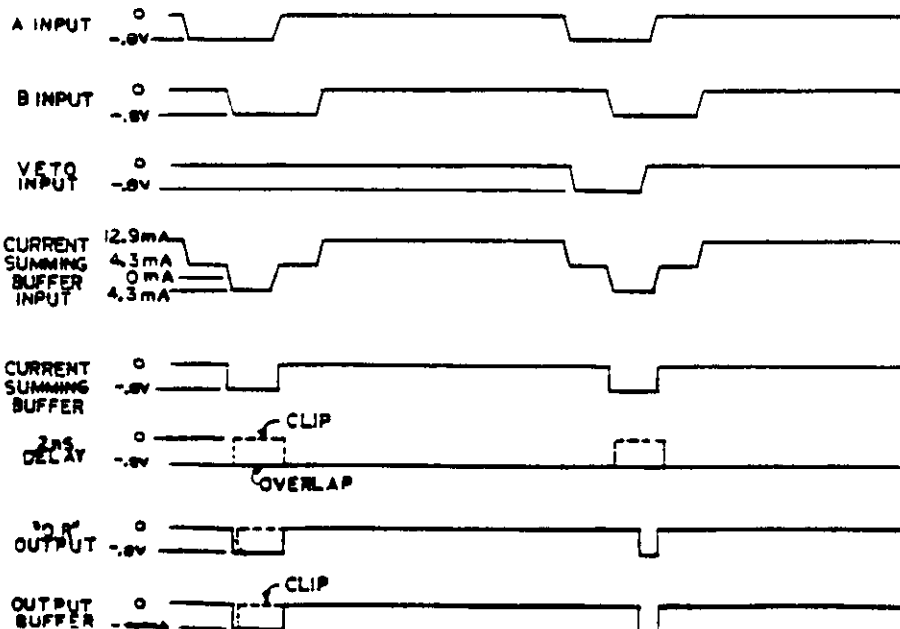
The output buffers provide 32 mA current source output pulses with widths determined by the previous stage. The differential outputs of the OR ing stage drive two separate differential current switching stages. Quiescently, each stage is balanced with one transistor "on" and one transistor "off". The "on" transistor of one stage is connected to the complementary output, which is quiescently at 32 mA, switching to 0 mA during an output. The "off" transistors tied to the normal (OUT) connectors quiescently supply 0 mA and switch to 32 mA during an output. Each output drives two paralleled connectors. All outputs are limited by the MBD 101 clamp diodes, and the -1.5 volt supply (Q9 & Q10) 0, to -2 volts.

In addition to using the standard +12 volts from the power connector, the Model 364 AL/365 AL also requires +0.8 and -5.0 volts. This is supplied by an internal 5.8 volt supply using 120 VAC from the rear power connector. The positive side of the supply is referenced to +0.9 volts by an emitter follower operating from a 741 operational amplifier. The reference for the op-amp is derived from a resistor divider connected between +12 volts and ground.

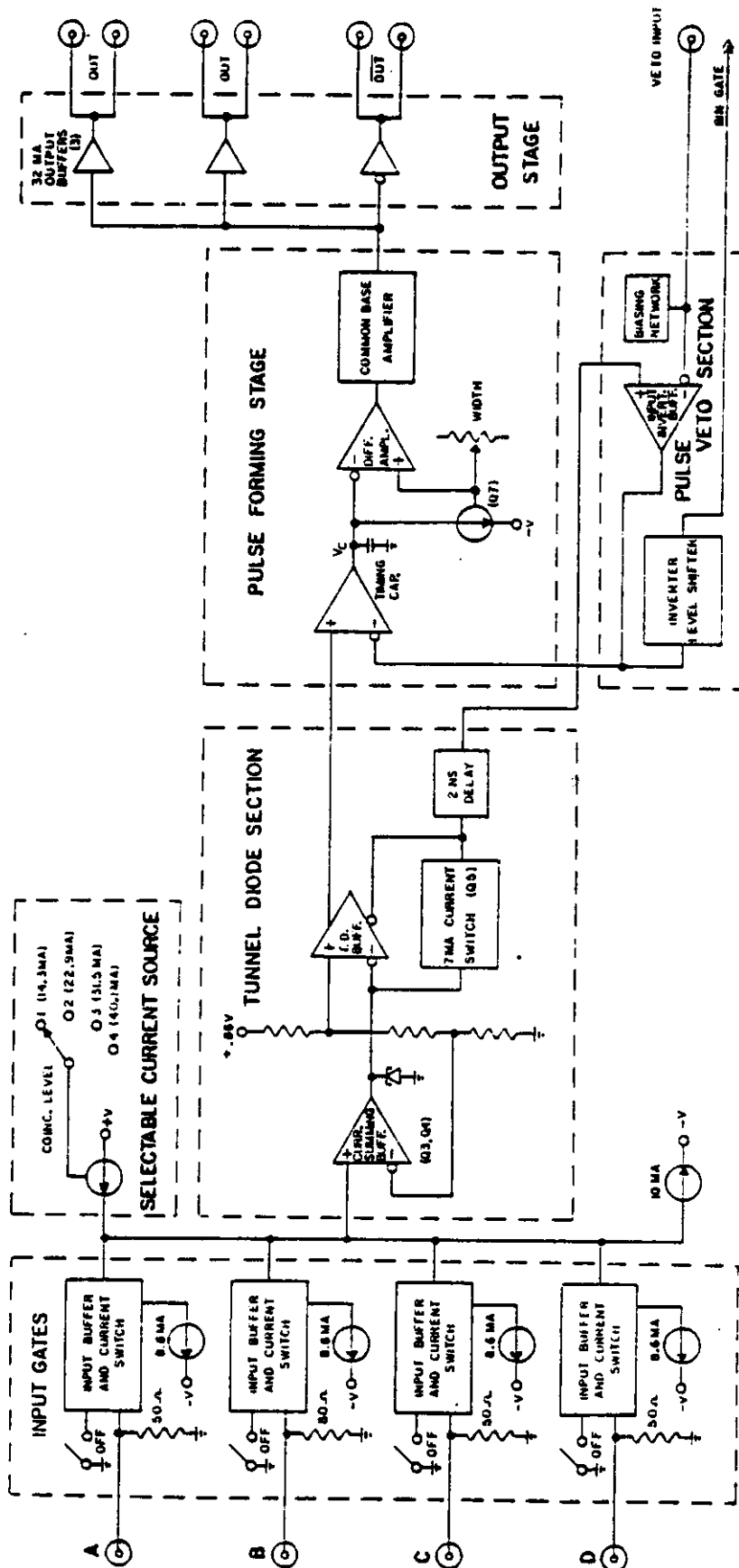
MODEL 364 BLOCK DIAGRAM



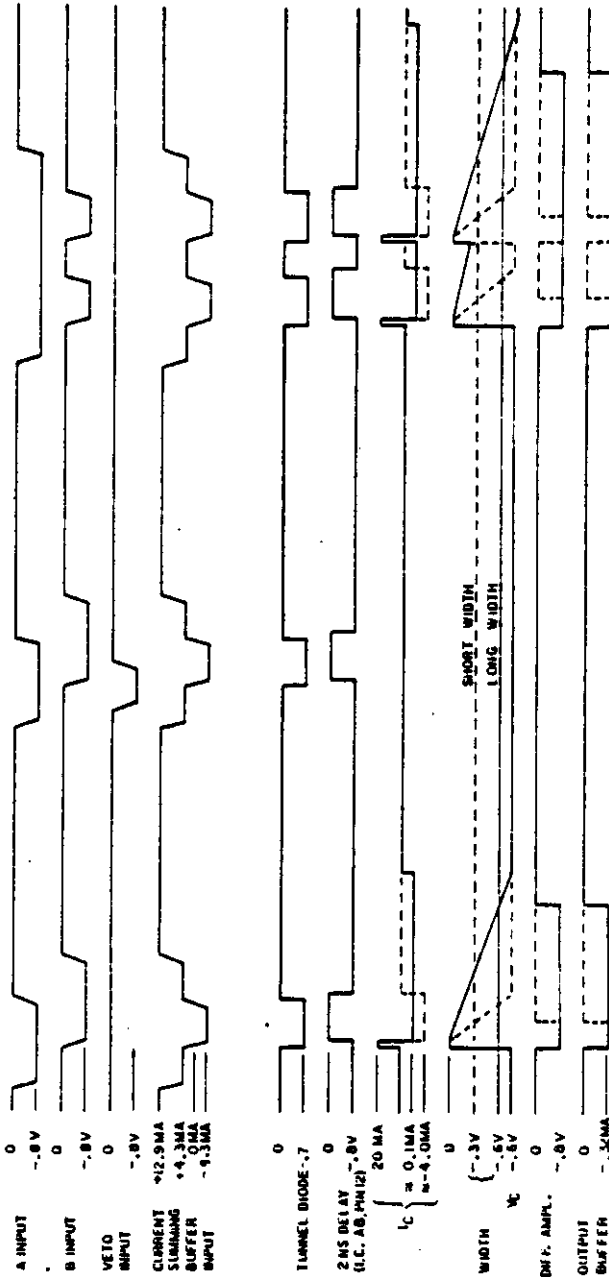
INTERNAL WAVEFORMS USING TWO INPUTS - A & B
WITH COINCIDENCE LEVEL SET AT 2



MODEL 365 BLOCK DIAGRAM



INTERNAL WAVEFORMS USING TWO INPUTS - A & B, WITH COINCIDENCE LEVEL SET AT 2.



MODEL NO 755AL
LAST REVISION NO 1007

4-FOLD LOGIC UNIT
REVISION DATE 17-Sep-79

PRINTED 13-Apr-81

148	531	401	RES PPREC RM55D	1.21 K	
159	531	479	RES PPREC RM55D	3.01 K	
168	531	435	RES PPREC RM55D	5.32 K	
121	427	103	RES VARI CERMET	10 K	1/2W 10%
137	527	202	RES VARI CERMET	2 K	3/4W 10%
202	431	443	IC 2-IN OR GATE	MC1564L	QUAD PKG/HI-Z/DIP-16
204	431	444	IC LINE RECEIVER	MC1492L	QUAD PKG/DIP-16
208	411	441	IC SINGLE OP AMP	UA741C	DIP-8
242	110	443	DIODE SWITCHING	1N4448	
242	110	445	DIODE SWITCHING	1N4448	
242	225	702	DIODE ZENER 2.6V	1N702A	250MU
242	225	703	DIODE ZENER 3.45V	1N703A	250MU
250	134	104	DIODE TUNNEL	LE005010804	10mA
257	412	235	DIODE HOT CARRIER	MP2835	4-P CASE 15
270	110	441	TRANSISTOR NPN	2N2369A	TO-18
270	110	401	TRANSISTOR NPN	A401	TO-72
270	150	441	TRANSISTOR NPN	2N3053	TO-5
270	170	441	TRANSISTOR NPN	2N5770	TO-92
275	150	443	TRANSISTOR PNP	40319	TO-5
275	170	442	TRANSISTOR PNP	2N5771	TO-92 SEE 275-170-004(MPS3640)
290	410	441	BEAD SHIELDING	FERRITE	
290	420	441	BEAD SHIELDING "1/2" SIZE		
290	450	441	CHOKE FERRITE SINGLE LEAD		
291	414	233	INDUCTOR BOLDED	92.00 UH	
315	430	442	POWER SUPPLY		
400	410	440	SOCKET IC ST	DIP-8	BONDED TIN CONTACTS/COPP-NICKEL PINS
401	410	415	SOCKET IC ST	DIP-16	BONDED TIN CONTACTS/COPP-NICKEL PINS
402	430	130	CONNECTOR CO-AXIAL	LEMO	
402	430	172	SPANNER NUT SMALL OD	LEMO	
402	430	443	GROUND LUG NON LOCK	LEMO	
402	430	444	GROUND STRAP "H"	LEMO	
404	430	130	CONN PC DUAL 30/2 ROWS 15		GAME 48 404 020 030 BUT 479 INSERT
405	110	441	CONNECTOR BLOCK	(PIN)	42 "MIXED"
405	212	442	GUIDE PIN	(MALE)	CADMIUM PLATED BRASS
405	212	441	GUIDE PIN	(MALE)	BRASS
405	212	443	GUIDE PIN	(FEMALE)	CADMIUM PLATED BRASS
405	410	414	CONNECTOR PIN	(MALE)	
405	417	441	CONNECTOR HOOD		CADMIUM PLATED STEEL/INT CLOSED END
405	750	443	PROGRAM PIN FOR PC CONN		373-11-000-09 13-00041
420	210	441	SWITCH SLIDE	090T	
500	120	442	TRANDIPAD	"LARGE"	
520	100	440	SPACER FIBER #1	1/16	
540	101	102	SIDE COVER	NIN LEFT	
540	101	103	SIDE COVER	NIN RIGHT	
540	104	101	WRAPAROUND	NIN SIZE #1	WITH BIN GATE
540	105	441	BRACKET NIN WRAP SIZE #1		
775	411	441	CAPTIVE SCREW	4-10	
775	421	440	CAPTIVE SCREW RETAINED		NICKEL PLATED BRASS
801	226	443	SCREW FLAT PHIL 2-58X1/4		
811	345	417	PC BO BRACKET	255A	
820	115	417	FRONT PHL BRACKET	355AL	510102001(1)555821000(1)
830	441	440	WRAPAROUND NIN 1 PIN GATE		510104101(1)

101	243	*32	PC	STOCK	DBL	SIDED	1	OZ				
102	145	104	CAP	CERA	DISC	12V	.1	UF	PT-FDCL-1/32	LEADS	3/8	AWG 22
102	245	103	CAP	CERA	DISC	25V	.01	UF	PT-FDCL-1/32	LEADS	3/8	AWG 22
102	444	101	CAP	CERA	DISC	100V	100	PF	10% S3M			
102	444	230	CAP	CERA	DISC	100V	22	PF	10% S2L			
102	444	330	CAP	CERA	DISC	100V	33	PF	10% S2L			
102	745	201	CAP	CERA	DISC	500V	200	PF	PT-FDCL-1/32	LEADS	3/8	AWG 22
102	745	221	CAP	CERA	DISC	500V	220	PF	PT-FDCL-1/32	LEADS	3/8	AWG 22
102	944	*50	CAP	CERA	DISC	1KV	5.0	PF	10% S2L			
102	944	100	CAP	CERA	DISC	1KV	10	PF	10% S2L			
102	944	120	CAP	CERA	DISC	1KV	12	PF	10% S2L			
102	944	150	CAP	CERA	DISC	1KV	15	PF	10% S2L			
102	924	435	CAP	TANT	DIP	CASE	6.8	UF	35V 20%			
107	447	*50	CAP	ALUM	METAL	CAN	50	UF	15 OR 16V -10% +75%			
161	335	*27	RES	COMP	1/4W	5%	2.7	OHMS				
161	335	100	RES	COMP	1/4W	5%	10	OHMS				
161	335	102	RES	COMP	1/4W	5%	1	K				
161	335	103	RES	COMP	1/4W	5%	10	K				
161	335	112	RES	COMP	1/4W	5%	1.1	K				
161	335	121	RES	COMP	1/4W	5%	120	OHMS				
161	335	122	RES	COMP	1/4W	5%	1.2	K				
161	335	151	RES	COMP	1/4W	5%	150	OHMS				
161	335	152	RES	COMP	1/4W	5%	1.5	K				
161	335	202	RES	COMP	1/4W	5%	2	K				
161	335	220	RES	COMP	1/4W	5%	22	OHMS				
161	335	222	RES	COMP	1/4W	5%	2.2	K				
161	335	270	RES	COMP	1/4W	5%	27	OHMS				
161	335	271	RES	COMP	1/4W	5%	270	OHMS				
161	335	272	RES	COMP	1/4W	5%	2.7	K				
161	335	300	RES	COMP	1/4W	5%	30	OHMS				
161	335	301	RES	COMP	1/4W	5%	300	OHMS				
161	335	341	RES	COMP	1/4W	5%	340	OHMS				
161	335	362	RES	COMP	1/4W	5%	3.6	K				
161	335	363	RES	COMP	1/4W	5%	36	K				
161	335	390	RES	COMP	1/4W	5%	39	OHMS				
161	335	392	RES	COMP	1/4W	5%	3.9	K				
161	335	430	RES	COMP	1/4W	5%	43	OHMS				
161	335	470	RES	COMP	1/4W	5%	47	OHMS				
161	335	471	RES	COMP	1/4W	5%	470	OHMS				
161	335	510	RES	COMP	1/4W	5%	51	OHMS				
161	335	511	RES	COMP	1/4W	5%	510	OHMS				
161	335	560	RES	COMP	1/4W	5%	56	OHMS				
161	335	562	RES	COMP	1/4W	5%	5.6	K				
161	335	620	RES	COMP	1/4W	5%	62	OHMS				
161	335	620	RES	COMP	1/4W	5%	62	OHMS				
161	335	750	RES	COMP	1/4W	5%	75	OHMS				
161	335	911	RES	COMP	1/4W	5%	910	OHMS				
161	445	301	RES	COMP	1/2W	5%	300	OHMS				
161	445	511	RES	COMP	1/2W	5%	500	OHMS				
162	531	352	RES	PREC	RN557		432	OHMS				
162	531	362	RES	PREC	RN550		475	OHMS				
162	531	371	RES	PREC	RN553		523	OHMS				
162	531	381	RES	PREC	RN550		553	OHMS				
162	531	397	RES	PREC	RN550		1.10	K				

DESCRIPTION

ECO NO. DATE

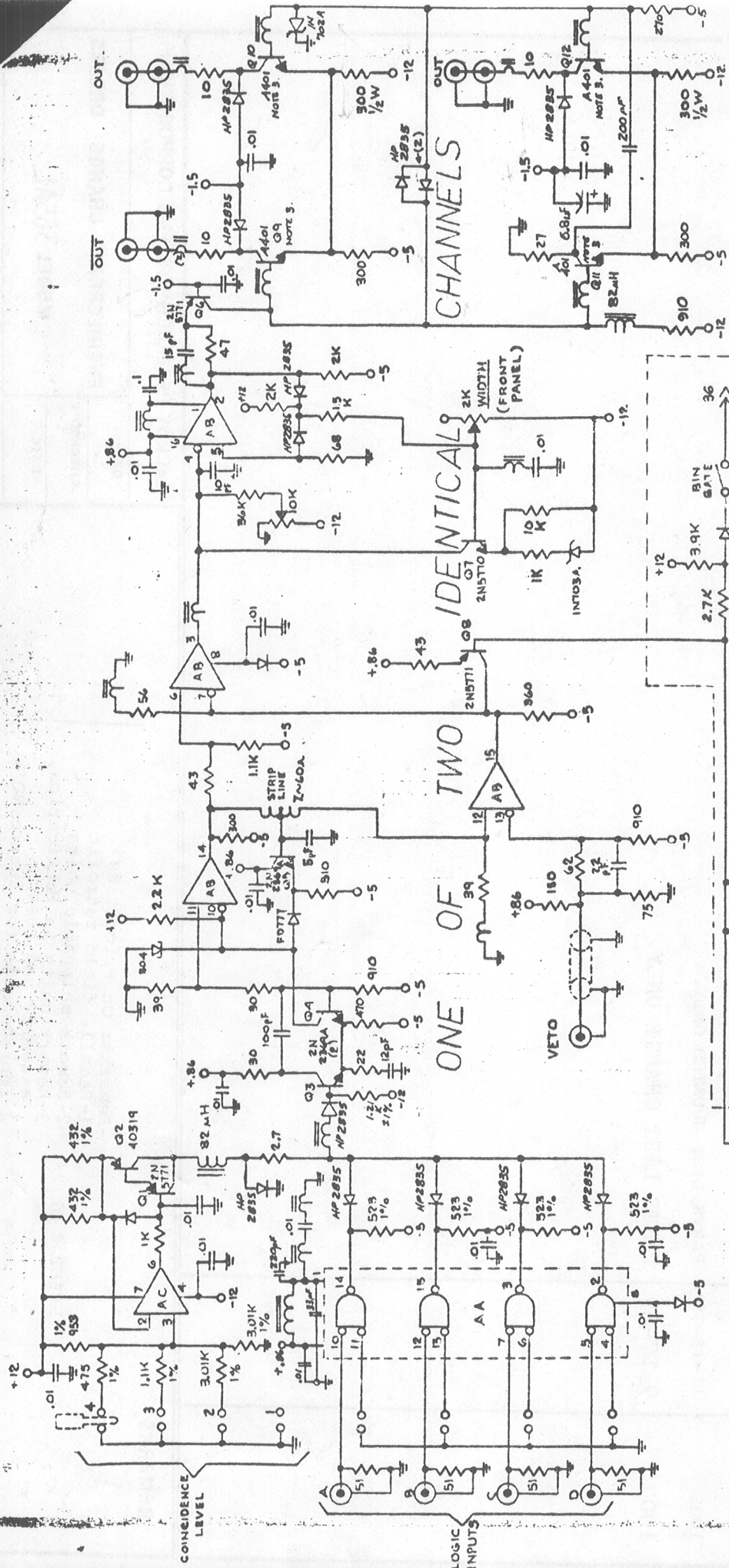
547	12-6-77	ASSEMBLY CHANGES ONLY.
1001	3-9-78	ASSEMBLY CORRECTIONS ONLY.
1002	6-7-78	CHANGED FRONT PANEL TO 2024-T5 ALUMINUM (DWG. NO. 265A-M1 & 365AL-M1).
1003	6-27-78	SEPARATED 365AL AND 365ALP PARTS LISTS INTO "BASIC" AND "ADDER" VERSIONS.
1004	8-9-78	PARTS LIST UPDATED ONLY.
1005	8-21-78	BROUGHT MINIMUM WIDTH TO LESS THAN 4 NSEC BY CHANGING 5.1K RES TO 2.0 K FROM +12V TO JUNCTION OF 2 HP2835'S. (SHEET 1 OF SCHEMATIC AFFECTED).
1006	11-15-78	PARTS LIST UPDATED ONLY.
1007	9-17-79	PARTS LIST CHANGE ONLY.

REMARKS

SHEET 2 OF 2

- Remarks: On Priorities
- 1-Recall, field retrofit
 - 2-Rework shippable units
 - 3-Rework units in fabrication, assembly and test
 - 4-Improvements for future MO's

LeCROY RESEARCH SYSTEMS CORPORATION	
DRAWN	ENGINEERING CHANGE ORDERS
CHECKED	MODEL 365AL
DATE	
DRAWING No.	



LeCROY RESEARCH SYSTEMS CORPORATION
 WEST YARAC, NEW YORK
 DRAWN J G P
 CHECKED WPC
 DATE 2-15-72
 DUAL 4-FOLD LOGIC UNIT
 MODEL 365A
 DRAWING No. 365A-S1 REV. ECO 100
 9/17/72

- NOTES:
 1 ALL UNMARKED DIODES INQ14
 POWER DESIGNS # X479
 OR LAMBDA LZ-10.
 2 ALSO MAY BE REPLACED BY 2N 5054.

C'S	REF	+12	+86	-12	-4.3
741	AC, BC, D	7	4		
MC1664	AA, RA	1, 16	8		
MC1692	AB, BB	1, 16	8		