WARRANTY

LeCroy Research Systems warrants its instrument and software products to operate within specifications under normal use and service for the period of one year from date of shipment. Custom monolithics and hybrids sold separately and all spare or replacement parts and repairs are warranted for 90-days. This warranty extends only to the original purchaser and shall not apply to fuses, magnetic recording media, disposable batteries, or any equipment not manufactured by the company. All non-LeCroy products are provided with the original equipment manufacturer's warranty, which is typically 90-days from the date of shipment.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the factory or an authorized service facility within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials. If the failure has been caused by misuse, neglect, accident, or abnormal conditions or operations, repairs will be billed at a nominal cost. In such cases, an estimate will be submitted before work is started.

The purchaser is responsible for the transportation charges arising from the return of products to the factory or authorized service facility. LeCroy will return all in-warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy Research Systems shall not be liable for any special, incidental, or consequential damages, whether in contract, or otherwise.

POST WARRANTY REPAIRS

For all LeCroy products in need of repair after the warranty period, the customer must provide a Purchase Order Number before any inoperative equipment can be repaired or replaced. The customer will be billed for the parts and labor for the repair as well as for shipping.

RETURN PROCEDURE

To determine your nearest authorized service facility, contact the factory or your local field office. All products returned for repair should be identified by the model and serial numbers and include a description of the defect or failure, name and phone number of the user, and, in the case of products returned to the factory, a Return Authorization Number (RAN). The RAN may be obtained by contacting the Customer Services Department at 914-425-2000.

Return shipments should be made prepaid. LeCroy will not accept C.O.D. or Collect Return shipments. Air-freight is generally recommended. Wherever possible, the original shipping carton should be used. If a substitute carton is used, it should be rigid and be packed such that the product is surrounded with a minimum of four inches of excelsior or similar shock-absorbing material. In addressing the shipment, it is important that the Return Authorization Number be displayed on the outside of the container to insure its prompt routing to the proper department within LeCroy.

INITIAL INSPECTION

It is recommended that the shipment be thoroughly inspected immediately upon delivery to purchaser. All material in the container should be checked against the enclosed Packing List. LeCroy cannot accept responsibility for shortages in comparison with the Packing List unless notified promptly. If the shipment is damaged in any way, please contact the factory or local field office immediately.

DOCUMENTATION DISCREPANCIES

LeCroy Research Systems is committed to providing state-of-the-art instrumentation. As a result, the Engineering Department at LeCroy is continually refining and improving the performance of products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying unit. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

APPLICATIONS ASSISTANCE

Answers to questions concerning the installation, calibration, and use of LeCroy equipment are available from the Customer Services Department, LeCroy Research Systems Corp., 700 South Main Street, Spring Valley, New York, telephone 914-425-2000, or your local field sales office.

A T T E N T I O N

CRATE POWER SHOULD BE TURNED OFF DURING INSERTION AND REMOVAL OF UNIT TO AVOID POSSIBLE DAMAGE CAUSED BY MOMENTARY MISALIGNMENT OF CONTACTS.

SEE POCKET IN BACK OF MANUAL FOR SCHEMATICS, PARTS LIST ADDITIONAL ADDENDA WITH ANY CHANGES TO MANUAL.

A T T E N T I O N

LeCroy

CAMAC ECLine Model 4532

32 Input Majority Logic Unit

- **High channel density: 32 parallel inputs**
- **Majority information up to 16 hits**
- **Single hit or cluster mode**
- **2 by 2 fast OR logic outputs**
- **Hit pattern CAMAC readable**
- **Self triggered or externally gated operation**
- **Provisions for multiple module cascading**

The new generation of high energy physics experiments, involving extremely high counting rates and/or large detector arrays, requires a "total system" approach to instrumentation. LeCroy's new CAMAC 4000 Series of ultra-fast, high-density programmable instrumentation modules provides the solution to this requirement by allowing the experimenter to achieve full computer control of the data acquisition system within a single instrumentation standard.

The ECLine Model 4532 answers most of the majority logic problems encountered in modern High Energy Physics Experiments.

The Model 4532 calculates the multiplicity value from 32 logic channels and presents the result as a current proportional to the number of inputs up to a maximum of 16. These may be either individual inputs or clusters (i.e. adjacent inputs are counted as one input) as determined by a side switch. The multiplicity calculation can either be performed on the overlap of input pulses during a time determined by an externally applied gate (e.g. with photomultipliers), or on latched levels which are set by inputs occurring within a predetermined time window (e.g. for use with proportional chambers). In the latter mode, the analog output will increase as each pulse arrives at the inputs. The time window can be either internally generated or externally provided. The internal time window is self-triggered by the first input pulse arriving after a previous reset. A front panel potentiometer permits adjustment of the time window.

In addition to the front panel outputs, the Model 4532 also stores the input information which arrived during the time window in a CAMAC addressable 32-bit register. In both the overlap Memory Disable and latching Memory Enable modes, a front panel output provides a two by two OR of the gated inputs. The OR is performed on channels 1 and 2, 3 and 4, etc. In Overlap mode, the outputs will be pulses having a width determined by the input pulse widths, while in Latching mode the outputs will be levels set by the leading edge of the input pulses and reset by the CAMAC or front panel fast reset functions.

The Model 4532 analog output is provided on two paralleled connectors to permit the cascading of several majority units and extending the multiplicity calculation beyond 32 inputs.

The analog output is designed to be used as input to a variable threshold discriminator, or to the Model 4504 Flash ADC for conversion into a four-bit binary word.

October 1982

Innovators in Instrumentation

LeCROY RESEARCH SYSTEMS SA • RUE CARDINAL-JOURNET 27 • 1217 MEYRIN 1-GENÈVE SUISSE
TELEX: 28230 TELEPHONE: (022) 82 33 55

SPECIFICATIONS
CAMAC ECLine Model 4532
32 INPUT MAJORITY LOGIC UNIT

INPUT CHARACTERISTICS

All inputs accept differential ECL level (– 0.8 V, – 1.7 V) into 110 ohm input impedance (high input impedance is possible by removing socket mounted terminators).

Data Input (IN):	32 in two 34 pin front panel connectors; minimum input pulse width 6 nsec, maximum width DC.
Reset Input (RTI):	Fast reset of the input registers; generates a reset of the analog majority output and of the comparator outputs (MDO, DMO). When the analog output is cascaded with other units, the RTI only resets the contribution from the modules that received the RTI. Minimum input pulse width 6 nsec, maximum width DC. In Memory Disable mode, the RTI is inhibited.
Gate Input (GAI):	Normally open when unconnected. Normally closed when connected to a cable providing standard ECLine levels. In Memory Disable mode, data pulses having an overlap with the GAI will contribute to the outputs. In Memory Enable mode, data pulses having their leading edge inside the GAI time will be accepted and stored. By deriving the GAI from the DMO, an internally generated time window is possible. Minimum overlap time width with input pulses for majority decisions, 10 nsec. Minimum overlap time width with input pulses for logical OR's, 3 nsec; maximum width DC.
Cluster Carry (CCI):	When Cluster Selection is Enabled, receives the carry information on the cluster from the Cluster Carry Output (CCO) of any adjacent majority logic unit.
Analog Majority Input/Output (AMIO):	Two bridged front panel Lemo type connectors; high impedance current source; generates a current proportional to the input multiplicity at the rate of 3.2 mA per hit (or 80 mV per hit into 25 ohms). The AMIO connectors can be used for daisy chaining of analog majority information within a group of similar units. Transit time between AMIO connectors 2 nsec. Unused output must be terminated with 50 ohms.

OUTPUT CHARACTERISTICS

All logic outputs provide complementary ECL levels (– 0.8 V, – 1.7 V) and are capable of driving differential 110 ohm loads.

Data Outputs (OUT):	16 in a 34 pin front panel connector. Each output corresponds to the logical OR of two channels (respectively, 1 and 2, 3 and 4, . . ., 31 and 32). In Memory Disable mode, provides pulses corresponding to an overlap coincidence between the gate pulse and the data inputs. In Memory Enable mode, provides levels started by the coincidence between the gate pulse and the leading edge of the data pulses.
OR Output (ORO):	Provides the logical OR of the 32 channels, otherwise, behaves as data outputs.
Strobe Output (STO):	Provides a pulse, suitable for strobing of subsequent logic units, at the end of the gate input and delayed by the internal transit time (6 nsec). Width adjustable from 10 to 25 nsec by a trimmer (STROBE WIDTH) accessible from the side of the module.
Majority Discriminated Output (MDO):	The AMIO input/output is internally used as input to an adjustable threshold comparator providing the MDO output. Threshold adjustable from 1 to 16 hits by a front panel potentiometer (MA THR). The output will be a pulse or a level depending on the selected operating mode.
Delayed Majority Output (DMO):	Reproduces the output MDO above, after an adjustable delay. A switch on the side of the module (DM RANGE) selects one of two delay ranges; 10-100 nsec or 50-1000 nsec. A front panel potentiometer (DMO DELAY RANGE) permits continuous adjustment. The DMO is cleared as soon as the MDO is cleared.
Cluster Carry (CCO):	When Cluster Selection is Enabled, indicates that Output channel 32 was hit for use in conjunction with channel 1 of a logically adjacent cluster logic in another 4532 module (CCI input).

CAMAC COMMANDS

Z, C	Clears data memory and LAM at S2 time.

L	A Look-At-Me signal is generated (in Memory Enable mode only) at the end of the gate input if the OR output is set. The LAM may be enabled or disabled by the LAM enable switch accessible on the side of the module.
X	An X = 1 response is generated for any executable function.
Q	A Q = 1 response is generated for any executable function in Memory Enable mode only
F(0)•A(0), A(1)	Read input pattern. A(0): channels 1 to 16. A(1): channels 17 to 32. A Q response is generated in Memory Enable mode only.
F(1)•A(0)	Read status register: R1 = 1 if LAM is ON R2 = 1 if LAM Enable switch is ON R3 = 1 if MEMORY Enable switch is ON R4 = 1 if CLUSTER Enable switch is ON Q response is always generated.
F(2)•A(0)	Read input pattern, channels 1 to 16. Q response is generated in Memory Enable mode only.
F(2)•A(1)	Read input pattern, channels 17 to 32, and clears the 32 channel data memory and LAM at S2. Q response is generated in Memory Enable mode only.
F(8)•A(0)	Test LAM: a Q response is generated if L is ON.
F(9)•A(0)	Clears the data memory and LAM at S2. Q response is generated in Memory Enable mode only.
F(10)•A(0)	Test and clear LAM, clears LAM at S2 time. Q response is generated if L is ON. The clear LAM operation is not executed if Q response is missing.

GENERAL

Mode Selection:

A Memory Enable switch, accessible on the side of the module, selects one of the following modes:

Memory Disable:
Functions are disabled: the multiplicity calculation is performed on the overlap of the data inputs.

Memory Enable
The data inputs are latched: the multiplicity is determined by the number of leading edges of data input pulses occurring during the gate time. In this mode the unit needs to be cleared either by the reset input (RTI) or by a resetting function.

Cluster Selection:

The Cluster Enable switch, accessible on the side of the module, determines one of the two following modes:

Cluster Disable:
Each data input provides one hit on the Analog Majority Output AMIO: the Cluster Carry Input (CCI) is disabled:

Cluster Enable:
Any group of adjacent input data pulses will be considered as a single hit.

Provision has been made for the clusters to extend beyond the 32 inputs. If an input is present on the logically adjacent channel to input 1 of this unit but is located in another unit, the CCI can be used to indicate its presence. The CCO of this module indicates that channel 32 of this module is present.

Transit Times:

Data IN to AMIO	16 nsec
AMIO to MDO output	5 nsec
End of gate IN to Strobe OUT	6 nsec
Data IN to Data OUT	12 nsec
Data IN to OR OUT	16 nsec
Reset IN to Data OUT	20 nsec
Reset IN to OR OUT	24 nsec
Data IN 32 to Cluster Carry OUT	11 nsec
Cluster Carry IN to Data IN 1	2 nsec

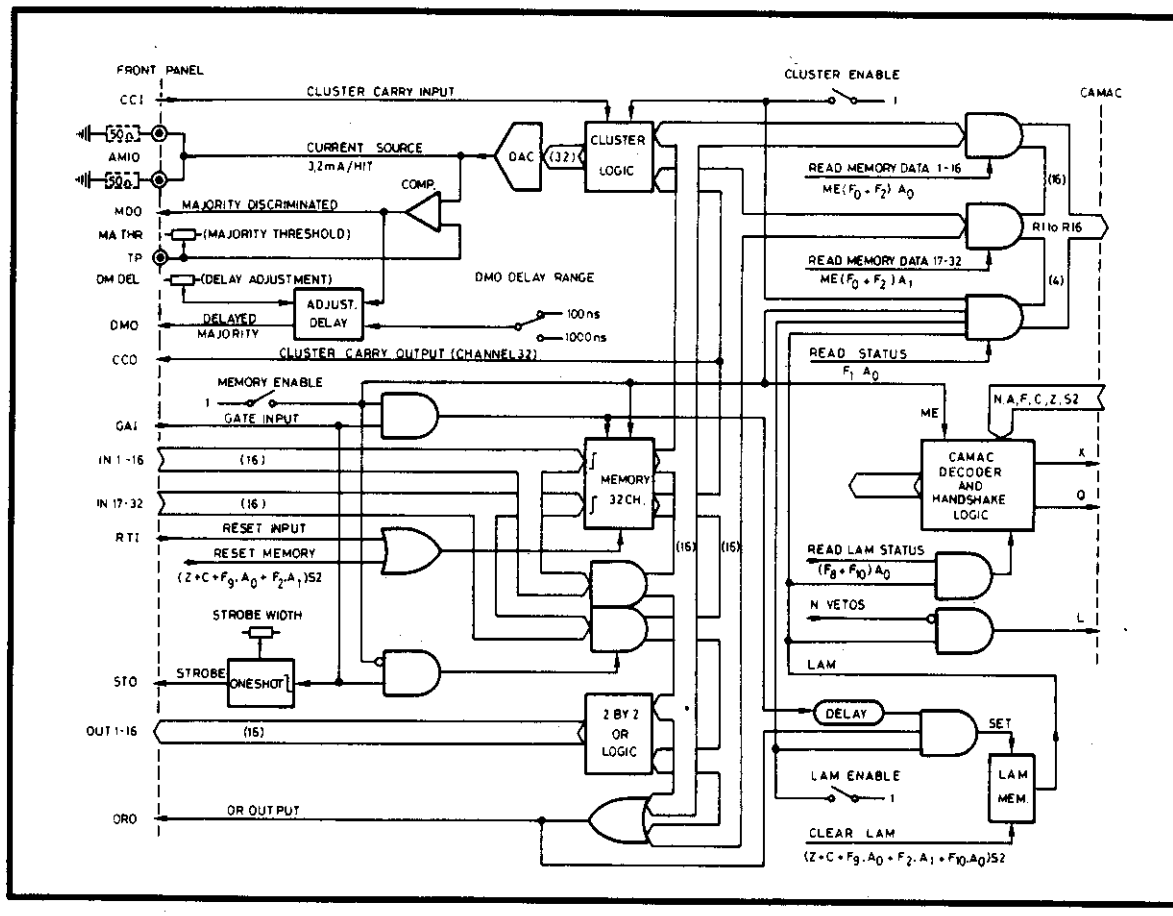
Gate pulse must precede Data pulse by at least 7 nsec.

Current Requirements:

+ 6 V at 200 mA
− 6 V at < 3.6 A (3 A when empty)
+ 24 V at 5 mA
− 24 V at 7 mA

Packaging:

Single-width standard CAMAC module.



BLOCK DIAGRAM
MODEL 4532 MAJORITY LOGIC UNIT

SPECIFICATIONS SUBJECT TO CHANGE

LeCroy

GENERAL DESCRIPTION

The LeCroy Model 4532, Majority Logic Unit, has two basic modes of operation depending on the position of the MEMORY ENABLE switch.

If the MEMORY ENABLE switch is OFF, the 4532 is completely transparent with respect to inputs and outputs.The information present at all outputs will be a function of the instantaneous signals at the inputs during the gate time. The CAMAC functions become clearely meaningless, and will not be executed. No Q response will be generated.

If the MEMORY ENABLE switch is ON, pulses arriving at the input having their leading edges falling during the GATE pulse widths, will be stored.

Consequently, at the end of the GATE pulse, all the outputs will be stable and a LAM signal can eventually be generated. The information at the outputs will remain stable until a reset is applied either by CAMAC or by the input RTI (Reset Input).

It should be noted that the RTI input does not clear the LAM. This avoids problems during the CAMAC search for LAM sources.

On the other hand, the RTI input cleares the data memory. Therefore care should be taken to synchronisation the CAMAC activity with with the RTI signals.

FUNCTIONAL DESCRIPTION

The following description refers to the bloc diagram and schematics included with this manual. Depending on the operation mode, the input pulses can either set bits in a memory or go through an AND gate enabled by the GATE input.

After this initial stage, the signals coming either from the memory or from the AND gate, follow same path. These signals are termed "internal data", and pass through the following consecutive logic stages.

1. OR outputs

The module provides a general logical OR of the 32 internal data on the output connector ORO (OR Output). In addition, the logical OR of the internal data taken 2 by 2 (IN1.OR.IN2 on OUT1, IN3.OR.IN4 on OUT2, and so on) is generated on the OUTs 1 to 16.

2. Cluster logic

If the CLUSTER ENABLE switch is OFF, the 32 channels of internal data go directly to the Digital to Analog Converter (DAC) which sets the multiplicity analog level at the output. If the CLUSTER ENABLE switch is ON, each internal data vetoes the adjacent higher one. Consequently only the first bit in a set of consecutive bits (cluster) will be active into the DAC.

In order to cascade several 4532's, channel 1 can be vetoed by the Cluster Carry Input (CCI). The internal data present on channel 32 is provided for the next 4532 module on the Cluster Carry Output (CCO).

3. Analog Majority Input-Output (AMIO)

After the cluster logic the data is converted to a current by the DAC.

The presence of a bit in the data coming into the DAC generates a 1.6 mA current source (adjustable by changing the Voltage-VD) in circuitry which at the same time adds these currents.

The sum of the currents is performed by the common base mounted transistors T1 and T2.

The collectors of T1 and T2 are connected together to finally give the total sum of the currents. This total current is carried to the base of transistor T12 and the collector of transistor T3.

The current flowing through T4 and T12 will be the image of the one flowing through T3. This fact permits the transfer of the current to T5, T13 and T6, mounted in the same configuration as T3, T4, T12.

The resistance on the T6 emitter is one half of the one on the T5 emitter. This means that the current finally procided by T3 at the output, will be of 3.2 mA/hit. In order to compensate the different offset currents that can be present, the transistor T7 produces a constant current, adjustable by the internal potentiometer OADJ (offset adjustement), permitting a zero quiescient current on AMIO.

The circuitry is protected against missing 50 Ω terminations at the AMIO outputs, by the 39 Ω resistor between T12 and T5.

4. Majority Discriminated Output (MDO)

The AMIO signal is directly connected to a comparator input. The comparator threshold can be adjusted between O V and -1.5 V by the front panel potentiometer MATHR (Majority Threshold). It should be noted that the status of MDO output will be conditioned not only by the DAC output, but also by signals connected to the AMIO from other units.

5. Delayed Majority Output (DMO)

The output DMO is internally connected to a delay circuit based on the principle of a comparator connected to a capacitor being charged by a constant current. The comparator threshold, and resulting delay, can be adjusted by the front panel potentiometer DM DEL. The digital output of comparator MDO regulates the charge and discharge of this capacitor. When the MDO is off the transistor T8 discharges and holds the capacitor at a high reference voltage. When the MDO comparator provides a signal, T8 goes off and the capacitor charges with constant current and the amplitude of this charge is limited by T9.

The DM DEL switch selects two capacitor values to permit two different delay ranges.

6. Strobe Output (STO)

The width of the strobe output is determined by the charge at constant current of the variable capacitor ST WIDTH. When a gate signal GAI is applied, it closes the gate B1 and charges the variable capacitor. The amount of the charge is limited by T10 and T11. At the end of the gate pulse, B1 opens again and the variable capacitor discharges. The strobe output STO will be present as long as the voltage on the variable capacitor is greater than the threshold of B1.

It should be noted that STO is cleared by GAI and starts again from the end of GAI.

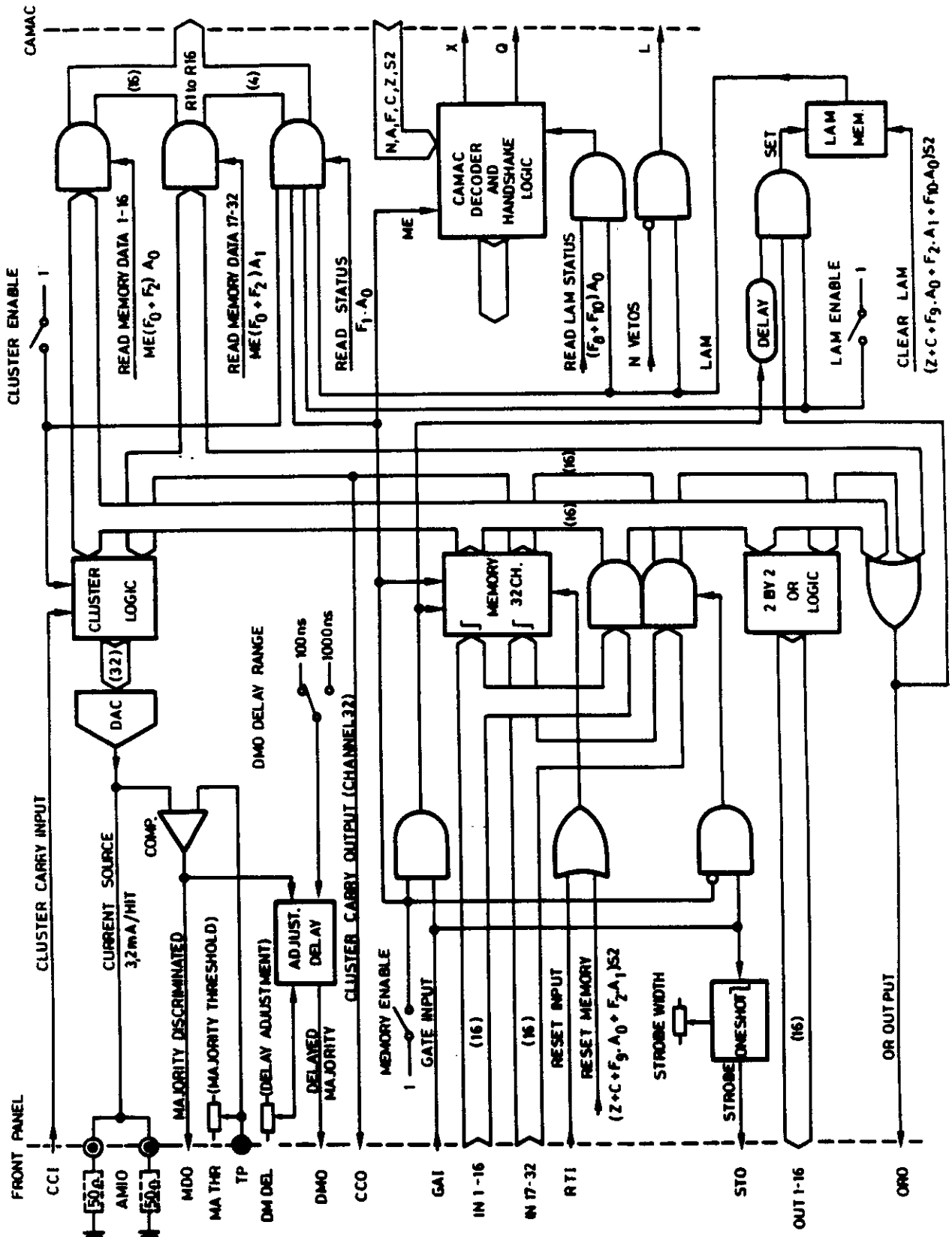
7. LAM circuit

LAM circuit is composed of the two flip-flops I1. The first one memorizes a LAM request and acts on the L line. Its setting is dependent on switches LAM ENABLE and MEMORY ENABLE being ON. The first flip-flop is set by the leading edge of the signal provided by gate B1, pin 14, and translated by transistor T12.

Gate B1 has the function of halting the OR signal during GAI which would have generated a LAM.

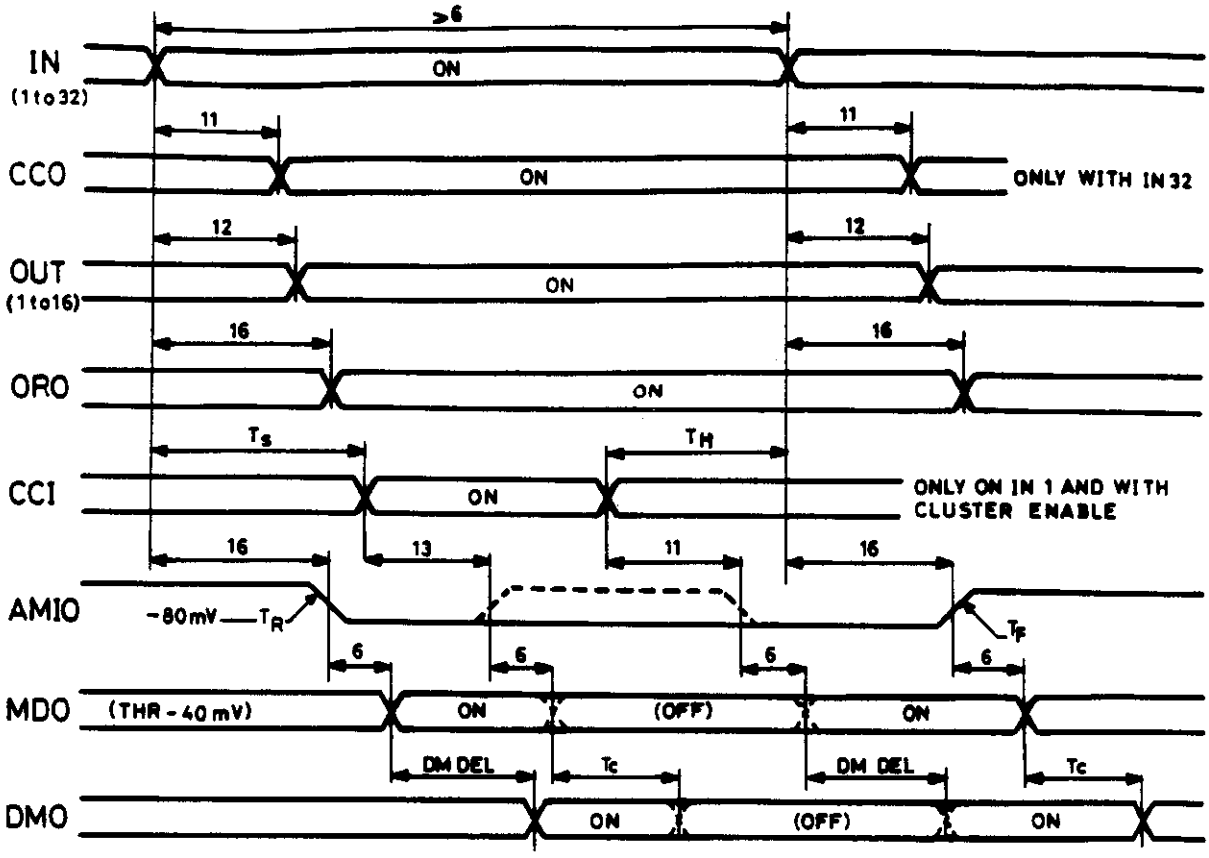
The second flip-flop, which is coupled to the first one, is set at the beginning of a CAMAC cycle if the L line is ON. It generates the Q response in recognition of F(8) and F(10).

In order to avoid loss of a LAM request coming during F(10), the reset by F(10) is halted if a Q response has not been delivered.



MODEL 4532 BLOCK DIAGRAM

MEMORY DISABLE TIMING (with GAI open)



All times in ns

T_s : Cluster disable set-up time, min. -2 nsec

T_h : Cluster disable hold time, min. 6 nsec

T_r : AMIO rise time < 6 nsec with amplitude of 1280 mV

T_f : AMIO fall time < 7 nsec with amplitude of 1280 mV

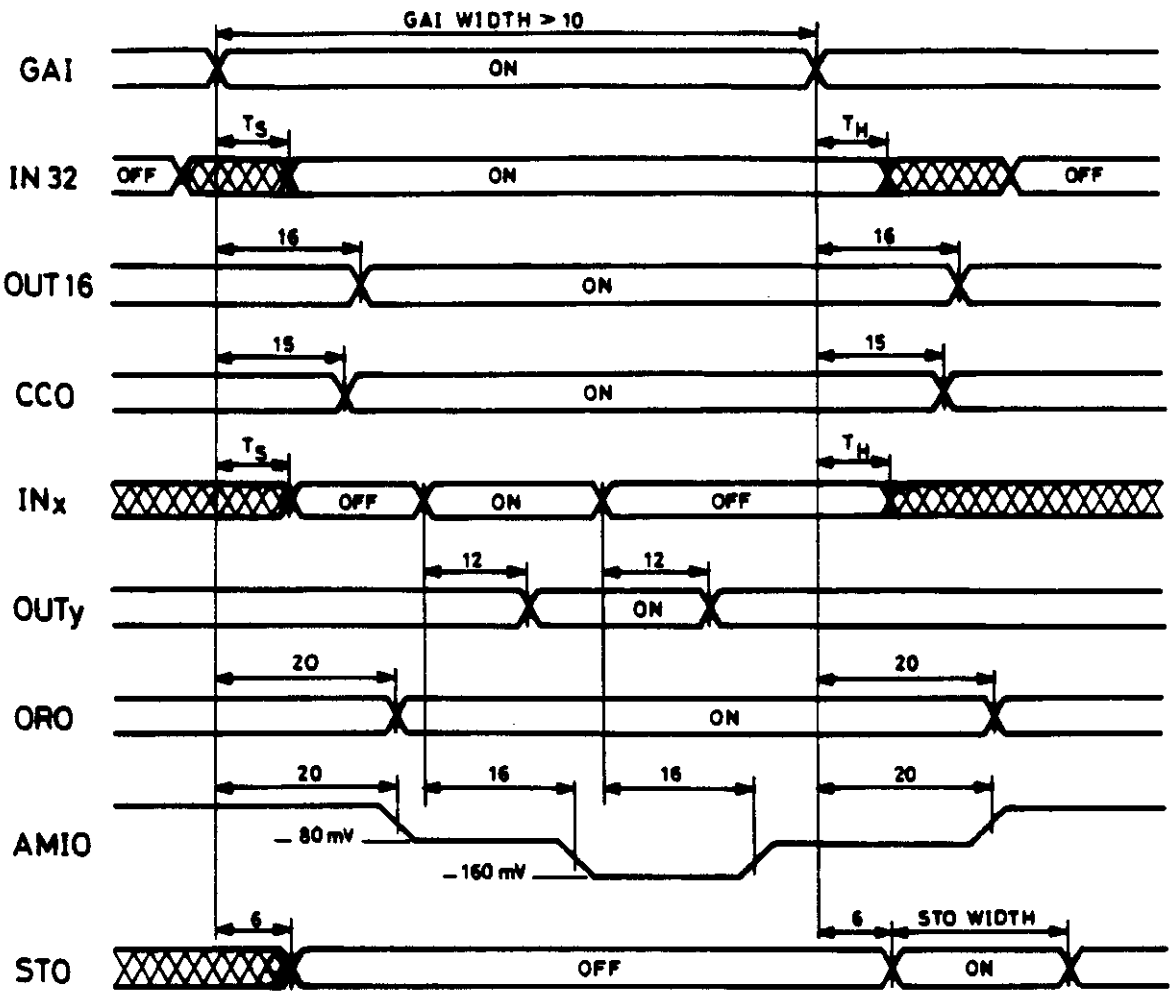
DMDEL : Adjustable from < 10 nsec to > 100 nsec

or from < 50 nsec to > 1 µ sec

T_c : DMO clear time: on range 100 nsec < 8 nsec

on range 1 µ sec < 16 nsec

MEMORY DISABLE TIMING



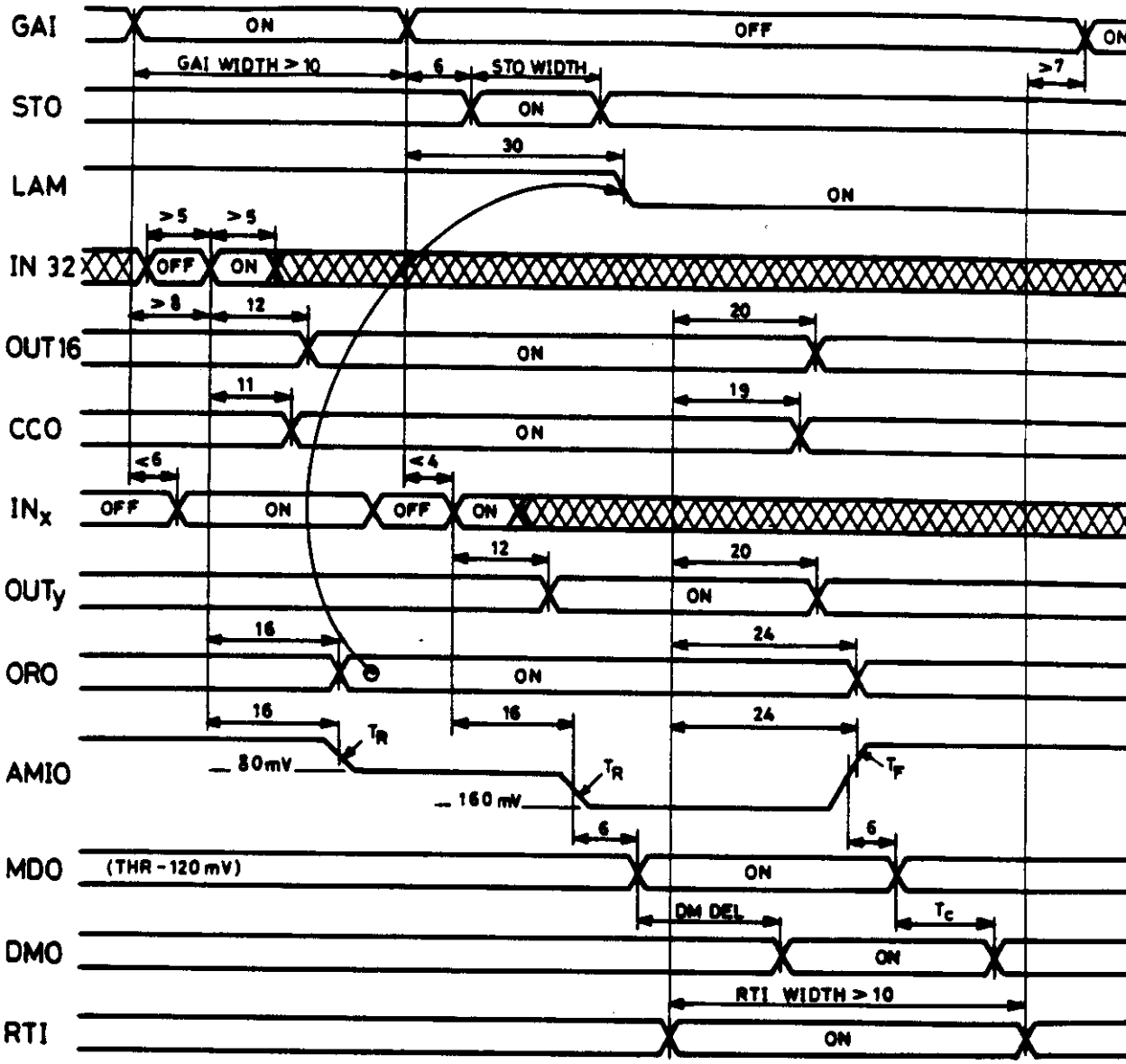
All times in nsec

T_s : GAI enable set-up time, min. 4 nsec

T_h : GAI disable hold time, min. 4 nsec

STO WIDTH : ADJUSTABLE FROM < 10 nsec to > 25 nsec

MEMORY ENABLE TIMING



All times in nsec

STO WIDTH : Adjustable from < 10 nsec to > 25 nsec

DM DEL : Adjustable from < 10 nsec to > 1 µsec

T_r : AMIO rise time < 6 nsec

T_f : AMIO fall time < 7 nsec with amplitude of 1280 mV

T_c : DMO clear time : on range 100 nsec < 8 nsec
on range 1 µsec < 16 nsec

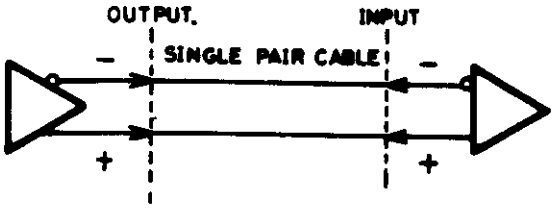
APPLICATION NOTE

In MEMORY ENABLE mode, several self triggering operations are possible by connecting the outputs ORO, STO, MDO, DMO with the inputs GAI and RTI.

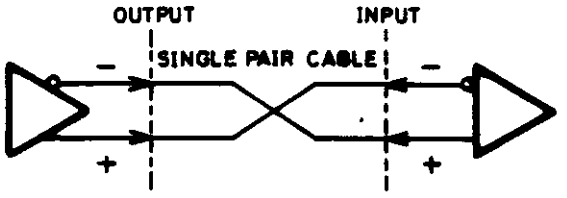
It should be noted that the RTI input can also be used as a gate. However the output signals are reset during the width of the signal applied on RTI.

Self Triggering can be done in two ways:

- Direct (example: RTI = MDO)

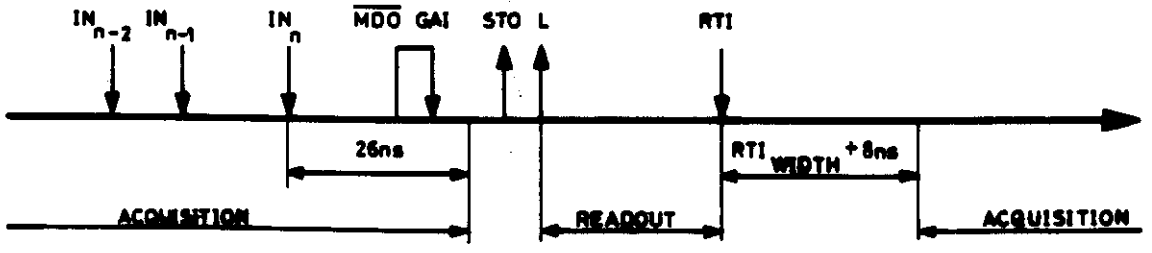


- Inverted (example: GAI = MDO)



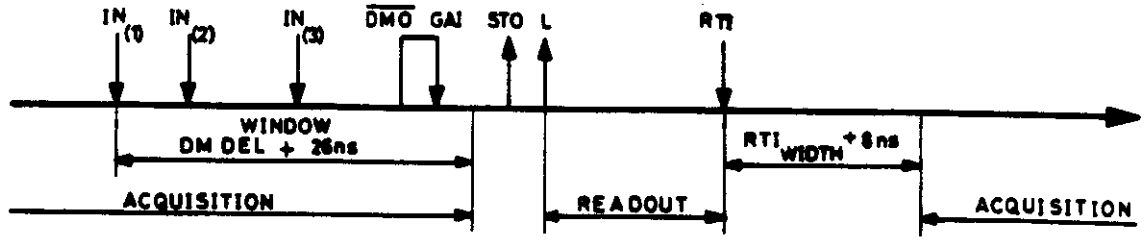
Application examples:

a) Start a CAMAC readout after reception of a given number n of inputs. The number n can be set from 1 to 16 adjusting the MATHR potentiometer. The GAI = MDO self triggering technique should be used, while RTI can be used as gate.

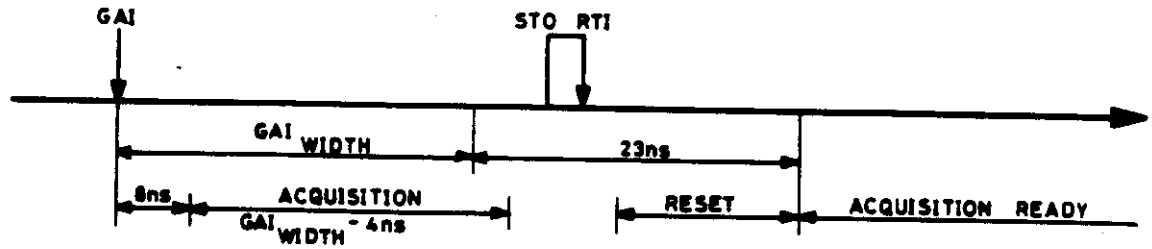


b) Start a CAMAC readout after a given time window of acceptance, where the time window is started by the first arriving input.

GAI = DMO should be used and the majority threshold (MA THR) set for n = 1. The first IN arriving will start the time window, while the width is established by DM DEL. RTI can again be used as gate.

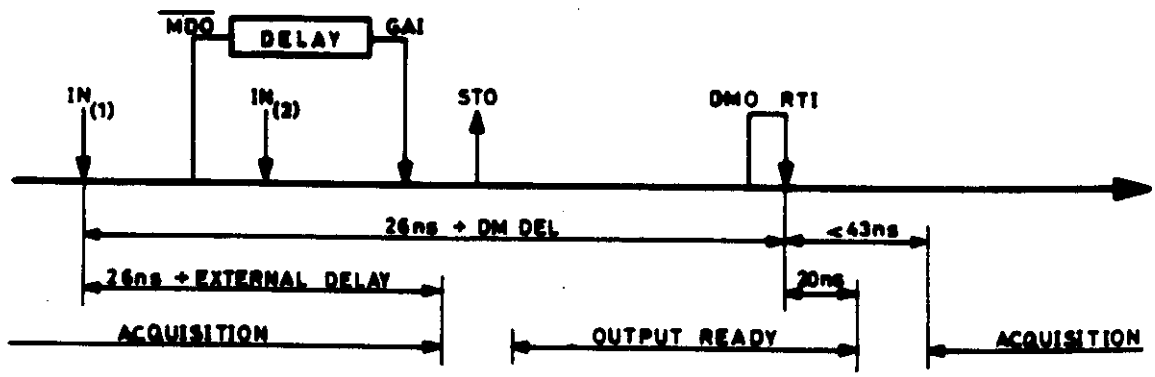


c) Automatic reset after a gate.
Let RTI = STO and adjust the STO width to 10 nsec.



d) Start a time window of acceptance by the first input signal; automatic reset after the time window.

MA THR should be set for n = 1 and GAI = MDO (or GAI = ORO) through a delay line. The reset will be executed by RTI = DMO with a delay adjustable by DM DEL.



OPTIONAL ACCESSORIES

ECL CABLES

Interconnections between different ECLine modules, for transmission of different ECL pulse pairs, can be made either by multiwire cables or by single twisted pair cables for one to one connections.

Such interconnecting cables may be purchased from LeCROY and in particular, as multiwire cables, two types are available; one for short connections using just flat cable, the second one for long interconnections using twisted and flat ribbon cable.

The notation for ordering these cables is as follows:

- STC-DC/34-LL Multiwire cable for short interconnections
- LTC-DC/34-LL Multiwire cable for long interconnections
- STP-DC/02-LL Single twisted pair cable

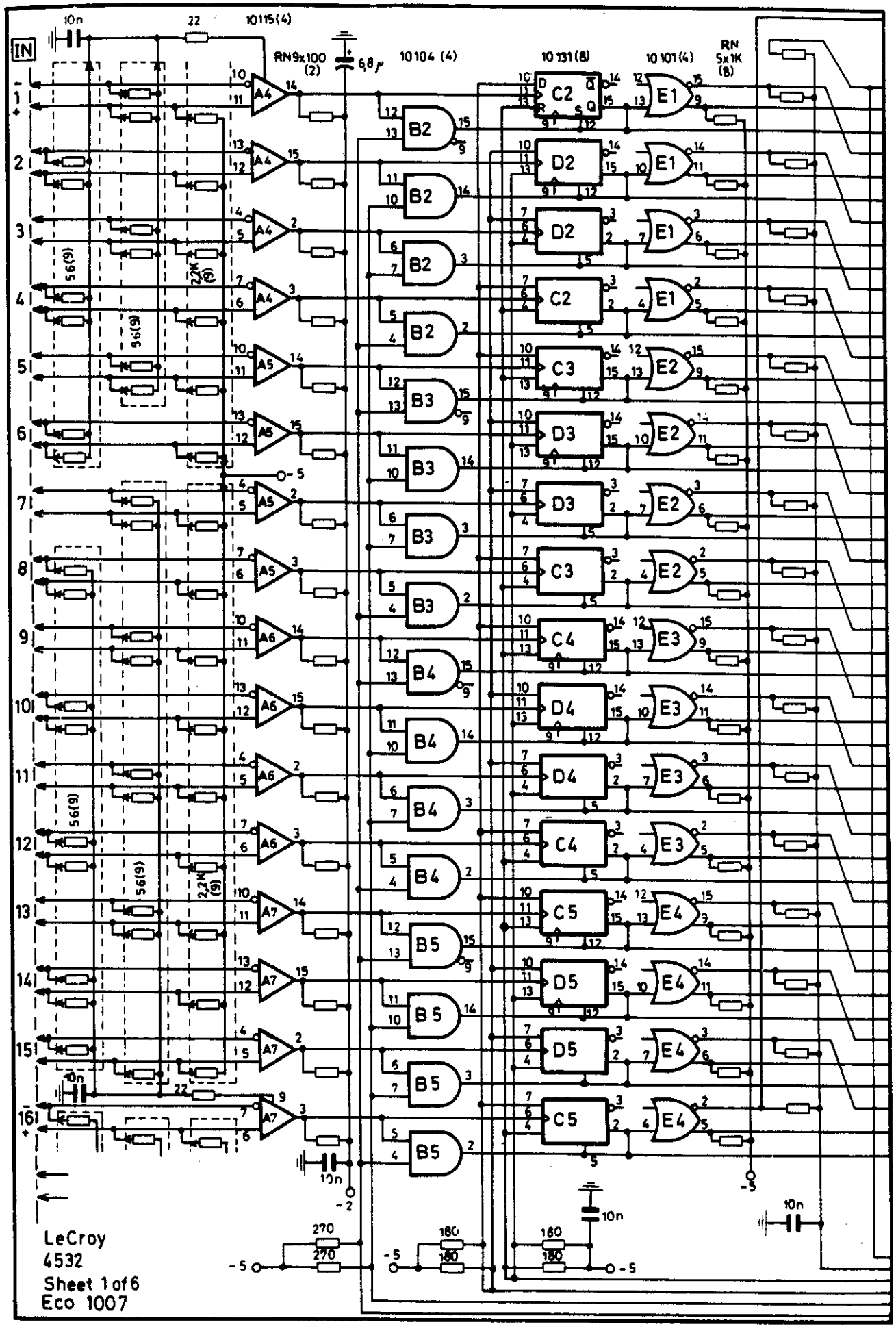
where LL is the cable length in feet which should be specified by the customer.

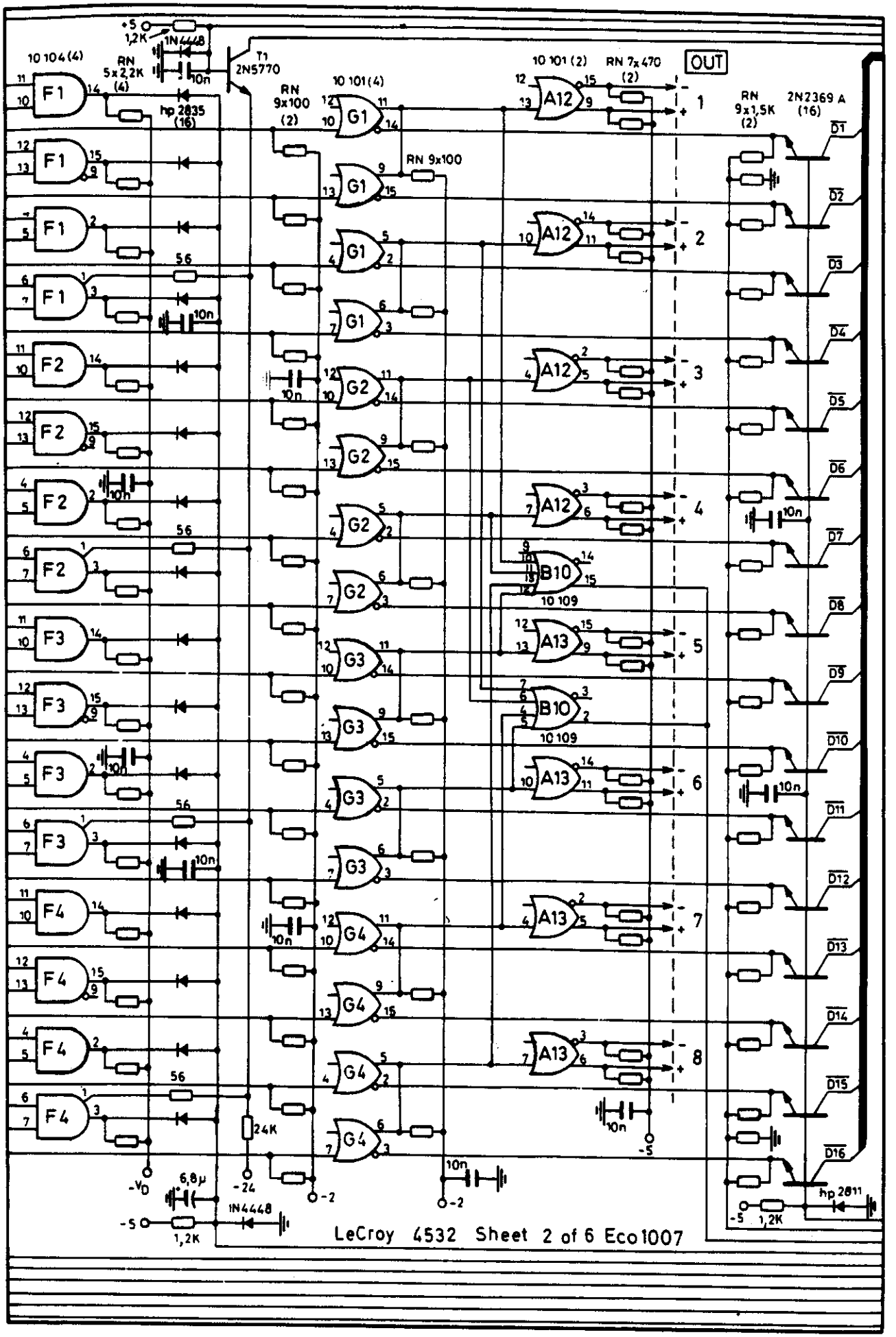
LECROY CORPORATION
4532 PARTS LIST

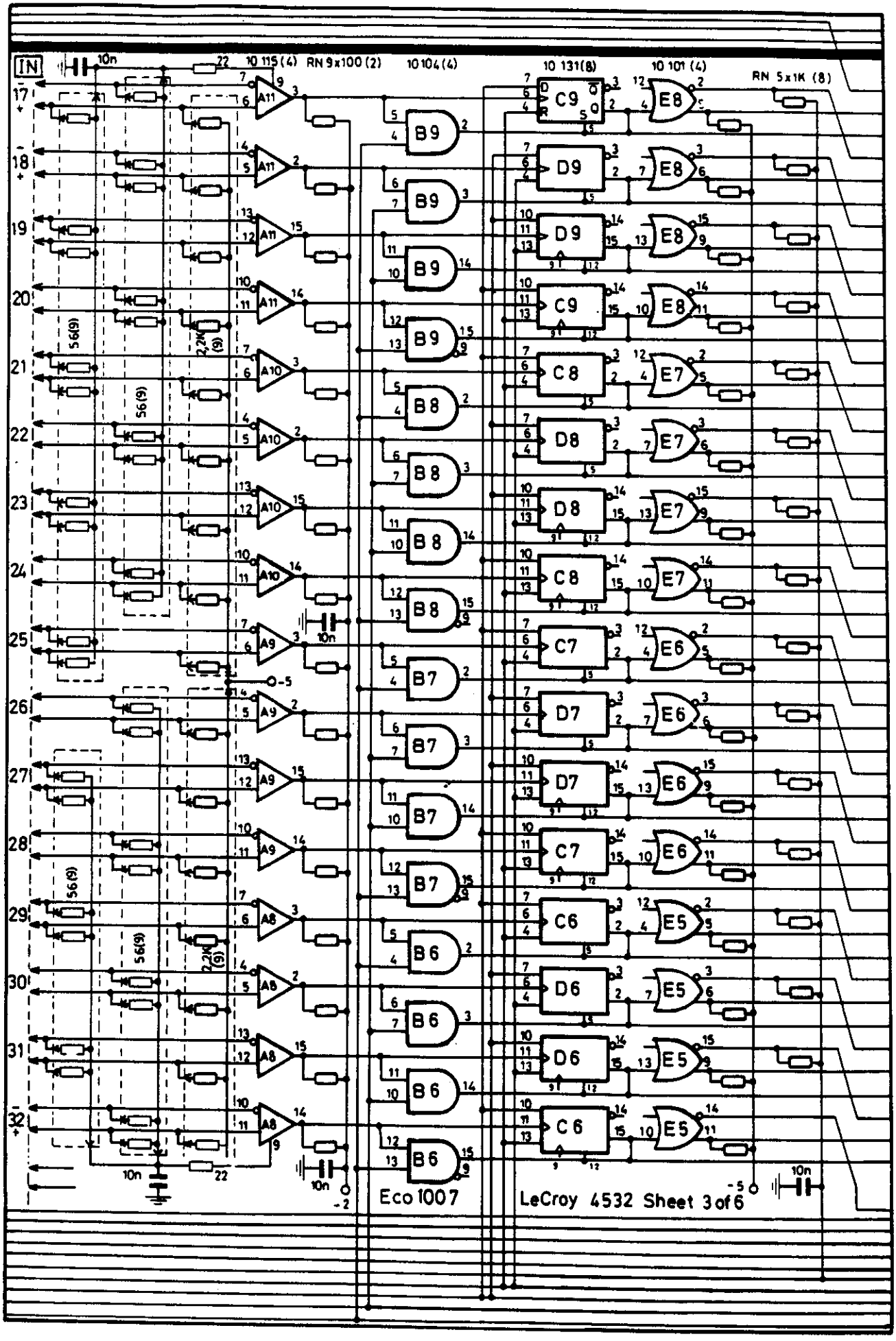
PART NUMBER	DESCRIPTION	QUANTITY PER
102412220	CAP CERA DISC 100V 22 PF	1
102412221	CAP CERA DISC 100V 220 PF	1
102412270	CAP CERA DISC 100V 27 PF	1
103327103	CAP CERA MONO 50V .01 UF	75
103427104	CAP CERA MONO 100V .1 UF	2
142824685	CAP TANT DIP CASE 6.8 UF	10
158819002	CAP VARI CERA 3.0 - 10 PF	1
158849006	CAP VARIABLE 7-45 PF	1
161225152	RES CARBON FILM 1.5 K	1
161225270	RES CARBON FILM 27 OHMS	1
161225393	RES CARBON FILM 39 K	1
161225472	RES CARBON FILM 4.7 K	1
161225560	RES CARBON FILM 56 OHMS	1
161225562	RES CARBON FILM 5.6 K	1
161335101	RES CARBON FILM 100 OHMS	1
161335102	RES CARBON FILM 1 K	21
161335121	RES CARBON FILM 120 OHMS	1
161335122	RES CARBON FILM 1.2 K	7
161335152	RES CARBON FILM 1.5 K	1
161335153	RES CARBON FILM 15 K	2
161335180	RES CARBON FILM 18 OHMS	1
161335181	RES CARBON FILM 180 OHMS	6
161335220	RES CARBON FILM 22 OHMS	4
161335222	RES CARBON FILM 2.2 K	3
161335223	RES CARBON FILM 22 K	1
161335243	RES CARBON FILM 24 K	2
161335271	RES CARBON FILM 270 OHMS	2
161335272	RES CARBON FILM 2.7 K	2
161335331	RES CARBON FILM 330 OHMS	2
161335390	RES CARBON FILM 39 OHMS	1
161335470	RES CARBON FILM 47 OHMS	1
161335472	RES CARBON FILM 4.7 K	4
161335560	RES CARBON FILM 56 OHMS	10
161335561	RES CARBON FILM 560 OHMS	5
161335821	RES CARBON FILM 820 OHMS	1
161335822	RES CARBON FILM 8.2 K	1
181457101	RES VARI CERMET 100 OHMS	1
181457102	RES VARI CERMET 1 K	1
181457202	RES VARI CERMET 2 K	1
182537102	RES VARI CERMET 1 K	2
190042101	RESISTOR NETWORK 100 OHMS	9
190042152	RESISTOR NETWORK 1.5 K	4
190042222	RESISTOR NETWORK 2.2 K	4
190042471	RESISTOR NETWORK 470 OHMS	2
190042560	RESISTOR NETWORK 56 OHMS	8
190042562	RESISTOR NETWORK 5.6 K	2
190642102	RESISTOR NETWORK 1 K	16
190642222	RESISTOR NETWORK 2.2 K	8
190642471	RESISTOR NETWORK 470 OHMS	2
190842101	RESISTOR NETWORK 100 OHMS	1
190842471	RESISTOR NETWORK 470 OHMS	2
200031032	IC HEX BUFF/DRIV SN7407N	3
200031033	IC 2-INPUT NAND SN7403N	2
200031035	IC J-K FLOP SN74S113N	1

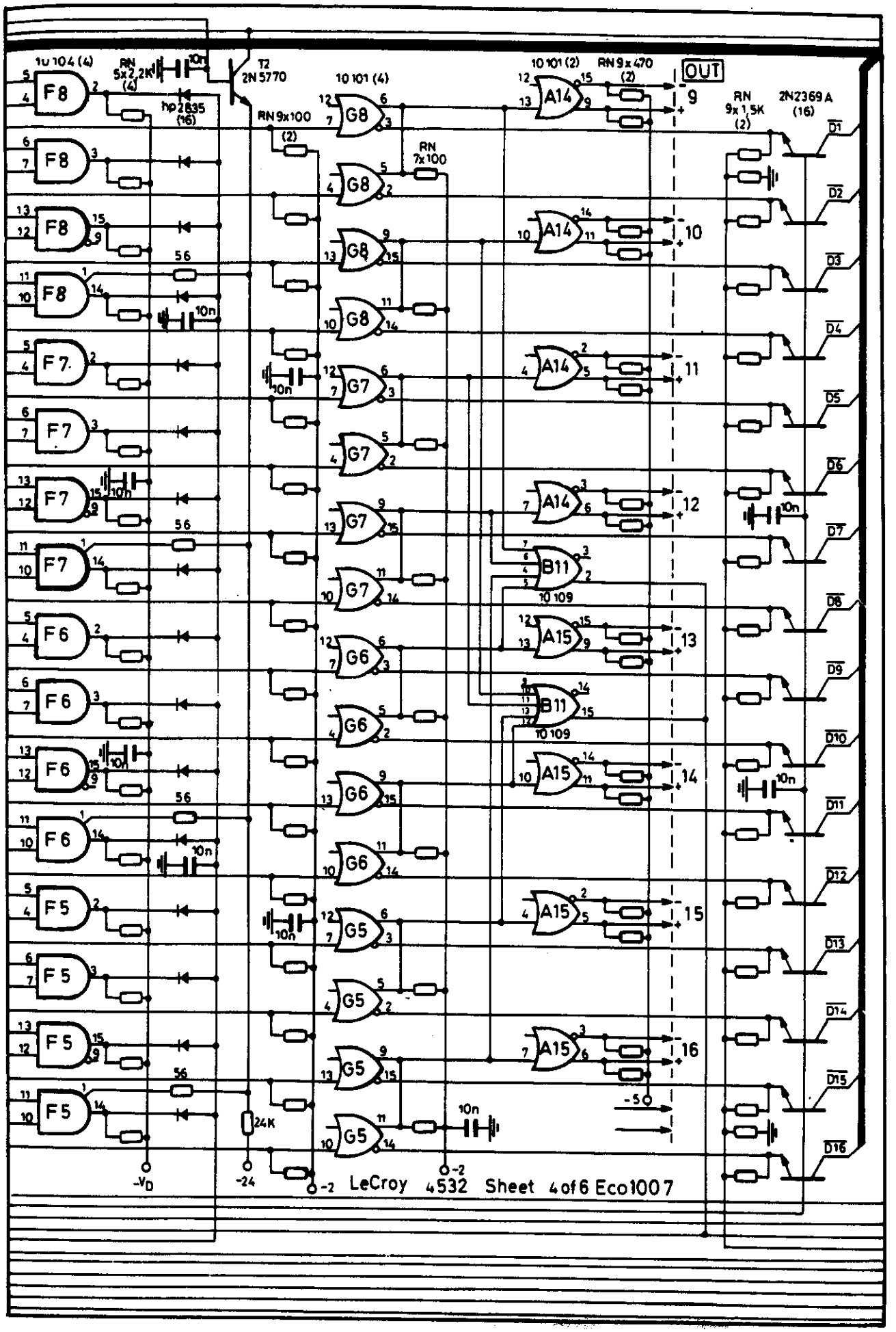
PART NUMBER	DESCRIPTION	QUANTITY PER
200031052	IC 8-INPUT NAND SN74LS30N	1
200031073	IC 2-IN POS OR SN74LS32N	1
200031077	IC 3-INPUT AND SN74LS11N	2
200031086	IC 2-INPUT AND SN74LS08N	1
200081004	IC DECODER/DEM DM74LS154N	1
204022003	IC DUAL A/D CONV MC1651L	1
204042001	IC 4-5 OR/NOR GT MC10109P	2
204042003	IC LINE RECEIVER MC10115P	9
204042005	IC TYP D FL-FL MC10131P	16
204042010	IC 3-IN 3-OUT OR MC10110P	1
204042012	IC 2-IN AND GATE MC10104P	17
204042016	IC 2-INPUT OR/NOR F10101P	21
208031004	IC PREC VOLT REG UA723C	1
208122337	IC ADJ -VOLT REG LM337T	1
230110005	DIODE SWITCHING 1N4448	8
235010005	DIODE RECTIFIER 1N4005	1
235050001	DIODE RECTIFIER 1N4139	1
253010811	DIODE SCHOTTKY BAR HP2811	1
253010835	DIODE HOT CARRIER HP2835	34
270110001	TRANSISTOR NPN PN2369A	38
270110003	TRANSISTOR NPN 2N2222A	1
270170001	TRANSISTOR NPN 2N5770	4
275170002	TRANSISTOR PNP 2N5771	10
300050001	CHOKE FERRITE SINGLE LEAD	4
402112001	CONN PC MTG LEMO NICKEL	2
403119234	HEADER RT ANGLE 34-PIN	3
405812002	SOCKET STRIP SOLDR 20 POS	6
419211001	SWITCH SLIDE DIP-MTG DPST	4
433220001	FUSE PICO II 125V 10 AMP	1
433221004	FUSE PICO II 125V 1 AMP	1
454310002	HDR DIP SOLD TO PC BD 2	7
454713016	HDR DIP SOLD TO MALE 16	1
468911001	TEST POINT (JACK) WHT	1
500460005	MOUNTING KIT FOR TO-220	1
521000004	SPACER HEX 2-56X.417	4
540206178	RAIL CAMAC STD BOT W/LIP	1
540209001	REAR PANEL CAMAC SIZE #1	1
555430003	CAPTIVE SCREW ASSEMBLY	1
560256005	SCREW PHILIPS 2-56X5/16	4
560440003	SCREW PHILIPS 4-40X3/16	4
560440006	SCREW PHILIPS 4-40X3/8	4
564440004	SCREW ROUND PHIL 4-40X1/4	2
567440006	SCREW FLAT PHIL 4-40X3/8	2
568256002	SCREW FLAT PHIL 2-56X1/8	4
593910001	CABLE CO-AXIAL RG178B/U	1
704532001	RAIL CAMAC TOP 4532	1
714532003	PC BD PREASS'Y 4532	1
724532003	FRONT PNL PREASSY 4532	1
734532003	SIDE ECLINE LEFT 4532	1
734532005	SIDE CAMAC RIGHT 4532	1

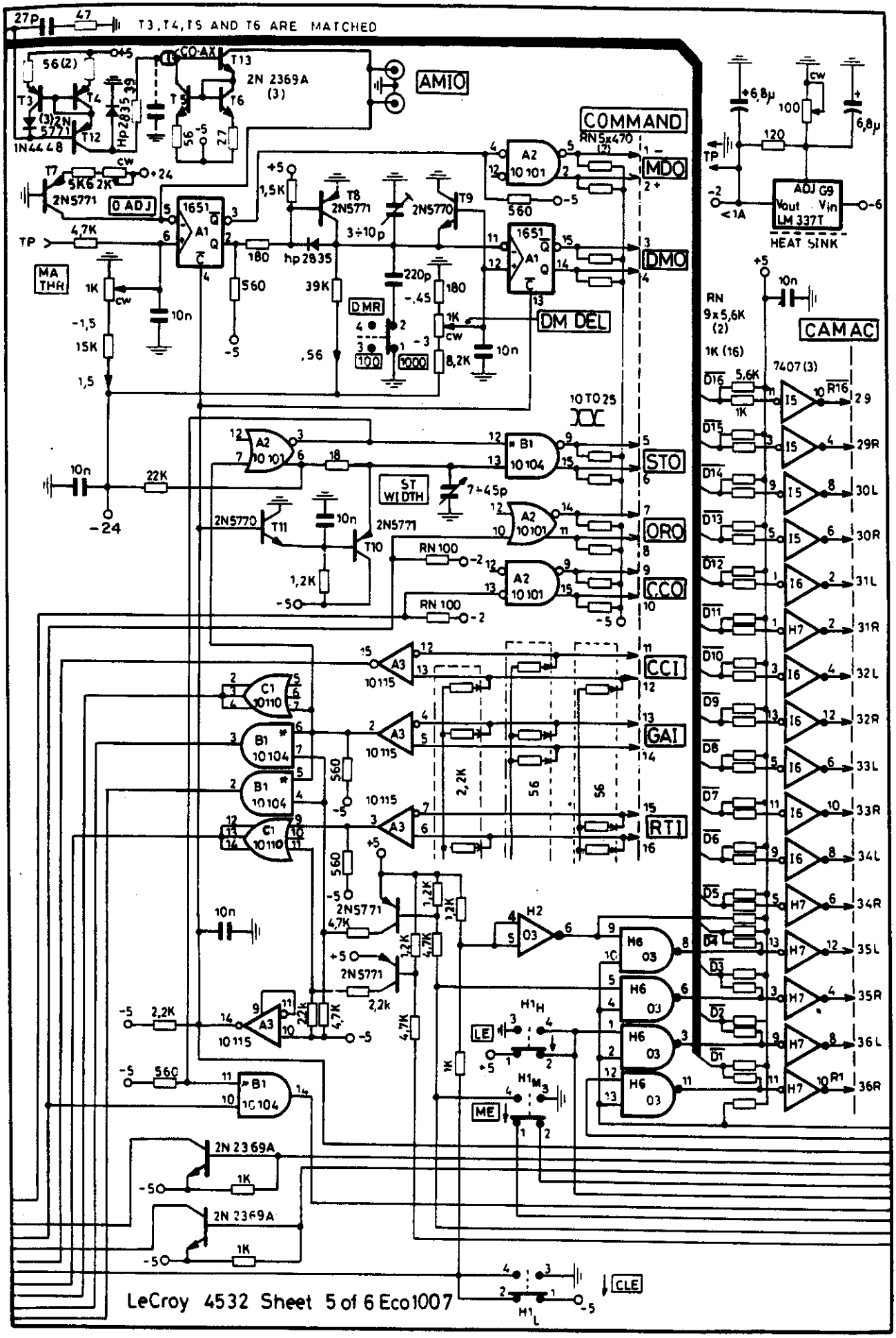
End of report. 104 Details encountered.

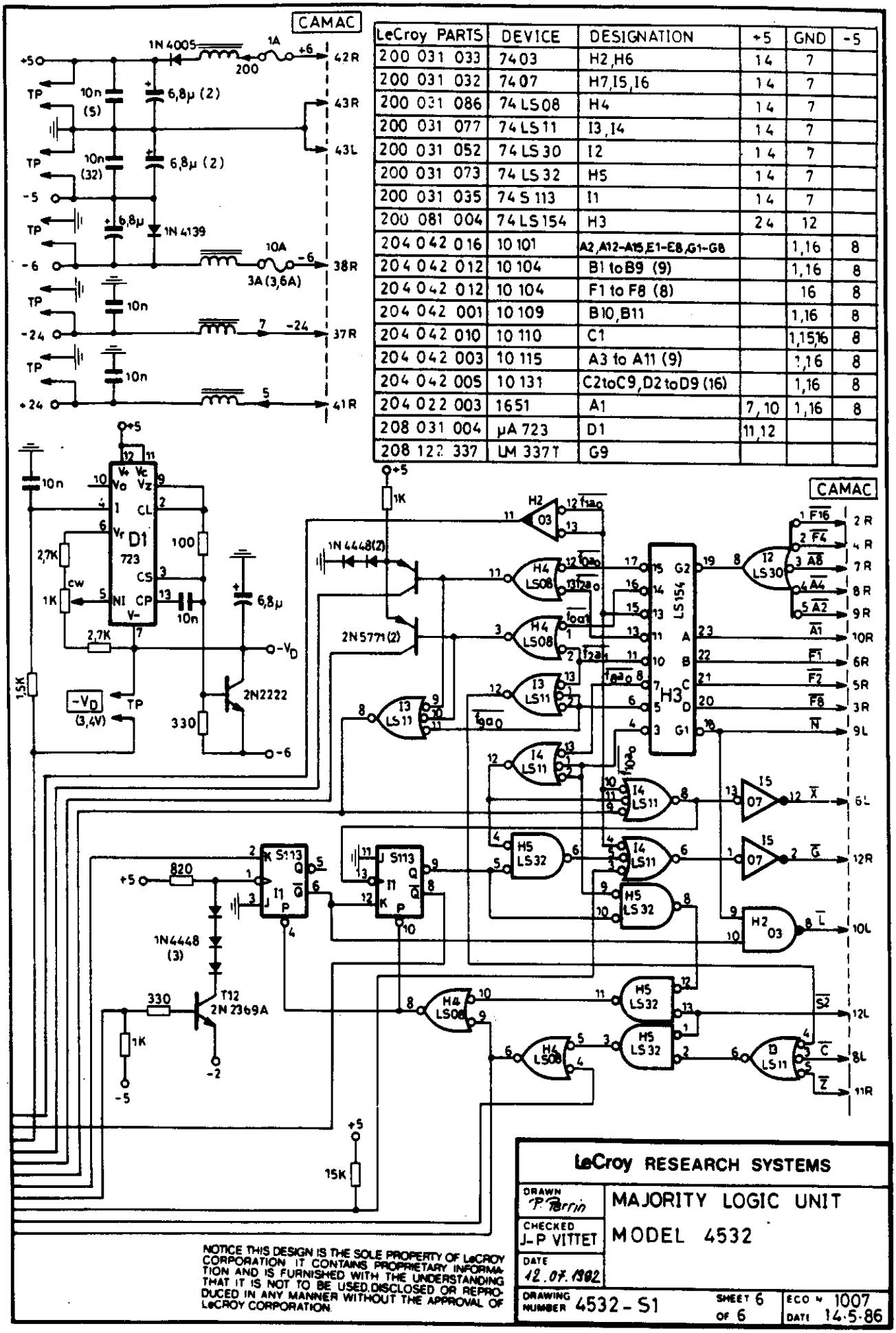

IN
10n
22
10115 (4)
RN9x100 (2)
6,8 µ
10104 (4)
10131 (8)
10101 (4)
RN 5x1K (8)
A4
A5
A6
A7
B2
B3
B4
B5
C2
C3
C4
C5
D2
D3
D4
D5
E1
E2
E3
E4
56(9)
2,2K (9)
270
180
-5
-2
LeCroy
4532
Sheet 1 of 6
Eco 1007


10 104 (4)
RN 5x2,2K (4)
+5
1,2K
1N4448
10n
T1 2N5770
hp 2835 (16)
F1
F2
F3
F4
56
10 101 (4)
RN 9x100 (2)
G1
G2
G3
G4
RN 9x100
24K
-V0
6,8µ
-24
-2
-5
10 101 (2)
RN 7x470 (2)
A12
A13
B10
10 109
OUT
1
2
3
4
5
6
7
8
RN 9x1,5K (2)
2N2369 A (16)
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
hp 2811
LeCroy 4532 Sheet 2 of 6 Eco1007


IN
10n
22
10 115 (4)
RN 9x100 (2)
10 104 (4)
10 131 (8)
10 101 (4)
RN 5x1K (8)
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
56(9)
2.2K (9)
A11
A10
A9
A8
B9
B8
B7
B6
C9
C8
C7
C6
D9
D8
D7
D6
E8
E7
E6
E5
-5
-2
Eco 1007
LeCroy 4532 Sheet 3 of 6


1u 104 (4)
RN 5x2,2K (4)
10n
T2 2N5770
hp2835 (16)
RN 9x100 (2)
10 101 (4)
RN 7x100
10 101 (2)
RN 9x470 (2)
OUT
RN 9x1,5K (2)
2N2369A (16)
F8
F7
F6
F5
G8
G7
G6
G5
A14
A15
B11
10 109
56
10n
24K
-5
-2
-24
-VD
LeCroy 4532 Sheet 4of6 Eco1007


T3,T4,T5 AND T6 ARE MATCHED
AMIO
COMMAND
MDO
DMO
DM DEL
STO
ORO
CCO
CCI
GAI
RTI
CAMAC
HEAT SINK
ADJ G9 Vout Vin LM 337T
0 ADJ
MA THR
DMR
ST WIDTH
10 TO 25
LE
ME
CLE
LeCroy 4532 Sheet 5 of 6 Eco1007



LeCroy PARTS	DEVICE	DESIGNATION	+5	GND	-5
200 031 033	7403	H2,H6	14	7	
200 031 032	7407	H7,I5,I6	14	7	
200 031 086	74LS08	H4	14	7	
200 031 077	74LS11	I3,I4	14	7	
200 031 052	74LS30	I2	14	7	
200 031 073	74LS32	H5	14	7	
200 031 035	74S113	I1	14	7	
200 081 004	74LS154	H3	24	12	
204 042 016	10 101	A2,A12-A15,E1-E8,G1-G8		1,16	8
204 042 012	10 104	B1 to B9 (9)		1,16	8
204 042 012	10 104	F1 to F8 (8)		16	8
204 042 001	10 109	B10,B11		1,16	8
204 042 010	10 110	C1		1,15,16	8
204 042 003	10 115	A3 to A11 (9)		1,16	8
204 042 005	10 131	C2 to C9, D2 to D9 (16)		1,16	8
204 022 003	1651	A1	7,10	1,16	8
208 031 004	µA 723	D1	11,12		
208 122 337	LM 337T	G9			

LeCroy RESEARCH SYSTEMS

DRAWN P. Perrin	MAJORITY LOGIC UNIT
CHECKED J-P VITTET	MODEL 4532
DATE 12.07.1982	
DRAWING NUMBER 4532 - S1	SHEET 6 OF 6
ECO N 1007	DATE 14-5-86