

Lecroy

NIM MODEL 465/466
TRIPLE 4-FOLD
COINCIDENCE UNITS

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A T T E N T I O N

SEE POCKET IN BACK OF MANUAL FOR
SCHEMATICS, PARTS LISTS, AND ADDITIONAL
ADDENDA WITH ANY CHANGES TO MANUAL.

A T T E N T I O N

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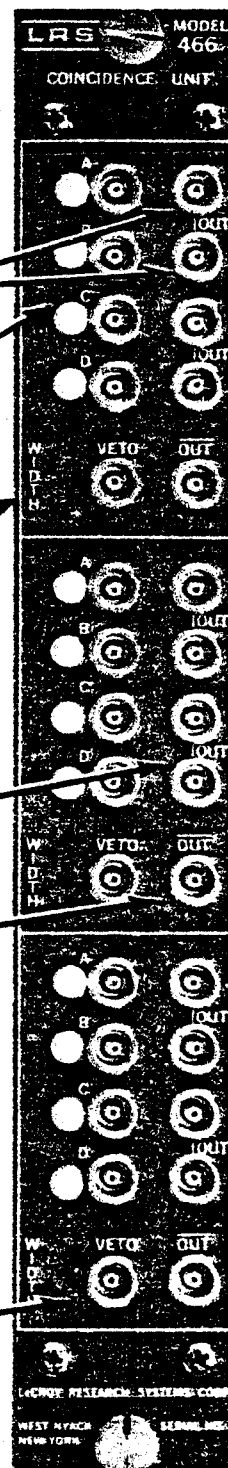
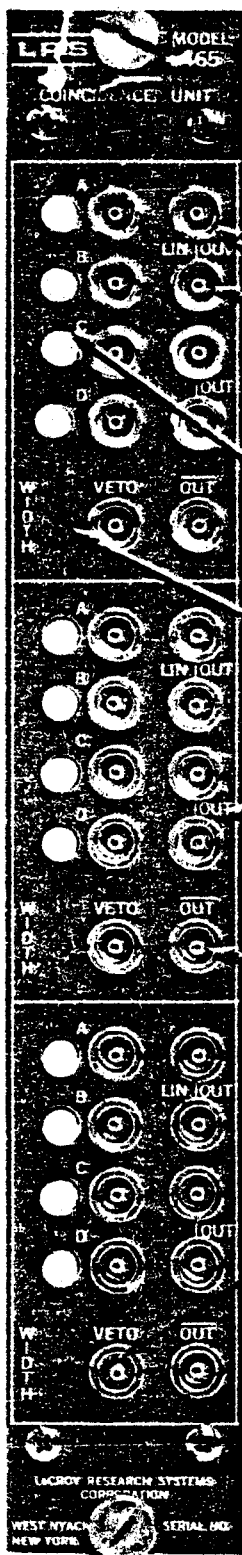
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Drafting Symbols

Schematics

NIM Model 465/466 Triple 4-Fold Coincidence Units



Linear output bridged pair.
Fast NIM output*. Duration =
input overlap duration.

Input Select Buttons
in = select
out = defeat

Width Adjust
<5 nsec to >500 nsec

Preset Output
NIM output* bridged pair.
Duration determined by
setting of width pot.

Complementary Output
(-16 mA quiescently; 0 mA during
pulse). Duration determined
by setting of width pot.

50 Ω ; > -600 mV input.
Veto must overlap
entire coincidence
interval.

50 Ω ; > -600 mV input.
Veto need overlap
leading edge of coinci-
dence only.

NIM Model 465

Triple 4-Fold Logic Unit WITH VETO

The LRS Model 465 contains three independent high-speed general-purpose coincidence units in a single-width NIM module. Each channel has four coincidence inputs and a separate veto input which accept standard negative NIM logic levels. The logic inputs may be individually enabled or disabled without altering input cabling or termination by means of front-panel pushbutton switches. With all inputs enabled, four inputs are required. Disabling the logic inputs is equivalent to reducing the number of simultaneous negative inputs required for an output. Thus, each channel may be programmed for 4-fold, 3-fold, or 2-fold logic decisions. With only one input enabled, each channel of the 465 operates as a logic fan-out.

Once triggered by signals satisfying the input coincidence requirements, the 465 generates five NIM fast logic outputs: one pair of -32 mA negative preset outputs, one -16 mA preset complementary output, and one pair of -32 mA overlap outputs. The preset outputs are continuously adjustable from less than 5 ns to greater than 500 ns by means of a front-panel multiturn potentiometer and are independent of input overlap time, amplitude, and rate. Because it is updating, it may be retriggered even before the end of an output pulse that is already present. The overlap outputs are equal in duration to the coincidence overlap and produce outputs up to the maximum input rate capability.

The front-panel fast veto input accepts standard negative NIM-level pulses. To veto the linear outputs, the veto signal must completely overlap any input coincidence; to veto the preset outputs, a prompt overlap of the leading edge of the input signal that would otherwise create the coincidence condition is required. A rear-panel bin-gate switch permits a slower (50 ns response time) inhibiting of the 465 by a clamp to ground from +4 volts through the bin gate pin of the rear power connector.

The Model 465 is packaged in a standard AEC/NIM #1 module (AEC Report TID-20893) and uses exclusively Lemo-type front panel connectors.

December 1975

Innovators in Instrumentation

SPECIFICATIONS

NIM Model 465

TRIPLE 4-FOLD LOGIC UNIT

INPUT CHARACTERISTICS

- Logic Inputs: 4; Lemo-type connectors; 50Ω impedance; negative NIM-level input requirements; each input can be separately enabled or disabled by front-panel push-buttons.
- Veto Input: Standard negative NIM-level signal, 3.5 ns minimum width. Requires complete overlap of input coincidence for linear outputs and prompt overlap of the leading edge of the input signal that would otherwise create the coincidence condition for the preset outputs. (Veto should precede this leading edge by approximately 5 ns in this case.)
- Bin Gate: Via rear connector; clamp to ground from +4 volts inhibits; risetimes and fall-times < 50 ns.

OUTPUT CHARACTERISTICS

- Preset Outputs: 3; one dual negative (quiescently 0 mA, -32 mA during output), one positive (quiescently -16 mA, 0 mA during output). Updating.
- Overlap Outputs: One dual negative; quiescently 0 volts, -32 mA during output; duration equal to coincidence overlap. Non-updating.
- Fan-Out: 5-fold, if each output drives a 50Ω load.
- Duration: Continuously adjustable from less than 5 ns to greater than 500 ns by means of front-panel, screwdriver-adjustable potentiometer. Width stability: better than $\pm 0.2\%/^{\circ}\text{C}$ maximum.
- Output Risetimes:*
OUT: ≤ 2.0 ns typical (max. 2.2 ns).
 $\overline{\text{OUT}}$: ≤ 2.2 ns typical (max. 2.5 ns; 3.0 ns with negative output unterminated).
- Output Falltimes:*
OUT: ≤ 2.0 ns typical (max. 2.5 ns). Slightly longer on wide output durations.
OUT: ≤ 2.2 ns typical (max. 2.5 ns). Slightly longer on wide output durations.

GENERAL

- Logic: 2-fold, 3-fold, or 4-fold coincidences plus fan-out determined by selectively disabling logic input.
- Coincidence Width: 1 ns up, determined by input pulse durations.
- Rate: 120 MHz minimum.
- Input-Output Delay: 13 ns preset; 8.5 ns linear.
- Multiple-Pulsing: None; one and only one output pulse of preset duration is produced each time the input conditions are satisfied regardless of the duration of the input pulses or their overlap.
- Double-Pulse Resolution: 8 ns.
- Packaging: Single-width AEC/NIM module; in conformance with AEC standard; Lemo-type connectors used for all inputs and outputs.
- Current Requirements: +12 V at 65 mA +6 V at 125 mA -24 V at 5 mA
-12 V at 135 mA -6 V at 640 mA

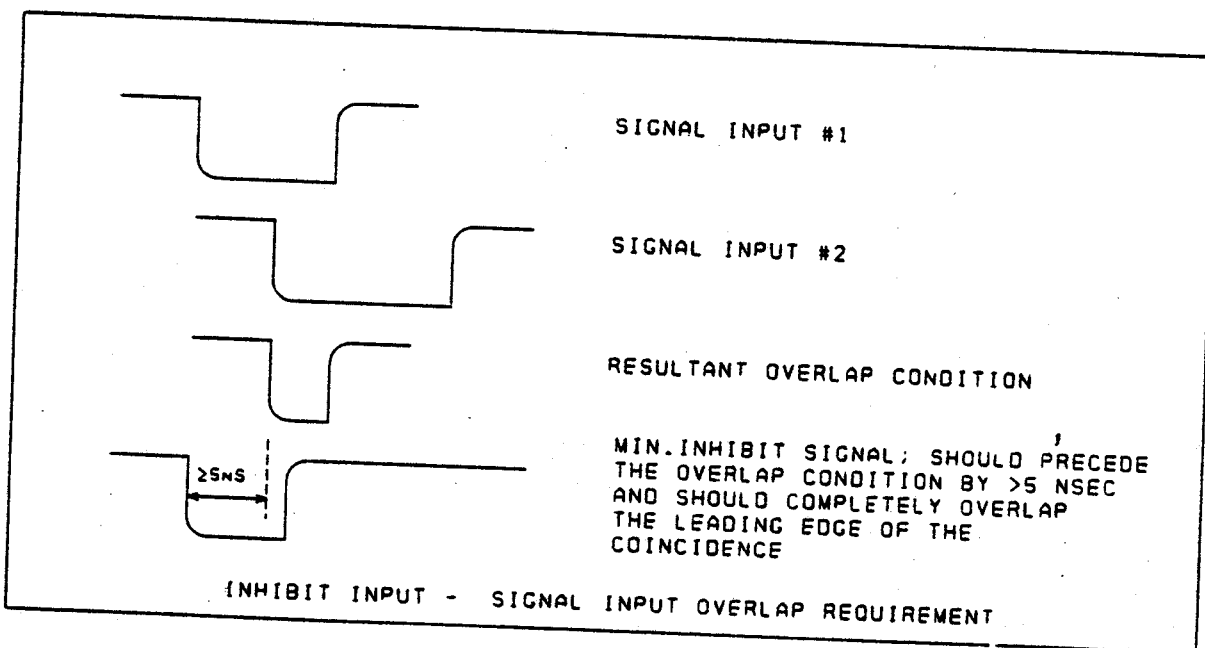
* -100 mV to -700 mV.

OPERATION

INPUT CHARACTERISTICS

Logic Inputs: The Models 465/466 have direct-coupled, 50Ω impedance inputs which accept fast NIM logic signals (-0.6 V to -1.8 V). These inputs, typically driven from a discriminator or other logic unit, are protected both for transient and DC signals up to ± 5 volts. Since the input reflections are less than 7% for signals of as little as 2 nsec risetime, even the maximum level signal in the NIM-specified range for a logic input (i.e. -1.8 volts) will reflect only approximately 125 mV, eliminating the probability of accepting multiple pulses corresponding to only one original input pulse.

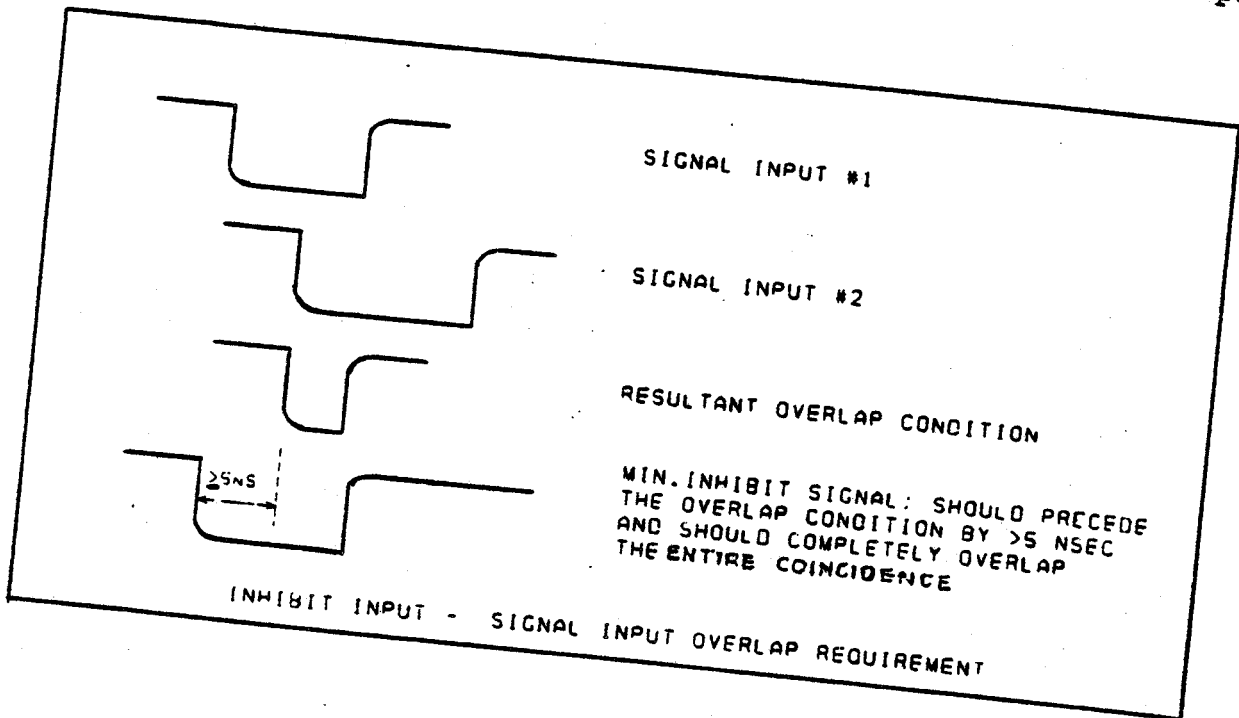
Model 466 Veto Inputs: The veto inputs of the Model 466 require NIM logical one input signals as described above. In order to inhibit (veto) a coincidence, the applied veto pulse must overlap the leading edge of the input signal that would otherwise cause the coincidence condition. Due to internal delays, the leading edge of the veto signal should precede the coincidence condition by at least 5 nsec. Consider the diagram below.



OPERATION

Model 465: Veto Input (for preset outputs only): The veto inputs of the Model 465 require NIM logical one input signals (ie, >-600 mV into 50Ω). In order to inhibit (veto) a coincidence, the applied veto pulse must overlap the leading edge of the input signal that would otherwise cause the coincidence condition. See description and associated diagram in preceeding section (Model 466: Veto Inputs).

Model 465: Veto Input (for linear outputs only): The veto inputs of the Model 465 require NIM logical one input signals as described above. In order to inhibit (veto) a coincidence, the applied veto pulse must overlap the entire coincidence condition as shown in the diagram below. This requirement is necessary since this linear output is determined only by the output of the front end of the logic unit, as opposed to the preset outputs where the leading edge of the front end output triggers a preset width stage. In the latter case, if the leading edge is vetoed, the entire preset width output stage never sees it, thereby preventing any preset output. In the case of the linear outputs, any portion of the front end output that is not specifically overlapped by the veto pulse will appear at the linear output connectors.



INHIBIT INPUT - SIGNAL INPUT OVERLAP REQUIREMENT

OPERATION

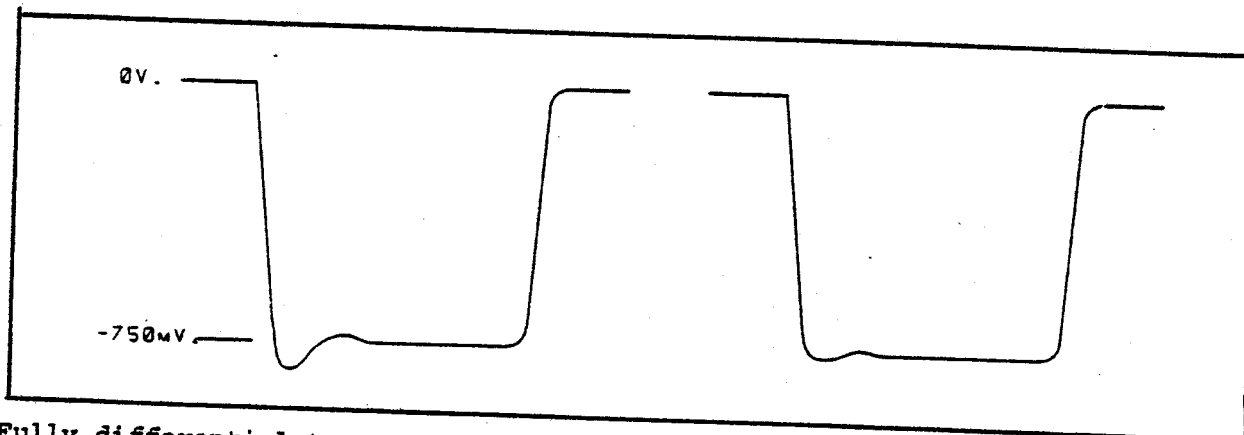
Inputs Select Switches: Any input will be removed from the coincidence requirement without removing its cable if the adjacent "Input Select Button" is in the OUT position.

Usage of 465/466 as a Triple 5-Fold Coincidence: In order to use the 465 or 466 as a 5-fold coincidence unit, a complementary fast NIM signal may be applied to the veto input. This signal will quiescently, then, hold the 465/466 in an off condition. When a pulse is applied to this input, it permits the 465/466 to give an output if the other selected inputs are in coincidence. Such application for the 465 and 466 is possible only at the sacrifice of usage of the veto input for a true inhibiting function.

OUTPUT CHARACTERISTICS

Bridged Negative Outputs: The Models 465 and 466 have two pairs of current source 50Ω outputs, delivering -32 mA of current during the output and 0 mA quiescently. These outputs are fully differential type current source outputs. These outputs maintain a risetime of approximately 2.0 nsec and a reasonably clean shape, as long as care is taken to terminate at least one half of the other bridged output in that channel.

The actual shape of typical outputs from the 465 and 466 is approximated below.

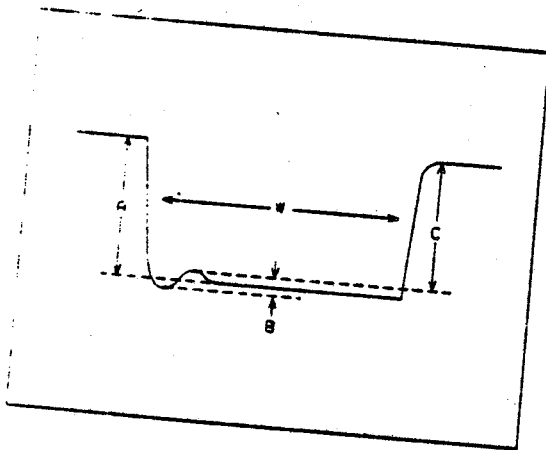


Fully differential type current source output, adjacent output pair unterminated; $tr \approx 2.5 \text{ nsec}$; overshoot $<15\%$.

Fully differential type current source output, output pair terminated; $tr \approx 2.0 \text{ nsec}$; overshoot $<10\%$.

OPERATION

Using the typical output pulse shape following as a visual reference, LRS output shapes for the fully differential type preset outputs on the 465 and 466 are set up to adhere to the following restrictions, with adjacent output pair terminated into 50 Ω :



- AMPLITUDE: $-700\text{mV} < A < -850\text{mV}$.
- OVERSHOOT: $B < 10\%$ OF A; C DOES NOT REACH -600mV
- RISETIME: $< 2.5 \text{ NSEC}$.
- FALLTIME: $< 2.5 \text{ NSEC}$. AT MINIMUM WIDTH.
- MINIMUM WIDTH: $W_{\text{MIN}} \text{ (FWHM)} < 5.0 \text{ NSEC}$.
- MAXIMUM WIDTH: $W_{\text{MAX}} \text{ (FWHM)} = 1 \text{ USEC}$.

Complementary Output: The single complementary output is actually the output from the collector of the other half of the differential pair supplying current to one pair of preset outputs. Although it is internally a double amplitude signal, it is subsequently internally back-terminated into 50 Ω , thereby maintaining a quiescent level of -16 mA, and logical 1 of 0 mA. Risetime and other characteristics are similar to that of the normal outputs.

Usage of Bridged Negative Outputs Driving a Single Cable: In applications where it is necessary to drive very long cable lengths from a logic unit output, it is common to use only one half of the bridged 32 mA output and to leave the other half unterminated. This effectively sends all 32 mA into one cable, giving nearly a double amplitude output. It is important to know that the 465 and 466 have clamp diodes that limit the output amplitude so as not to saturate the output transistors. This limit is approximately -1.4 volts. It cannot be assumed, therefore, that the -32 mA into one 50-ohm cable will give a -1.6 volt output signal.

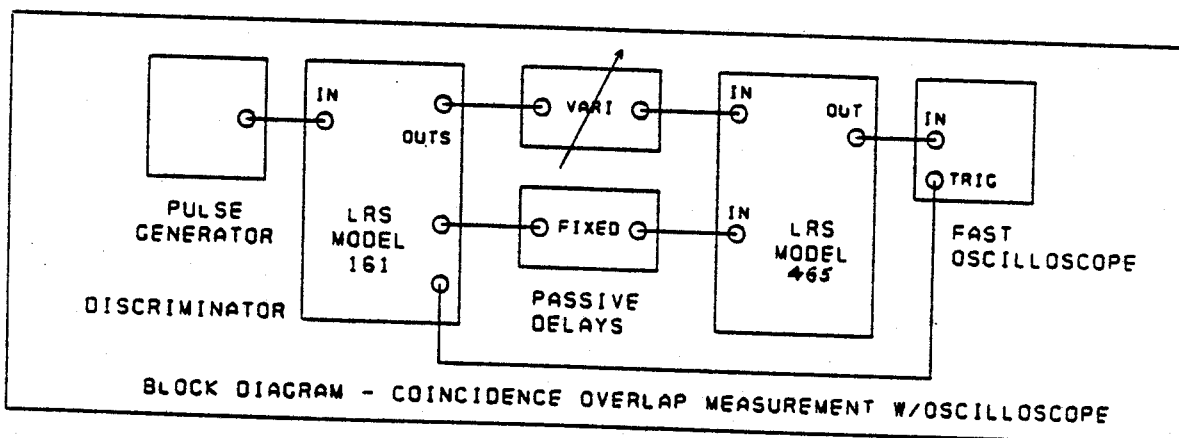
OPERATION

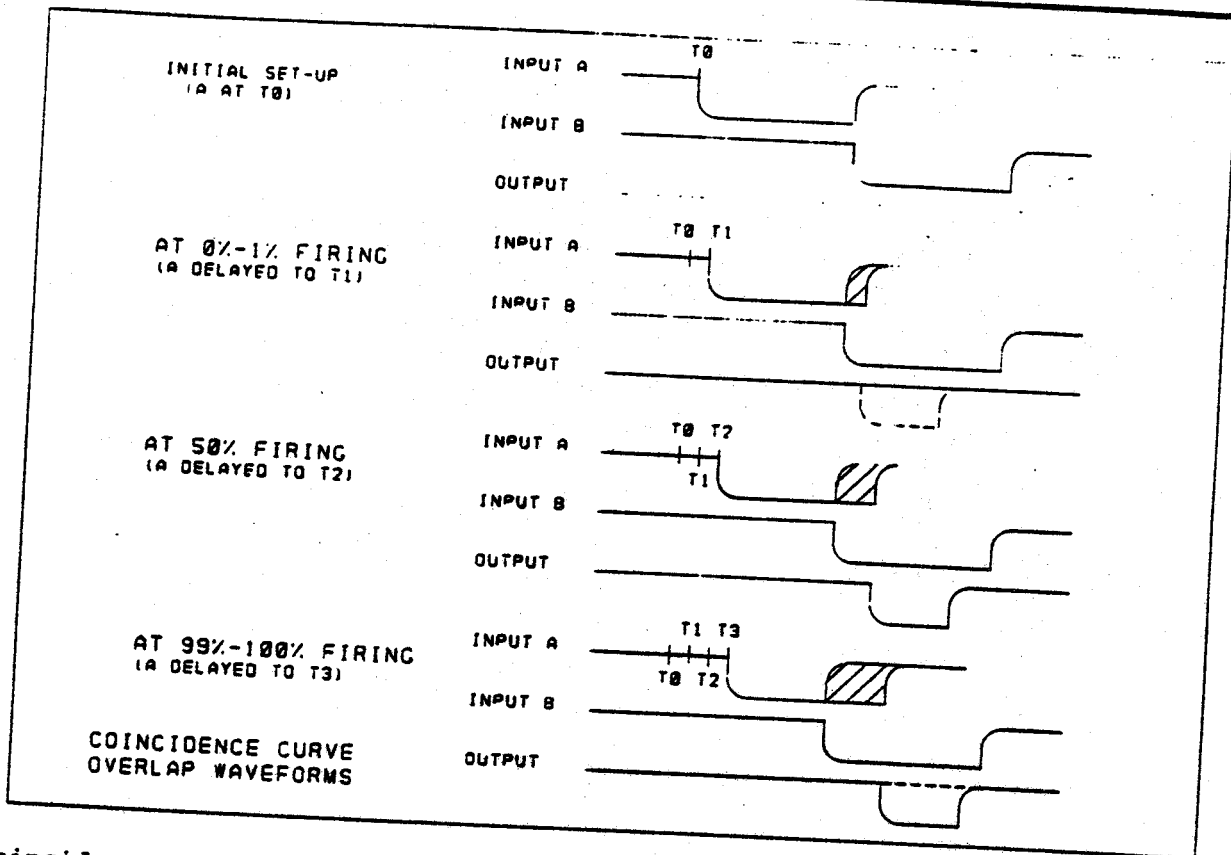
GENERAL

Coincidence Characteristics

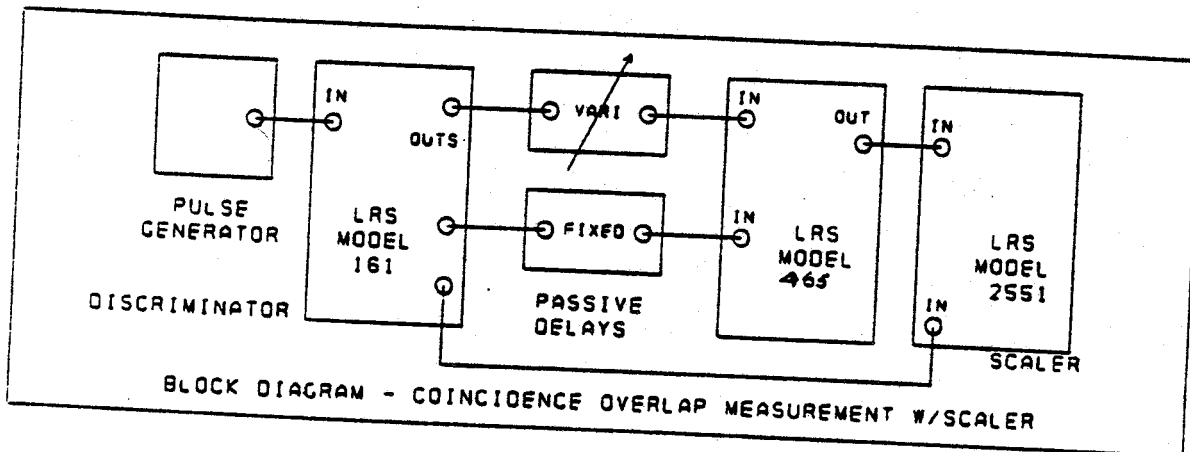
Minimum Coincidence Overlap (Coincidence Resolving Time): The required coincidence overlap time of two input signals on the 465/466 is approximately nsec. Although this measurement should be made with two pulses of zero risetime for an absolute result, functionally, no discriminator or other logic unit driving the 465/466 could output such fast pulses. The measurements on the 465/466 were therefore made with an LRS Model 161 Dual Discriminator of 1.5 nsec risetime and faltime.

One method used at LRS is to measure the overlap time as follows. Two 10 nsec FWHM pulses from a single source all initially separated in time and fed into two of the inputs of the Model 465 or 466. The output of the 465/466 is displayed on an oscilloscope which is being externally triggered by the source (see diagram below). Initially, no output will appear from the 465/466 (see waveforms below). At some duration of overlap, output pulses will always appear. The minimum coincidence overlap is defined in LRS terminology as that amount of overlap which produces one output on the average for every two sets of inputs (i.e., 50% point). From the waveforms below this is equal to $T_3 - T_1$. The 50% point can be quite accurately estimated on the oscilloscope (externally triggered) by adjusting the second pulse delay for equal intensity of trace (of the output states) for the duration of the output pulse. The minimum resolving time for the Model 465/466 is 1.1 nsec. The resolving time jitter can also be measured by taking the difference between 0% limit and the 100% limit ($T_3 - T_1$). The resolving time jitter for the Model 465/466 is +20 psec.





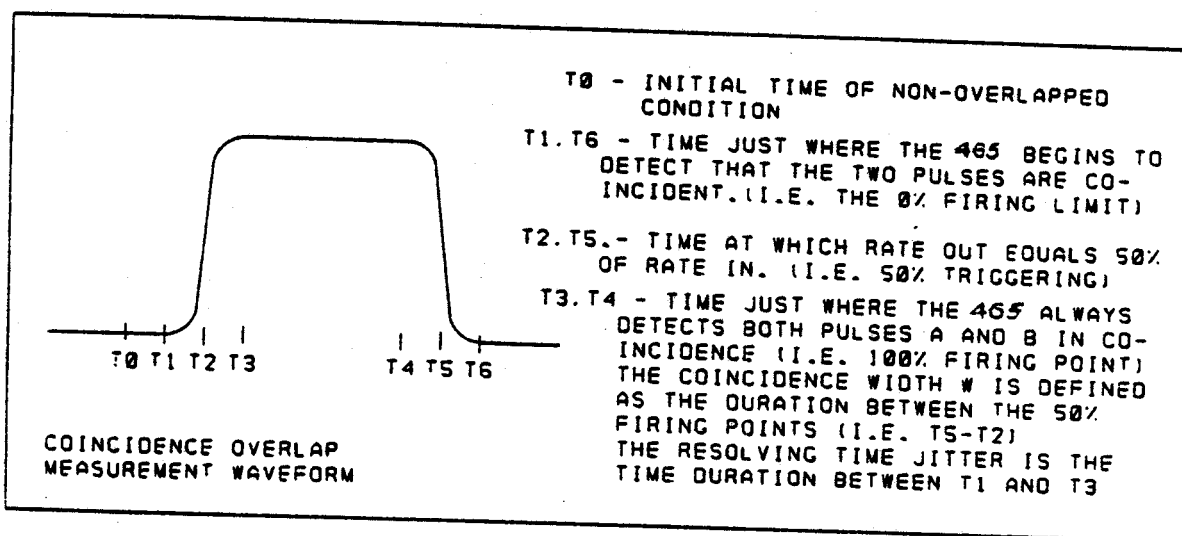
Coincidence Curve Method of Measuring Resolving Time: An alternate method used at LRS to measure the resolving time and time jitter involves making a coincidence curve and then measuring its "risetime" and "faltime". Two pulses from a single source are initially separated in time and fed into the inputs of the 465 or 466, at the same time being collectively counted in a scaler (see diagrams below). The 465/466 output is also counted into another scaler channel.



OPERATION

As one pulse is delayed more and more, the two pulses become more and more coincident; by comparing the counts in the two scaler channels at different delay amounts, a curve can be made representing Rate Out/Rate In vs. Time Delay where the time delay is measured from the trailing edge of Pulse A to the leading edge of Pulse B. (The previous waveform diagram is valid for this measurement also, except Pulse A delay should be continued until its leading edge is past the trailing edge of Pulse B.)

The resultant coincidence curve for this measurement would appear as follows:



The minimum coincidence overlap or minimum resolving time of the logic unit is defined as one-half the difference between the sum of the input pulse widths and the coincidence width measured above. Alternately (but with more difficulty), if t_0 represents the time at which pulse A trailing edge and Pulse B leading edge are exactly coincident in time, then the minimum resolving time is equal to $t_2 - t_0$.

If both input pulses A and B are identical in shape, and if the inputs to the coincidence unit are identical, the trailing edge side of the coincidence curve should be symmetrical to the leading edge side. If they differ, the larger one (either 0% to 100% or 100% to 0%) is specified as the resolving time jitter.

OPERATION

It is important to note that the major contribution toward resolving time jitter in typical logic units is the instability of the "threshold" level of the differential amplifier following the input "AND" stage, particularly for inputs with slow inherent risetimes (i.e., ≈ 2 ns). In the 465 and 466, a true high sensitivity discriminator is used which has a very stable and jitter-free threshold (the LD601C hybrid used in all LRS multichannel NIM discriminators). For this reason, the resolving time jitter of the 465/466 is quite small.

Timing Characteristics: Maximum CW rate capability of the 465/466 is guaranteed at 110 MHz. Typically, the maximum rate is 120 MHz, with some units being capable of operation beyond 130 MHz for small bursts of input pulses. The measurement for maximum rate is made by applying pulses to one of the inputs, with the other three inputs either disconnected or set in the OFF position (i.e., internally always enabled at a DC logical 1).

The double pulse resolution (DPR), as opposed to CW rate capability, actually defines the speed of a logic unit in high energy physics applications, since the double pulse or the pulse burst is apt to occur whereas a CW input pulse train would be unlikely. For a coincidence unit like the 465 or 466, the coincidence width of the input pulses would limit the double pulse resolution of the unit. Each input itself is capable of responding to input pulses spaced 8 nsec apart, measured at the FWHM points of the leading edge (i.e., -375 mV point for -750 mV input pulses). Since the minimum coincidence width of the 465/466 is approximately 5 nsec (defined by a 1.1 nsec minimum overlap of two 3.5 nsec pulses in coincidence), the 465 and 466 can actually function as a coincidence circuit, resolving coincidences spaced as narrow as 8 nsec apart.

Packaging: The 465 and 466 Triple Coincidence Units are packaged in #1 NIM modules with Lemo-type connectors. Due to front panel space limitations, the 465/466 is not offered with BNC's.

Current Requirements: The current usage of the 465 and 466 will permit the use of modules per standard NIM bin offering 5 A of ± 6 V, 2 A of ± 12 V, and 1 A of ± 24 V. Power calculation works out to 7.1 watts, which does not exceed the 8 watts recommended by the NIM standard for the maximum power dissipation for a single NIM slot. It is recommended that additional -6 volt current be supplied to permit maximum usage of NIM Bin space or that the 465's and 466's are powered in the same NIM bin with other modules not requiring -6 volts.

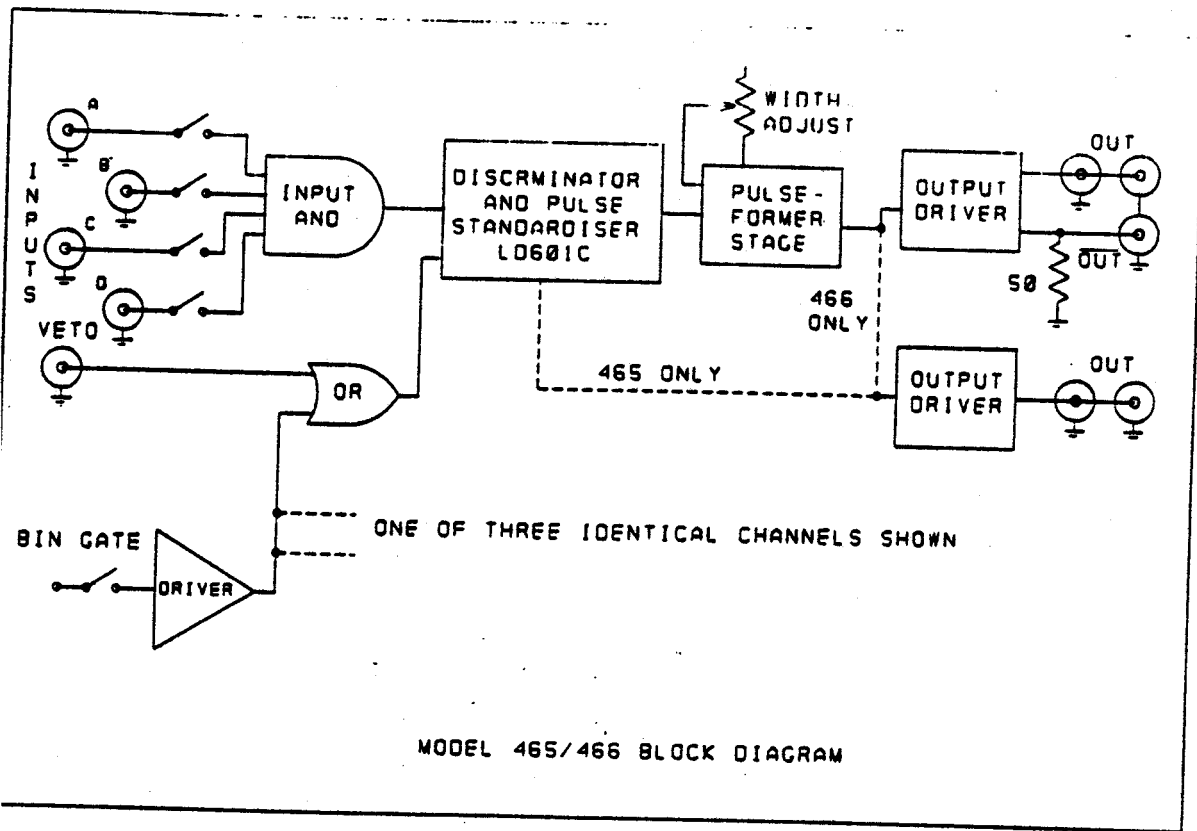
OPERATION

Recommended Use of the NIM Power Bins: It is highly recommended to keep any NIM bin at as constant a temperature as possible, using air conditioning in the trailer or experimental station and definitely using fans to assure an air flow through all modules in every bin. Elimination of large temperature variations removes the worry of temperature drift effects upon modules of any manufacturer, and the forced air flow is good insurance against the potential failure of components in the modules due to excessive heating for extended periods of time. Despite the fact that all components are pre-aged and burned-in before insertion into LRS modules, and the modules themselves are temperature cycled for days under power between initial test and final test, it is recommended to avoid subjecting any modules to adverse operating conditions if it could be avoided.

FUNCTIONAL DESCRIPTION

General

Each of the three channels of the Models 465 and 466 are composed of four basic sections: the Input AND Stage, the Discriminator and Pulse-Standardizer Stage, the Timing or Pulse-Former Stage, and the Output Stage. A block diagram of the Models 465 and 466 can be seen below, and a complete schematic of the specific model can be found at the end of this manual.



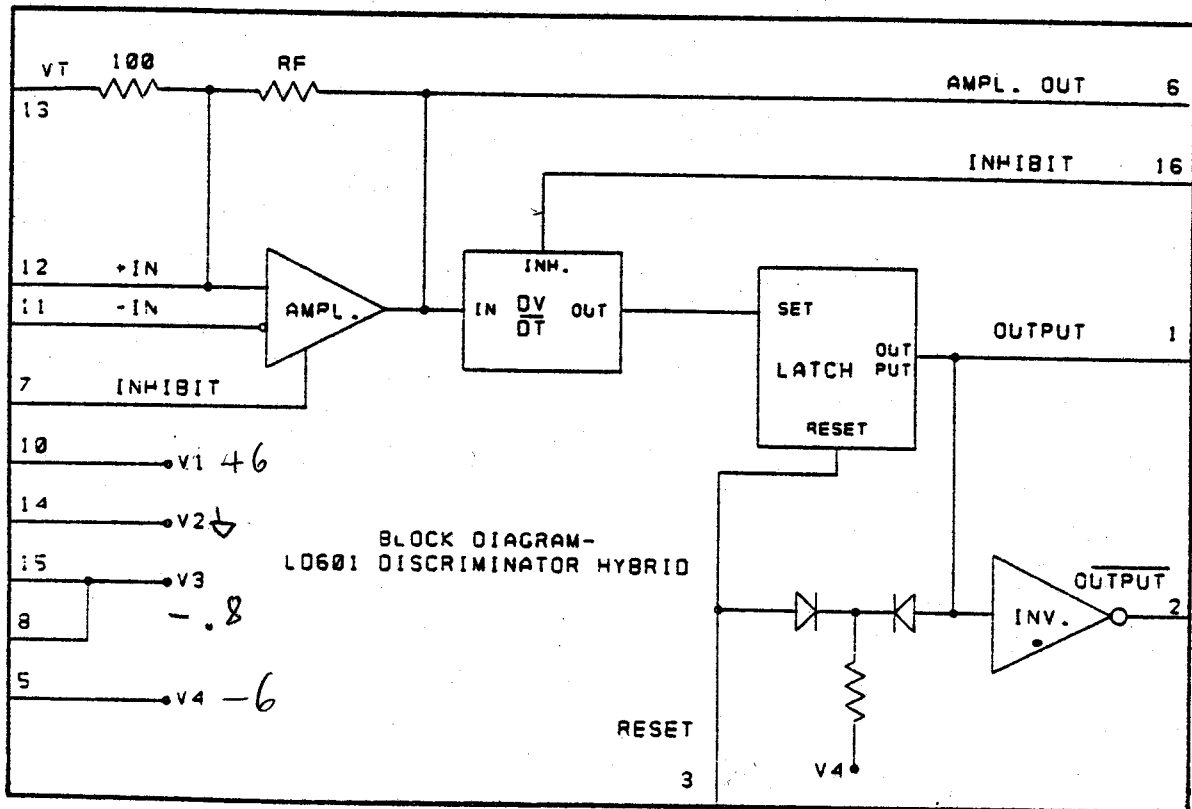
MODEL 465/466 BLOCK DIAGRAM

Input AND Stage

The input stage accepts up to four inputs, each of which can be switched such that the input is disconnected from the internal logic AND gate and a DC logic "1" continuously enables the internal input. The result is the equivalent of a switch-selectable 1-input, 2-input, 3-input, or 4-input AND. This is accomplished with four emitter-ORed followers driving a discriminator stage which is biased at a negative voltage to compensate for

FUNCTIONAL DESCRIPTION

the base-emitter drop of the transistors while sensing the NIM outputs at the full-width-half-amplitude point when a coincidence overlap occurs. In the special case where all four inputs are switch-disabled, to prevent the LINEAR (Overlap) output of the Model 465 from going high, a diode OR senses the condition and disables the input.



Discriminator and Pulse Standardizer

The discriminator stage is based on the LRS Model LD601C hybrid. This unit contains all of the circuitry of the discriminator. The LD601C is functionally presented above. The threshold level is set by the voltage bias on a fast differential amplifier which has positive feedback to provide regeneration at threshold. In actual operation the V_T input is tied to -0.8 V and the threshold level is determined primarily by the 19:1 voltage divider composed of the external 1.8 K resistor to -6 V (the 1N4448 diode is not conducting unless a veto or bin gate is present) and the internal 100 Ω resistor. When an input

FUNCTIONAL DESCRIPTION

signal applied to -IN from the Input is equal to the threshold voltage at +IN, the saturating amplifier output will begin to go positive. This will force +IN closer to 0 volts, which increases the differential input voltage in such a direction that the output locks and then the cycle reverses. The amplifier output thus provides a time-over-threshold pulse with fixed amplitude. This pulse can be monitored at the AMPL. OUT point (pin 6). The quiescent level should be nominally -2.4 volts going to -1.6 volts during the pulse. The leading edge of this output sets the latch circuit which is used as a pulse width standardizer. Before the amplifier and the latch can be set, the inhibit inputs (used for the bin gate and veto) must be off. (See following paragraph.) Once the latch is set, a latch OUTPUT is available to start the Model 465/466 timing stage. The OUTPUT amplitude and leading edge should be similar in appearance to the AMPL. OUT above, but the width of the output will be fixed independent of the input width. Internally, the latch output is fed back to reset the latch after a short time delay, thus generating a short output pulse whose actual width can be set by the proper external selection of RC time constant and voltage levels at Pins 3 and/or 4. It is set at approximately 3 nsec in the Model 465/466.

Each channel of the Model 465/466 has an independent front panel NIM-level veto input and a common rear connector bin gate input. The bin gate driver output is used to disable the three veto input stages, accomplishing the equivalent to a veto pulse causing the veto input circuit to current-switch. In either case, the normally off diode connecting this circuit to +IN of the LD601C will now conduct, pulling the +IN below the level of the -IN. This type inhibit is required for the Model 465 LINEAR (overlap) output, and it is important that the veto input completely overlap the coincidence overlap input to completely block the LINEAR output. The veto circuit is also connected to Pin 16 of the LD601C to accomplish a leading edge inhibit (requiring only an overlap of the leading edge of the coincidnec overlap input) for the 466 and the PRESET outputs of the 465.

Older Models 465 and 466 units use the LD601B hybrid, while more recent units use LD601C's. These two hybrids are identical and interchangeable.

Timing Stage

The timing or pulse-forming stage of the Models 465 and 466 utilize three stages of MECL MCL692 receiver for amplifying and shaping. The timing is done by first charging a 33 pf capacitor with the pulse from the LD601 (via one MCL692 stage and the differential stage, composed of two A430 transistors) until it is clamped by the FD777 diode to a voltage set indirectly by the front-panel width

FUNCTIONAL DESCRIPTION

potentiometer (via two stages of 747). The discharge rate is set by the current source stage composed of the width potentiometer, one stage of 747, the current source transistor, and its associated 604-ohm emitter resistor. The actual current is varied from near zero (for the 1 μ sec maximum width) to about 10 mA for the 5 nsec minimum width). Thus, simultaneously, as the width is increased, the clamp voltage is increased (allowing more initial charge to be stored on the timing capacitor) and the current is decreased (reducing the rate of discharge), thus multiplying the effect of the width control. An internal trim resistor, T_W , sets the minimum width to 5 μ sec. The effect of the 2N5962 and the diodes associated with it are to provide fast recovery of the timing capacitor. The MCL692 ECL amplifiers are interconnected in a manner to provide stable leading edge timing and fast risetimes and falltimes of the output pulse. The first amplifier (output pin 3) provides final shaping and standardization of the pulse from the LD601 to the timing stage, as well as driving the preset output stage directly via a second 1692 amplifier (output pin 14). This provides a prompt output pulse for the duration of the 601 output, independent of the delay encountered in initializing the timing stage. Before the 601 output is over, the timing capacitor is charged, causing the third amplifier (output pin 15) to now maintain the pulse level to the output stage (using emitter ORing) until the timing capacitor subsequently discharges to a sufficiently low level (approximately -2.0 volts). At this point, (because of regeneration, the third amplifier promptly switches back to its quiescent off condition, terminating the output pulse.

The Model 465 has one set of bridged outputs which completely bypass the timing stage, receiving their timing and drive directly from the AMPL. OUT of the LD601C. Thus, the output duration is just equal to the FWHM of the overlap of the input pulses.

Output Stage

One output stage of the Model 465 and both outputs of the 466 all utilize a conventional differential stage. This stage requires a continuous 32 mA of current of which 16 mA is quiescently available at the complementary back-terminated output connector. During an output pulse, the MCL692 will switch from the quiescent level of -2.4 volts to a higher level of -1.6 volts, causing the differential stage to switch the 32 mA current from the complementary half of the stage to the normal output connectors for the duration of the pulse. All outputs are diode clamped so they will provide proper operation even without output loads. Without the diode path for the current during the pulse, the

FUNCTIONAL DESCRIPTION

current would have to be supplied via the transistor base, which would severely load the driver and not allow proper drive to the remaining stages. In all cases, the dual bridged outputs should both be terminated in 50 ohms for normal output amplitudes and shape.

The other output stage of the 465 output stages is connected directly to the AMPL. OUT of the LD601. The voltage levels of the LD601 are the same as the MC1692, so the operation is as above.

Internal Power Supplies

Three internal power supplies are used to generate the -0.8, and -2.2, and -11.5V which are special bias voltages used by the three channels. These stages provide voltage regulations and tracking and provide proper temperature compensation for the other sections, particularly the width and threshold circuits. They depend to some degree on uniform heating of the entire circuit board. Heating local areas of the board may cause drifting, but operating in a normal bin environment these supplies compensate to stabilize operation. In all cases, the power supply uses a LM301 operational amplifier to maintain the output voltage of a series-pass transistor equal to an input reference voltage. The reference voltages are adjusted via individual potentiometers or trimmed resistors.

If the -6 voltage is DC sequenced on before the +6 voltage, the LD601C may be forced into a DC latched condition. To prevent this, a relay contact does not supply the -6 VDC until the relay coil, operating from the +6 VDC is energized. This insures that the +6 is up before the -6 in any power-on sequence.

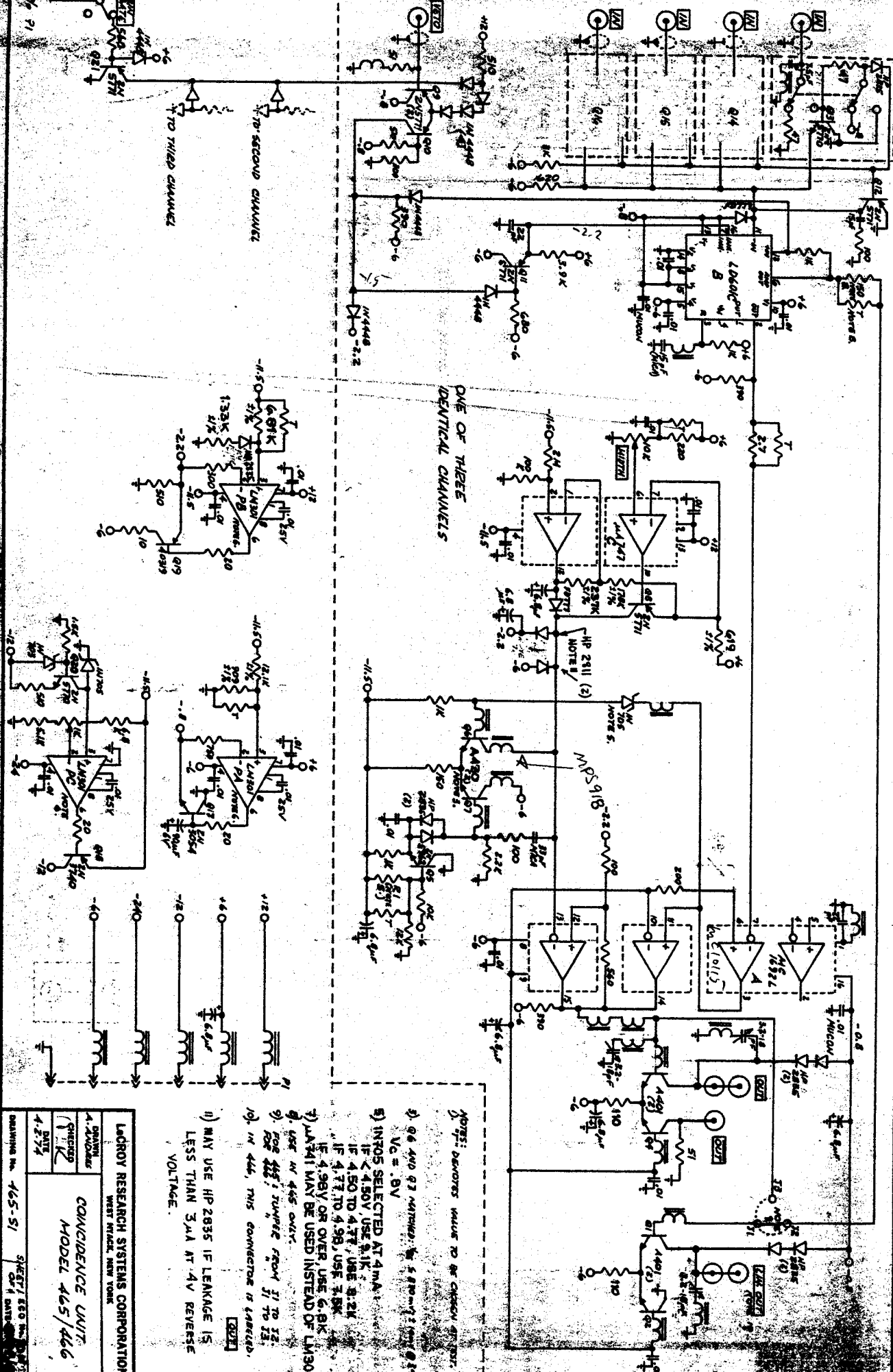
Date of Last Update: _____

Updating Addenda to General Description or Specifications

Model 465: Input/Output Delay: 13 nsec for preset outputs; 8.5 nsec for linear outputs.

Model 465/466: Coincidence Resolving Time: The required minimum coincidence overlap time of the 465 and 466 is 1.1 nsec.

Resolving Time Jitter: As defined in the Operation of this manual, is +20 psec.



- NOTES: DENOTES VALUE TO BE CHOSEN AT 20°C.
- 1) 0.6 AND 0.7 PARTS PER 5.8 PARTS PER 0.1 Vc = .8V
 - 2) INTOS SELECTED AT 4mA
 - 3) IF < 4.50V USE 2.1K
 - 4) IF 4.50 TO 4.77, USE 3.2K
 - 5) IF 4.77 TO 4.98, USE 4.8K
 - 6) IF 4.98V OR OVER, USE 6.8K
 - 7) JAW741 MAY BE USED INSTEAD OF LM301
 - 8) USE IN 445 ONLY
 - 9) FOR 445; SWAP FEED J1 TO J2.
 - 10) FOR 446; SWAP FEED J1 TO J2.
 - 11) MAY USE HP 2835 IF LEAKAGE IS LESS THAN 3µA AT 4V REVERSE VOLTAGE.

LADROY RESEARCH SYSTEMS CORPORATION
 WEST PALM BEACH, FLORIDA

COINCIDENCE UNIT
 MODEL 465/466

DRAWING NO. 465-51 SHEET 1 OF 2
 DATE 4-27-64

DESCRIPTION

DATE

ECO NO.

059	2-19-76	FOLLOWUP OF ECO 995: ALL OUTPUT TRANSISTORS CHANGED TO A 401, WITH A FULL BEAD ON EACH BASE/ 46 & 47 (MATCHED PAIR) CHANGED TO PLRS 003/ ALL OUTPUT BEADS REMOVED/ A 3.2 - 18 pF TRIMMER ADDED IN SERIES WITH BEAD FROM EACH BRIDG. OUTPUT TO GROUND.
075	3-16-76	ALL DOCUMENTATION: MBD 101 CHANGED TO HP2835, - IN 18 PLACES./ PRINTED CKT. ONLY: TAPING CORRECTIONS/ PARTS LIST ONLY: HARDWARE CORRECTED/ SCHEMATIC ONLY: CONNECTION FROM J3 CORRECTED - MUST GO TO PIN 14 OF MC1692L.
195	6-23-76	AT MC1692, betw. Pins 14 AND 15: TWO FULL BEADS ADDED/ OFF BASE OF Q3: ONE BEAD DELETED, 18 pF CAPACITOR CHANGED TO 3.2 - 18pF TRIMMER/
367	4-13-77	REMOVED 1.8K RESISTOR AT PIN 12 OF LD-601C(ONE PER CHANNEL).
381	4-3-77	CHANGED ALL MBD101 DIODES TO HP2811 EXCEPT DIODE CONNECTED TO I.C. PB PIN 3 WHICH SHOULD BE HP2835.
1001	5-12-78	REDID FRONT PANEL ARTWORK.
1002	8-9-78	PARTS LIST UPDATED ONLY.
1004	9-17-79	PARTS LIST CHANGED ONLY.
1005	10-1-79	PARTS LIST CHANGE ONLY.
1006	11-5-79	PARTS LIST S465 ENTERED (465 COMP BD.)
1007	11-27-79	REMOVED 3.2-18 pF CAP FROM PIN #3 OF I.C."A". (PRIORITY 4)
1008	3-24-80	Increased emitter resistors on output drivers from 100ohm to 110 ohm.
1009	8-12-80	DELETED PART #'S 168-531-372(3), 168-531-622(3), 168-531-474(1), 169-531-404(1), 270-170-003(6) ADDED PART #'S 168-531-473(1), 168-531-621(3), 168-531-405(1) 270-130-002(6)
1010	2-26-81	TO SPECIFY STRAIGHTNESS OF SHAFT ADDED TRUE POSITION TOLERANCE.DWG #465-M1
1011	2-28-81	CHANGED LENGTH OF ROLL PIN ON FRONT PANEL FROM 11/16 TO 5/8 .ALSO PUT SPACERS UNDER 10K POTS IN 3 PLACES. #519-350-001(9 REQ'D).

LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK

ENGINEERING CHANGE ORDERS

MODEL 465/466

SHEET 2 OF 2

REMARKS: On Priorities
 1-Recall, field retrofit
 2-Rework shippable units
 3-Rework units in fabrication, assembly and test
 4-Improvements for future MO's

DRAWING No.

MODEL NO 465
LAST REVISION NO 1011

COINCIDENCE UNIT
REVISION DATE 28-Feb-81

PRINTED 21-May-81

101	246	**2	PC STOCK DBL SIDED	1	OZ					85M
102	245	103	CAP CERA DISC 25V	.01	UF	PT-FDCL-1/32	LEADS 3/8	AWG 22		41
102	444	220	CAP CERA DISC 100V	22	PF	10% S2L				6
102	944	*75	CAP CERA DISC 1KV	7.5	PF	10% S2L				12
102	944	150	CAP CERA DISC 1KV	15	PF	10% S2L				3
105	228	103	CAP MUCON RIBB LD	.01	UF	SUPER-K CERA 25V 30%				6
116	515	150	CAP DIP MICA DM10	15	PF					3
116	515	330	CAP DIP MICA DM10	33	PF					3
142	824	685	CAP TANT DIP CASE	6.8	UF	35V 20%				19
147	147	*90	CAP ALUM METAL CAN	90	UF	6V -10% +75%				1
158	819	**1	CAP VARI CERA 3.5	-	18	PF				9
161	335	*27	RES COMP 1/4W 5%	2.7	OHMS					3
161	335	100	RES COMP 1/4W 5%	10	OHMS					1
161	335	101	RES COMP 1/4W 5%	100	OHMS					9
161	335	102	RES COMP 1/4W 5%	1	K					12
161	335	103	RES COMP 1/4W 5%	10	K					3
161	335	104	RES COMP 1/4W 5%	100	K					3
161	335	111	RES COMP 1/4W 5%	110	OHMS					6
161	335	123	RES COMP 1/4W 5%	12	K					3
161	335	151	RES COMP 1/4W 5%	150	OHMS					6
161	335	152	RES COMP 1/4W 5%	1.5	K					1
161	335	200	RES COMP 1/4W 5%	20	OHMS					3
161	335	201	RES COMP 1/4W 5%	200	OHMS					3
161	335	205	RES COMP 1/4W 5%	2	MEG					3
161	335	221	RES COMP 1/4W 5%	220	OHMS					3
161	335	222	RES COMP 1/4W 5%	2.2	K					3
161	335	301	RES COMP 1/4W 5%	300	OHMS					4
161	335	302	RES COMP 1/4W 5%	3	K					3
161	335	391	RES COMP 1/4W 5%	390	OHMS					9
161	335	392	RES COMP 1/4W 5%	3.9	K					3
161	335	470	RES COMP 1/4W 5%	47	OHMS					24
161	335	510	RES COMP 1/4W 5%	51	OHMS					6
161	335	511	RES COMP 1/4W 5%	510	OHMS					8
161	335	512	RES COMP 1/4W 5%	5.1	K					1
161	335	561	RES COMP 1/4W 5%	560	OHMS					4
161	335	621	RES COMP 1/4W 5%	620	OHMS					3
161	335	681	RES COMP 1/4W 5%	680	OHMS					3
161	335	682	RES COMP 1/4W 5%	6.8	K					1
161	335	751	RES COMP 1/4W 5%	750	OHMS					1
161	335	752	RES COMP 1/4W 5%	7.5	K					3*
161	335	822	RES COMP 1/4W 5%	8.2	K					3*
168	531	373	RES PREC RN55D	619	OHMS					3
168	531	389	RES PREC RN55D	909	OHMS					1
168	531	405	RES PREC RN55D	1.33	K					1
168	531	473	RES PREC RN55D	6.81	K					1
168	531	497	RES PREC RN55D	12.1	K					1
168	531	609	RES PREC RN55D	178	K					3
168	531	621	RES PREC RN55D	237	K					3
181	457	102	RES VARI CERMET	1	K	1/2W 10%				1
182	537	103	RES VARI CERMET	10	K	3/4W 10%				3
204	*21	**4	IC LINE RECEIVER	MC1692L	QUAD	PKG/DIP-16				3
208	*11	**3	IC SINGLE OP AMP	LM301AN	DIP-8					3
208	*34	**1	IC DUAL OP AMP	UA747	DIP-14					3
210	*40	**2	IC AMPLITUDE DISCR	LD601C	DIP-16					3

MODEL NO 465
 LAST REVISION NO 1011

COINCIDENCE UNIT
 REVISION DATE 28-Feb-81

PRINTED 21-May-81

230	110	**3	DIODE SWITCHING	FD 777			6
230	110	**5	DIODE SWITCHING	1N4448			22
240	225	703	DIODE ZENER 3.45V	1N703A	250MW		1
240	225	705	DIODE ZENER 4.85V	1N705A	250MW		4
253	*10	811	DIODE SCHOTTKY BAR	HP2811	H-P CASE OUTLINE 15		6
253	*10	835	DIODE HOT CARRIER	HP2835	H-P CASE 15		31
270	130	**2	TRANSISTOR NPN	A 430	TO-72		6
270	130	401	TRANSISTOR NPN	A401	TO-72		12
270	170	**1	TRANSISTOR NPN	2N5770	TO-92		13
270	170	**2	TRANSISTOR NPN	2N5962	TO-92		3
270	190	**1	TRANSISTOR NPN PWR	2N3054	TO-66		1
275	150	**3	TRANSISTOR PNP	40319	TO-5		1
275	170	**2	TRANSISTOR PNP	2N5771	TO-92	SEE 275-170-004(MPS3640)	16
275	190	**1	TRANSISTOR PNP PWR	2N3740	TO-66		1
300	*10	**1	BEAD SHIELDING	FERRITE			48
300	*20	**1	BEAD SHIELDING	"1/2" SIZE			6
300	*50	**1	CHOKE FERRITE	SINGLE LEAD			5
400	*10	**8	SOCKET IC ST	DIP-8	BONDED TIN CONTACTS/COPP-NICKEL PINS		3
400	*20	*14	SOCKET IC ST	DIP-14	BONDED TIN CONTACTS/COPP-NICKEL PINS		3
400	*30	*16	SOCKET IC ST	DIP-16	BONDED TIN CONTACTS/COPP-NICKEL PINS		6
402	*30	**0	CONNECTOR CO-AXIAL	LEMO			30
402	*30	**2	SPANNER NUT SMALL OD	LEMO			30
402	*30	**3	GROUND LUG NONLOCK	LEMO			A/R
402	*30	**4	GROUND STRAP "H"	LEMO			A/R
405	112	**1	CONNECTOR BLOCK	(PIN)	42 "MIXED"		1
405	212	**2	GUIDE PIN	(MALE)	CADMIUM PLATED BRASS		1
405	213	**1	GUIDE PIN	(MALE)	BRASS		2
405	312	**1	GUIDE PIN	(FEMALE)	CADMIUM PLATED BRASS		A/R
405	410	*16	CONNECTOR PIN	(MALE)			1
405	613	**1	CONNECTOR HOOD		CADMIUM PLATED STEEL/INT CLOSED END		12
412	**0	801	SPACER CERAMIC	1/8" LONG	"SUB-MINIATURE"		12
418	**0	301	RETAINING CLIP				12
418	**0	508	SHAFT NYLON		PER DWG 465-M1		12
418	**0	509	COUPLER		PER DWG 465-M2		12
418	241	**2	SWITCH SLIDE PB-10	4 STA	TERM BOTH SIDES/PUSH-PUSH/NO MTG TAB		
420	212	**1	SWITCH SLIDE	DPDT			
500	120	**2	TRANSIPAD	"LARGE"			
519	350	**1	BUSHING NYLON		APPROX .114 OD & .040 ID/.078 LONG		
540	103	102	SIDE COVER	NIM LEFT			
540	103	103	SIDE COVER	NIM RIGHT			
540	104	101	WRAPAROUND	NIM SIZE #1	WITH BIN GATE		
540	105	**1	BRACKET	NIM WRAP SIZE #1			
555	611	**1	CAPTIVE SCREW	6-32			
555	621	**2	CAPTIVE SCREW RETAINER		NICKEL PLATED BRASS		
567	256	**4	SCREW FLAT PHIL	2-56X1/4			
585	141	237	RIVET "POP" ALU	1/8X.237	BUTTONHEAD 1/8 DIA .237 LONG		
710	465	*13	PC BD PREASS'Y	465-466			
720	465	*13	FRONT PNL PREASS'Y	465	540102001(1)555621002(2)		
740	**0	**2	WRAPAROUND NIM	1 BIN GATE	540104101(1)		

NOTE: 1
 NOTE: 2
 NOTE: 3
 NOTE: 4
 NOTE: 5