NSCL-ELECTRONIC

MODEL 612AM
6-CHANNEL PHOTOMULTIPLIER
AMPLIFIER

Rev: November 19, 1981

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ANY APPLICATION OR USE QUESTIONS, which will enhance your use of this instrument will be happily answered by a member of our Engineering Services Department, telephone 914-425-2000 or your local distributor. You may address any correspondence to:

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ATTENTION

SEE POCKET IN BACK OF MANUAL FOR SCHEMATICS, PARTS LISTS, AND ADDITIONAL ADDENDA WITH ANY CHANGES TO MANUAL.

ATTENTION

GENERAL

The LeCroy Model 612AM is a six channel, variable gain, wideband amplifier, packaged in a single width NIM module. The gains at the six channels are individually setable via front panel screwdriver adjustments. Each channel consists of a VV100B hybrid amplifier cascased to a second VV100B via a variable attenuator. Each channel is capable of driving two 50 Ω loads.

OPERATION

Operation of the 612AM is extremely simple and consists of cabling to inputs and outputs as well as front panel gain adjustment. All channels are factory compensated for a 25 Ω output load. Thus, if only a single 50 Ω output is used, the other output should be terminated into 50 Ω. The VV100B incorporates an integrating output stage which senses and limits output current to an average value of 120 mA. Thus, output peak currents are a function of input pulse amplitude, width and repetition rate. A switch on the rear panel of the 612AM allows operation from either 6 or 12 volts. Twelve volt operation extends the linear operation region from -2 volts to about -5 volts. The 612AM incorporates a dual diode limiting input stage. For small ($\leq$-300 mV) inputs, the input impedance is 50 Ω nominal. But at higher pulse levels or D.C. offset input levels, the diode impedances will short the 50 Ω resistive termination. Because the 612AM input is D.C. coupled, several channels may be cascaded. However in cascaded operation, the user should always be aware of the effects of both input noise and input D.C. offset. For instance, four cascaded amplifiers must maintain an input offset of less than 0.5 mV over the entire temperature range in order to ensure linear operation.

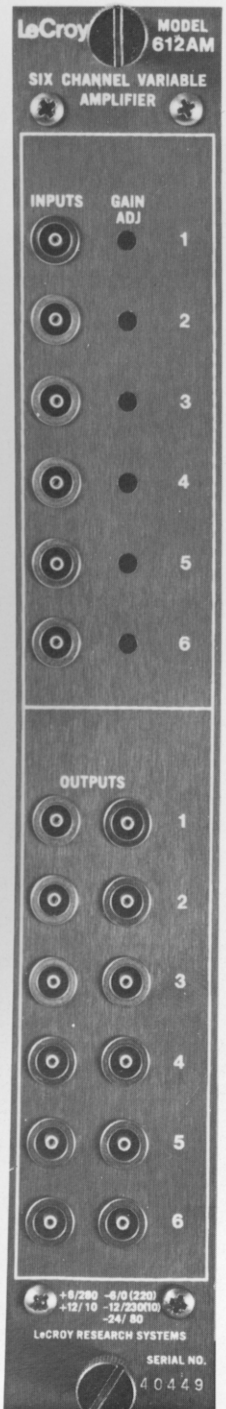
REPLACEMENT INFORMATION

In the event that the 612AM must have a channel of VV100B replaced, the trims described in the VV100B manual must be readjusted. Trims T1 and T3 are fixed resistors soldered onto the 612AM board. Trim T2 is accomplished by an on-board 1 MΩ potentiometer and high frequency compensation is set by a variable capacitor. Before the fixed resistors are removed, the user should check to see whether input D.C. offset and low frequency gain are within acceptable limits with the new VV100B installed.

June, 1978

TECHNICAL DATA

LeCroy



NIM Model 612AM

6-Channel Photomultiplier Amplifier

* 6 channels/ #1 NIM module
* Identical 50 Ω outputs per channel
* Gain of 2.5 to 40, direct-coupled
* < 3 nsec risetime
* −5 volt linear range (5000:1 usable dynamic range)
* 0.2% integral linearity
* Low cost

The LeCroy Model 612AM is a six-channel, wide-bandwidth amplifier with continuously adjustable gain packaged in a #1 NIM module. The unit features a bandwidth of DC to 140 MHz with a maximum gain of 40. Representing a major advance in fast amplifier stability, dynamic range, and general utility, the 612AM allows the experimenter for the first time to consider the use of economical lower gain photomultiplier tubes even in demanding direct-coupled ADC applications. The adjustable gain feature affords simpler high voltage distribution systems because the gains may be equalized by the 612AM. This avoids the problems of variation in photomultiplier propagation time with high voltage. The Model 612AM offers a built-in fan-out of two, simplifying simultaneous use of the same photomultiplier signal for both analog and logic purposes by eliminating the extra cable run necessary when both anode and dynode signals are used. Packaged 6 channels per module, the 612AM offers substantial savings in bin space and is directly compatible with standard LeCroy ADC's and multichannel discriminators.

A new high-speed operational amplifier circuit design makes the performance of the amplifier virtually independent of external variables such as supply voltages or temperature. Input and output DC levels remain negligibly small even when the module is moved from bin to bin, or under extremes of operating temperature. There is virtually no warmup drift on turn-on. These stability characteristics, together with the excellent linearity, speed and noise characteristics of the circuit, come very close to the ideal of a "transparent gain" element that simply magnifies the input without significant distortion or operating constraints.

The Model 612AM normally operates from ±6, ±12, and −24 volts. A rear-panel switch permits operation from −12 instead of −6 volts for those applications in which −6 volts is not available or where dynamic range is more important than a moderate saving in power consumption. When operated from −12 volts, maximum output amplitude is increased from −2 to −5 volts. In either case, the large output levels available reduce recovery time problems associated with overload.

October 1982

Innovators in Instrumentation

LeCROY RESEARCH SYSTEMS CORPORATION • 700 SOUTH MAIN STREET • SPRING VALLEY, N.Y. 10977
TWX: 710-577-2832 CABLE: LERESCO TELEPHONE: (914) 425-2000

SPECIFICATIONS
NIM Model 612AM
6-CHANNEL PHOTOMULTIPLIER AMPLIFIER

INPUT CHARACTERISTICS	
Impedance:	50 Ω.
Input Protection:	±5 A for 0.5 μsec; ±0.5 A continuous; clamps at ±0.6V.
Reflection Coefficient:	Less than 5% over input dynamic range.
Quiescent Voltage:	±0.5 mV.
OUTPUT CHARACTERISTICS	(Both outputs of each used channel must be terminated for optimum waveshape.)
Maximum Positive Amplitude (Linear):	+200 mV.
Maximum Negative Amplitude (Linear):	−2 volts with −6 V supply; −5 volts with −12 V supply.
Overshoot:	Less than ±10% for input risetimes >1.5 nsec and gains >4X. Slightly larger for gains <4X.
Quiescent Voltage:	0 V ±3 mV.
Output Voltage DC Offset Temperature Coefficient:	400 μV/°C maximum.
Output Voltage Variation with Supply Voltage:	<4 mV for ±1% variation of any supply voltage.
GENERAL	
Gain:	2.5 to 40, non-inverting. Long-term stability ±1%.
Linearity:	0.2% integral.
Coupling:	Direct.
Risetime:	<3.0 nsec, 10% to 90%.
Delay:	Approx. 5.5 nsec.
Noise:	Less than 50 μV rms, referred to input, total.
Interchannel Crosstalk:	Output in one channel affects any other channel by no more than −40 dB.
Overload Recovery:	a) Operation with −12 volt supply: saturated for approximately 15 nsec after 10X overload. b) Operation with −6 volt supply: saturated for approximately 50 nsec after 10X overload. For wide pulses (i.e., >5 μsec) it is recommended to use −12V supply for best overload recovery.
Packaging:	RF-shielded AEC/NIM #1 width module conforming to specifications outlines in AEC Report TID-20893; Lemo-type connectors.
Current Requirements:	+6 V at 280 mA; −12 V or −6 V at 230 mA (selected by rear-panel switch); +12 V at 10 mA; −24 V at 80 mA.

SPECIFICATIONS SUBJECT TO CHANGE.

TECHNICAL DATA

VV100B/VV101A Hybrid Circuit
Wideband Pulse Amplifier

FEATURES:

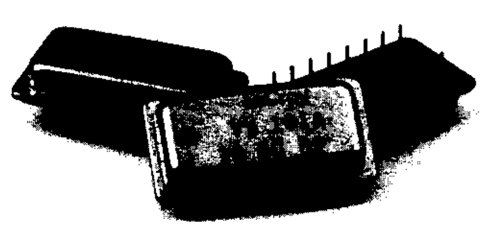
- **WIDE BANDWIDTH** risetime: <2 nsec VV100B
  <1 nsec VV101A
- **DIRECT-COUPLED DESIGN** permits high rate application without baseline shifts.
- **10X GAIN, CASCADABLE** to 1000X for direct compatibility with a wide range of input amplitude applications.
- **±0.2%, INTEGRAL LINEARITY** to outputs of −3 V.
- **EXCELLENT DC STABILITY** (<1 mV long term) assures optimum performance in dc coupled applications.
- **LOW IMPEDANCE OUTPUT** designed to drive two 50 Ω loads, allowing the amplified signal to be used directly for both logic and analog functions.
- **COMPACT PACKAGING** permits the complete amplifier to be mounted near the pulse source in a standard 16-pin DIP socket, thereby reducing amplification of extraneous noise.

The LeCroy Model VV100B/VV101A is a wide-bandwidth, gain-of-10 pulse amplifier packaged as a standard 16-pin DIP hybrid circuit. Representing a major advance in fast amplifier bandwidth, stability, dynamic range, and general utility, the VV100B/VV101A provides unprecedented performance in demanding, direct-coupled, high-duty-cycle applications.

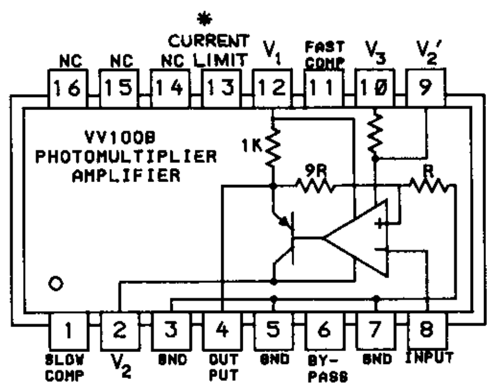
A new high-speed amplifier circuit design makes the performance of the VV100B/ VV101A virtually independent of external variables such as supply voltages or temperature. Shifts in the dc output level remain negligibly small even when the amplifier is subjected to extremes of operating temperature or variations in power supplies. There is virtually no warm-up drift at turn-on.

An ideal "transparent gain" element would simply magnify the input signal without significant distortion or operating constraints. The VV100B/VV101A performance is very close to this ideal by virtue of its extraordinary stability, speed, linearity, and noise characteristics.

PACKAGING



LOGIC DIAGRAM (TOP VIEW)



* VV100B ONLY

November 1981

Innovators in Instrumentation

LeCROY RESEARCH SYSTEMS CORPORATION • 700 SOUTH MAIN STREET • SPRING VALLEY, N.Y. 10977
TWX: 710-577-2832 CABLE: LERESCO TELEPHONE: (914) 425-2000

SPECIFICATIONS
Hybrid Circuit Models VV100B/VV101A
WIDEBAND PULSE AMPLIFIER

	VV100B	VV101A
GAIN:	10 FIXED, ±5% tolerance, non-inverting, long term stability ±1%	Same as VV100B
LINEARITY:	±0.2% intergral (0 to −3 V)	Same as VV100B
MAXIMUM OUTPUT SWING:	−5 V at 200 mA Note 1 +250 mV at 5 mA Note 3	−5 V at 200 mA Note 2 Same as VV100B
OUTPUT IMPEDANCE:	<0.2 Ω for negative outputs	<0.3 Ω for negative outputs
FREQUENCY RESPONSE:		
Full Signal Bandwidth (3 dB)	≥170 MHz for 2 voltage operation Notes 4,7 ≥200 MHz for 3 voltage operation	≥350 MHz for 2 voltage operation Note 4 ≥380 MHz for 3 voltage operation
RISETIME (10% to 90%):	≤2 nsec	≤1 nsec
INPUT SIGNAL RANGE:		
Maximum Safe Input Signal	±1 V; external clamp diodes recommended Note 6	Same as VV100B
Linear Range	−0.5 V to +0.01 V	Same as VV100B
WIDEBAND OUTPUT NOISE: (referred to input)	<50 μV rms	<60 μV rms
INPUT IMPEDANCE:	>1 kΩ	Same as VV100B
INPUT BIAS CURRENT:	−25 μA	Same as VV100B
Drift vs. Temperature	250 nA/°C	Same as VV100B
INPUT OFFSET VOLTAGE:		
Typical	2 mV, adjustable to 0	Same as VV100B
Drift vs. Temperature	10 μV/°C (max)	
Drift vs. Supply Voltage	<100 μV for ±1 % variation	
Drift vs. Time	<100 μV, long term	
COUPLING:		
Input	Direct	Direct
Output	Direct	Direct
TEMPERATURE RANGE:	0°C to 70°C	Same as VV100B
POWER SUPPLY REJECTION RATIO:	90 dB at 120 Hz	Same as VV100B
POWER SUPPLY: (Two Voltage Operation) Note 4		
Rated Voltage, Quiescent Current	$V_1 = +6$ V at 30 mA $V_2 = -6$ V to −12 V at −20 mA (Tie pin 9 to pin 2)	Same as VV100B
POWER SUPPLY: (Three Voltage Operation) Note 5		
Rated Voltage, Quiescent Current	$V_1 = +6$ V at 30 mA $V_2 = -6$ V to −12 V at −28 mA $V_3 = V_2 - 12$ V (e.g.,−24 V when $V_2 =$ −12 V and pin 9 open) at −8 mA	Same as VV100B
OVERLOAD RECOVERY:	Operation with $V_2 = -12$ V supply: saturated for approximately 15 nsec after 10× overload.	Same as VV100B
PACKAGE:	Standard 16-pin dual in-line hybrid integrated circuit.	Same as VV100B

NOTES:

1. Overload protected to limit the average output current to <60 mA. See application notes.
2. No overload protection. Average output current should be <50 mA to avoid damage to the unit.
3. For increased positive swing, see application notes.
4. Three voltage operation recommended for most applications.
5. Three voltage operation provides increased bandwidth.
6. See figure 1.
7. For two voltage operation install a 6.8 μF capacitor from pin 13 to ground with the positive lead grounded.

SPECIFICATIONS SUBJECT TO CHANGE.

APPLICATION NOTES

The LeCroy Model VV100B/VV101A is a hybrid circuit designed as a high bandwidth amplifier primarily intended for amplification of negative pulses such as those from photomultiplier tubes. It has a fixed gain of 10 and a risetime of less than 2 / 1 nsec. The output is capable of driving two 50 Ω loads (25 Ω). The linear range of the VV100B is +200 mV to − 5 V. The Model VV101A provides similar performance with twice the bandwidth.

The user may supply suitable input impedance for his particular needs. The unit requires an input terminating resistor, power supply bypass capacitors, input and output dc trims and an output shape capacitive trim.

Figure 1 shows a typical application circuit for the VV100B and is the circuit on the LeCroy VV100BTB amplifier. Here input trim T1 is accomplished by the series combination of a 27 kΩ resistor and a 500 kΩ potentiometer. Trim T2 is set by the 1 MΩ potentiometer and series 100 kΩ fixed resistor. A fixed resistor to ground sets the low frequency gain trim (T3). High frequency compensation is set by the 51 Ω, 6-35 pF combination.

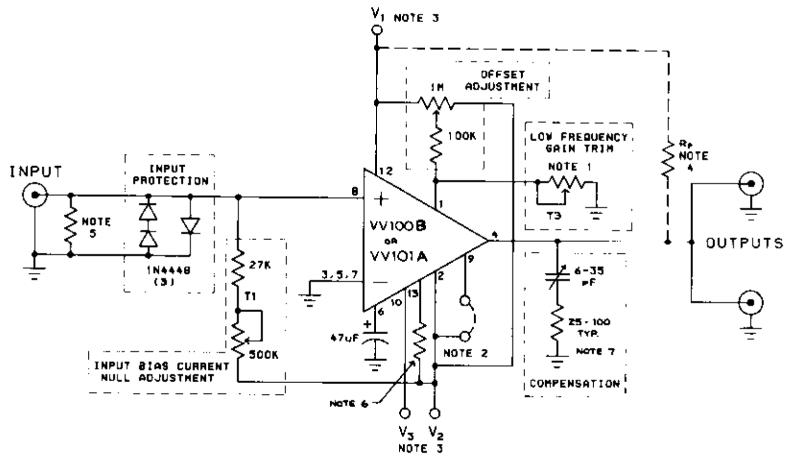


Figure 1

NOTES:

1. Typical value = 7.5 kΩ
2. Add jumper for 2-supply operation
3. All power supply voltage lines should include a high frequency bypass, typically a 6.8 μF capacitor to ground and a 50 μH series choke.
4. Optional pull-up for extended positive voltage exclusions.
5. Input termination resistor, chosen to match input cable impedance.
6. 10 Ω current limiting resistor should be added when driving 25 Ω load (VV100B only).
7. For VV101A, 6-35 pF in series with 25 Ω connected from pin 11 to ground provides additional compensation.

The VV100B contains output protection circuitry which limits the average output current to 60 mA. The time constant of the limiting circuit is approximately 6 μsec. This feature is not provided in the VV101A, so caution should be used to avoid damage by short circuit of its output. One common failure mode results when several stages of VV101A are cascaded. The second stage should not have diode protection of its input, otherwise an overdrive of the first stage will activate the second stage protection circuit, shorting and possibly damaging the first VV101A.

The internal current limiting of the VV100B may be defeated by placing a jumper between pins 13 and 2. This connection allows bipolar operation if an additional resistor is connected from the output to a positive supply voltage. All positive current delivered to the load is through this additional resistor. The dc value of this added current should be held to less than 40 mA.

If internal current limiting is not defeated, the maximum positive voltage excursion into a load R_L is

$$V^{+}_{Max} = \frac{6\ R_L}{R_P + R_L}$$

The most negative will be given by

$$V^{-}_{Min} = (0.06\ V)\frac{R_P\ R_L}{R_P + R_L}; \qquad V^{-}_{Min} \geq -5\ V$$

LAYOUT

Because of the extremely high bandwidth of the VV100B and VV101A, care should be used in layout of the printed circuit board. Continuous ground plane construction is essential. To ensure minimum inductance, low profile sockets like the TI or AUGAT should be used. Insertion pins (Berg 75315-001 or equivalent) are even better. Input busses should be separated from the output. Interconnections to other circuitry greater than 3 cm away should be made only by properly terminated coaxial cable. Input protection circuitry and bypass capacitors as described below should be located as close to the hybrid as possible.

THE INPUT

Proper termination and protection must be supplied to the input. In most cases, input to the amplifier will be via 50 Ω cable. In this case, a 50 Ω resistor from the input (pin 8) to ground should be employed. In addition, three 1N4448 or equivalent diodes to ground as shown in figure 1 will provide overload protection. The input dc level must be trimmed to zero by a trim resistor (T1) to a negative supply. Where the best dc stability is required, this supply should be regulated. Note that fluctuations in the input offset will appear at the output amplified 10-fold.

POWER

A current of about 30 mA from +6 V must be supplied at pin 12. In addition, two negative supplies, V_2 and V_3, are recommended. V_2 (pin 2) requirement is 20 mA at a voltage between −6 and −12. V_3 (pin 10) is to be set 12 V more negative than V_2. For example, with V_2 set to −12 V, V_3 should be −24 V. The VV101A and VV100B each require about 8 mA from the V_3 supply. Proper bypass requires at least 6.8 μF tantalum capacitors to ground from pins 2, 12, (and 10 if three voltages are used) and 47 μF on pin 6. Minimum length leads should be employed. Be sure to observe proper polarity. See figure 1. Either VV100B or the VV101A can be operated with only two proper power supplies at the expense of rise time and linearity. For this configuration, tie pin 2 to pin 9, set $V_2 = -6$ V to −12 V, V_3 is omitted and $V_1 = +6$ V.

THE OUTPUT

The VV100 Series is optimized for a 25 Ω load in order to drive two 50 Ω cables simultaneously. If only one cable is to be driven, a 50 Ω resistor should be connected from the output of the VV100B to ground, to provide a net 25 Ω load. Other numbers of cables, and cables of impedances other than 50 Ω may be driven, always taking care to maintain the required 25 Ω through the use of additional series or shunt resistance. For example, three 91 Ω cables require an additional 142 Ω shunt to ground; five 50 Ω cables may be driven via five 75 Ω series resistors (yielding reduced gain and output swing as the price of the additional fanout). Driving loads other than 25 Ω will cause output shape and stability problems. Loads less than 25 Ω degrade risetime, gain, and linear range; loads larger than 25 Ω produce ringing and oscillation.

OUTPUT PROTECTION

The output of the VV100B is protected against sustained shorts to ground in the presence of dc inputs. The VV101A is not. This short circuit protection is implemented by an integrating stage which senses output current and limits it to an average current of 60 mA. The time constant of the limiting stage is approximately 6 μsec. The maximum pulse output current is a function of the input pulse width, amplitude and repetition rate.

When limiting occurs, this integrating stage must recover before linear operation may resume. Longer averaging times can be achieved by adding capacitance from pin 13 to ground. Current limiting may be defeated by a jumper from pin 2 to pin 13. Under this condition, safe operation requires $(V_{out}-V_2)\, i_{out} < 1$ w.

The limiting circuitry is based upon the average output current of the VV100B. The maximum output swing for pulses less than the average time will be

$$d_{max} = \frac{(60\text{ mA})}{D}$$

Here, D is the duty factor. For larger widths the VV100B output will begin to shut down after a time t_{limit} and approach 60 mA with a 6 μsec time constant.

TRIMS

Amplifiers in the VV100 Series require three separate trims: input dc level, output dc level, and fast compensation.* The values of these trims must be selected for each VV100B and hence must be reset if the VV100 is replaced. All trims should be made with the VV100 output loaded with 25 Ω.

The first trim, T1, is used to set the input dc offset. With no input to the VV100B, install a resistor between the input connector and a regulated negative supply. The value of the resistor should be chosen to set the input voltage to 0.0 mV. Typical values of this trim are 30 kΩ to 300 kΩ.

The second trim, T2, is used to set the output dc level to zero. This trim is a resistor from pin 1 to either the negative or positive supply, depending upon the polarity of the initial dc offset. Typical values of this trim are 100 kΩ to 1 MΩ.

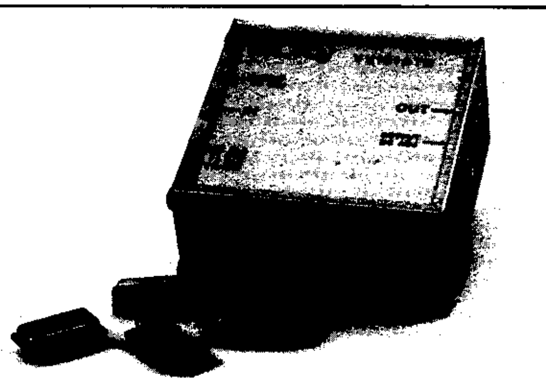
The last trim is an RC adjustment of the overshoot of the output. A 6-35 pF trimmer capacitor in series with a 25-100 Ω resistor is required to minimize the overshoot. Using a fast risetime input pulse, observe the output of the VV100B. Adjust the trim capacitor to give the best output pulse shape.

*Occasionally an additional slow compensation trim (T3) is required. To make this trim, a flat-topped pulse of about 10 μsec duration is applied to the VV100B or VV101A input. A resistor in the range of 10k to 300k connected from pin 1 to pin 4 (or ground as required) is used to trim the output pulse to a flat top.

ORDERING INFORMATION

The LeCroy Model VV100BTB/VV101ATB provides the high-bandwidth circuitry, shown in Figure 1, in a ready-to-use format. The 3 inch × 3 inch × 1.6 inch enclosure size of this device allows one to use the Model VV100B or VV101A in locations too small for many fast amplifiers. The amplifiers employ LEMO type coaxial cable connectors. The units may be purchased with a Model VV100B or VV101A. The trim and compensation variables are factory adjusted for optimum high-speed performance.

MODEL	DESCRIPTION
VV101A	Amplifier hybrid.
VV100B	Amplifier hybrid.
VV101ATB	VV101A mounted in circuit board. LEMO connectors.
VV100BTB	VV100B mounted in circuit board. LEMO connectors.



Models VV100BTB and VV100ATB wideband amplifier modules.

INTRODUCTION

The LeCroy Model VV100B is a hybrid circuit designed as a high bandwidth amplifier primarily intended for amplification of pulses from photomultiplier tubes. It has a fixed gain of 10 and a rise time of less than 2 nsec. The output is capable of driving two 50 Ω loads (25 Ω). The linear range of the VV100B is +200 mV to -5 V.

The user may supply suitable input impedance for his particular needs. The unit requires an input terminating resistor, power supply bypass capacitors, input and output DC trims and an output shape capacitive trim. See Figure 2 for an overall wiring diagram to be discussed below. Figure 1 shows the pin numbering scheme used on the VV100B and all other 16 pin DIP packages.

The VV100B contains circuitry which limits the average output current to 60 mA. The time constant of the limiting circuit is approximately 6 μsec. Performance details of this limiting scheme are contained in the VV100B data sheet.

LAYOUT

Because of the extremely high bandwidth of the VV100B, care should be used in layout of the printed circuit board. Continuous ground plane construction is essential. To ensure minimum inductance, low profile sockets like the TI or AUGAT should be used. Input busses should be separated from the output. Interconnections to other circuitry greater than 3 cm away should be made only by properly terminated coaxial cable. Input protection circuitry and bypass capacitors as described below should be located as close to the VV100B as possible.

THE INPUT

Proper termination and protection must be supplied to the input of the VV100B. In most cases, input to the amplifier will be via 50 Ω cable. In this case, a 50 Ω resistor from the input (pin 8) to ground should be employed. In addition, a pair of diodes to ground as shown in Figure 2 will provide protection. 1N4448 or equivalent diodes should be used. The input DC level must be trimmed to zero by a trim resistor (T1) to a negative supply. Where the best DC stability is required, this supply should be regulated. Note that fluctuations in the input offset will appear at the output of the VV100B amplified 10-fold.

POWER

The VV100B may be operated from either two or three DC supplies. In most applications two-voltage operation is recommended for the sake of convenience and lower power dissipation. Three-voltage operation provides slightly better linearity and slightly faster overload recovery at the cost of additional power, bypassing, and a third supply.

For two-voltage operation, +6 volts (pin 12) and -5 to -12 volts (pin 2) are required. Both supplies must deliver 20 mA. In this mode, pin 9 must be tied to pin 2. Pin 10 is not used. Proper bypass requires at least 6.8 µF tantalum capacitors to ground on pins 2 and 12, and 47 µF on pin 6. Be sure to observe proper polarity. See Figure 2.

In three-supply operation VV100B operation is optimized. Again 20 mA of +6 volts must be supplied at pin 12. In addition, two negative supplies, V2 and V3, are required. The V2 (pin 2) requirement is 20 mA at a voltage between -6 and -12. V3 (pin 10) is to be set 12 volts more negative than V2. The VV100B used in this mode requires 6 mA from the V3 supply. For example, with V2 set to -12 volts, V3 should be -24 volts. Proper bypass requires at least 6.8 µF tantalum capacitors to ground from pins 2, 10 and 12, and 47 µF on pin 6. Be sure to observe proper polarity. See Figure 2.

In either type of operation, the maximum linear output swing depends upon the voltage V2 at pin 2, ranging approximately linearly from -2 V for V2 = -6 volts to -5 volts for V2 = -12 volts. This linear range applies only for pulse duty cycles which do not activate the output limiting circuit.

THE OUTPUT

The VV100B is optimized for a 25 Ω load in order to drive simultaneously two 50 Ω cables. If only one cable is to be driven, a 50 Ω resistor should be connected from the output of the VV100B to ground, to provide a net 25 Ω load. Other numbers of cables, and cables of other impedances other than 50 Ω, may be driven, always taking care to maintain the required 25 Ω through the use of additional series or shunt resistance. For example, three 91 Ω cables require an additional 142 Ω shunt to ground; five 50 Ω cables may be driven via five 75 Ω series resistors (yielding, of course, reduced gain and output swing as the price of the additional fanout).

Driving loads other than 25 Ω will cause output shape and stability problems. Loads less than 25 Ω degrade rise time, gain, and linear range; loads larger than 25 Ω produce ringing and oscillation.

The output of the VV100B is protected against sustained shorts to ground in the presence of DC inputs. This short circuit protection is implemented by an integrating stage which senses output current and limits it to an average current at 60 mA. The time constant of the limiting stage is approximately 6 μsec, thus the maximum pulsed output current is a function of both the input pulse width, amplitude and repetition rate. Also, when limiting occurs this integrating stage must recover before linear operation may resume.

TRIMS

The VV100B requires three separate trims: input DC level, output DC level, and fast compensation.* The values of these trims must be selected for each VV100B and hence must be reset if the VV100B is replaced. All trims should be made with the VV100B output loaded with 25 Ω.

The first trim, T1, is used to set the input DC offset. With no input to the VV100B, install an input resistor between the input and a regulated negative supply. The value of the resistor should be chosen to set the input DC voltage to 0.0 mV. Typical values of this trim are 10 KΩ to 100 KΩ.

The second trim, T2, is used to set the output DC level to zero. This trim is a resistor from pin 1 to either the negative or positive supply, depending upon the polarity of the initial DC offset. Typical values of this trim are 100 KΩ to 1 MΩ.

The last trim is an RC adjustment of the overshoot of the output. A 6 to 35 pF trimmer capacitor in series with a 51 Ω resistor are used to set the overshoot. Using a fast rise time (≤2 nsec) input pulse, observe the output of the VV100B. Adjust the output capacitor to give the best output pulse shape.

* On some VV100B's, an additional slow compensation trim (T3) is required. To make this trim, a flat-topped pulse of about 10 μsec duration is applied to the VV100B and a resistor in the range of 10K to 100K (or sometimes larger) is connected from pin 1 to either pin 4 or ground as required to trim the output pulse to a flat top.

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APPLICATION INFORMATION

Figure 2 shows a typical application circuit and is the circuit on the LeCroy 1952 Test/Mounting board. Here input trim T1 is accomplished by the series combination of a 27 KΩ resistor and a 500 KΩ potentiometer. Trim T2 is set by the 1 MΩ potentiometer and series 100 KΩ fixed resistor. A fixed resistor to ground sets the low frequency gain trim.(T3) High frequency compensation is set by the 51 Ω,6-35 pF combination.

The internal current limiting may be defeated by placing a jumper between pins 13 and 2. This connection allows bipolar operation if an additional resistor(RA) is connected from the output to a positive supply voltage. All positive current delivered to the load is through this additional resistor. The DC value of this added current should be held to less than 40 mA.

If internal current limiting is not defeated, the maximum positive voltage excursion into a load RL is $V+Max = 6 \frac{RL}{RP+RL}$. The most negative will be given by $V-Min = V+Max - \left(\frac{RP\ RL}{RP+RL}\right)(.06)$ with the additional limitation that

$V-Min \geq -5$ volts.

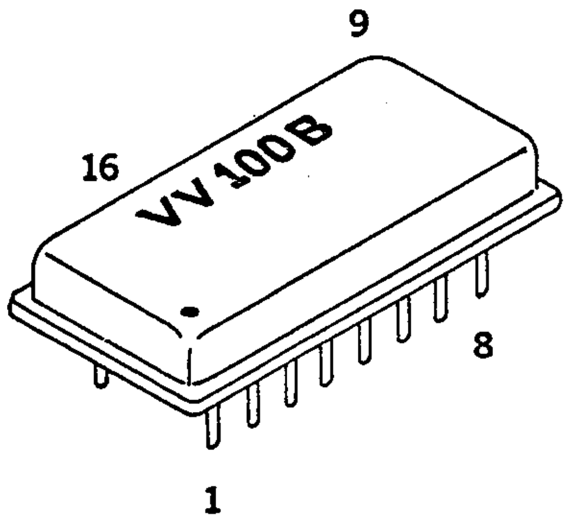

FIGURE 1

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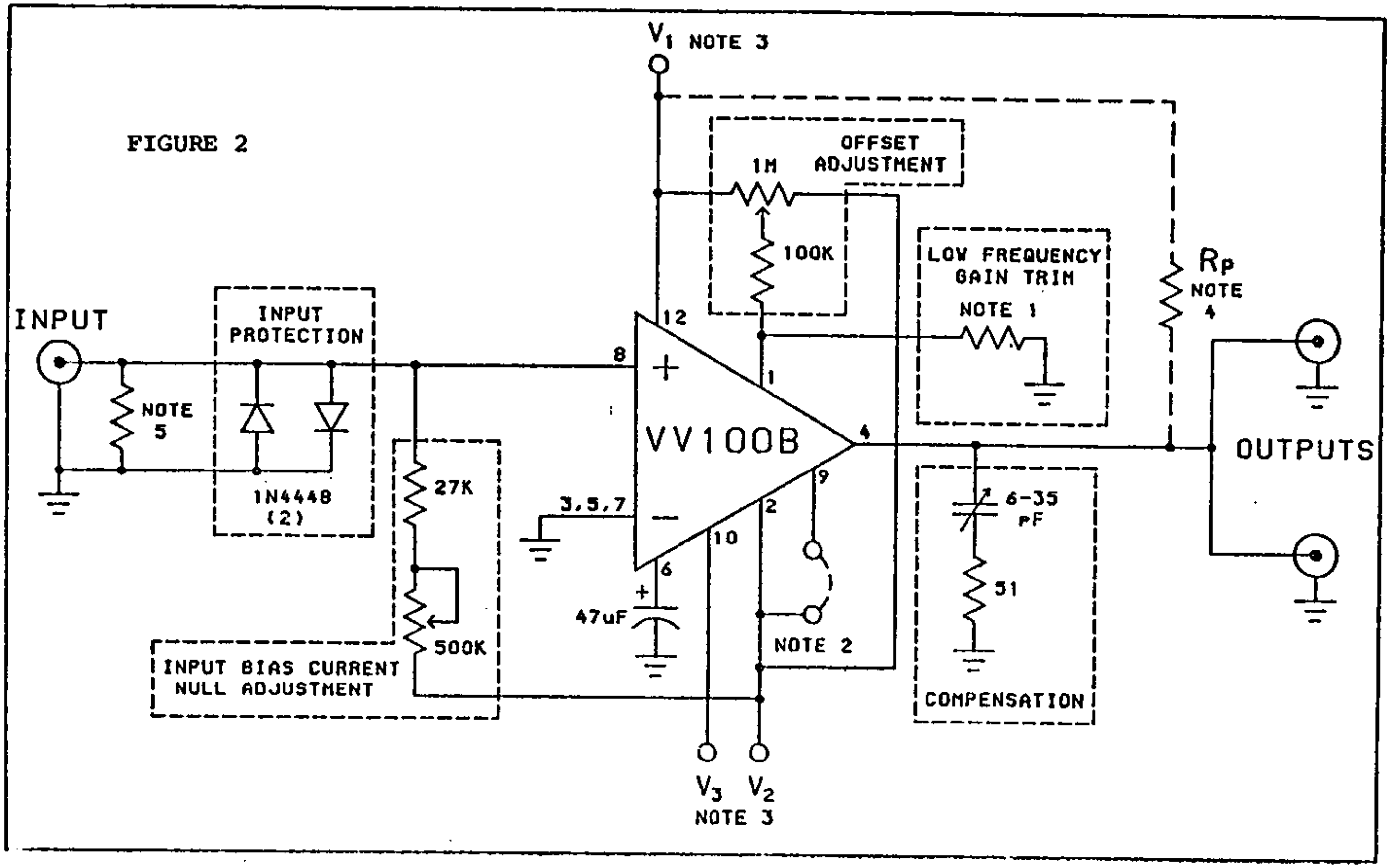
FIGURE 2



NOTES:

1) Typical value = 7.5 KΩ
2) For two power supply operation connect jumber between pins 2 & 9, leaving pin 10 open.
3) All power supply voltage lines should include a high frequency bypass typically a 6.8 μF cap to gnd. and a 50 μH series choke.

Two supply operation:
- V_1= +6 V
- V_2= -6 V to -12 V
- V_3 , not used

Three supply operation:
- V_1= +6 V
- V_2= -6 V to -12 V
- V_3= 12 V more negative than V_2.

4) Optional pull-up for extended positive voltage excusions. This configuration reduces the max. output current according to: $I_{max} = I_o - \frac{6000\,(mA)}{R_P}$, where $I_o = \begin{cases} 60\text{ mA, steady} \\ 200\text{ mA, pulsed} \end{cases}$.
5) Input termination resistor, chosen to match input cable inpedance.

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