2249A, 2249SG and 2249W

12-CHANNEL ADC

April, 1984

WARRANTY

LeCROY RESEARCH SYSTEMS CORP. warrants each instrument it manufactures to be free from defects in material and workmanship under normal use and service for the period of 1-year from date of purchase. Custom monolithics and hybrids sold separately and all spare or replacement parts are warranted for 90-days. This warranty extends only to the original purchaser. This warranty shall not apply to fuses, disposable batteries or any product or parts which have been subject to misuse, neglect, accident or abnormal conditions of operations.

In the event of failure of a product covered by this warranty, LeCroy will repair and calibrate an instrument returned to the factory or an authorized service facility within 1 year of the original purchase; provided the warrantor's examination discloses to its satisfaction that the product was defective. The warrantor may, at its option, replace the product in lieu of repair. With regard to any instrument returned within one year of the original purchase, said repairs or replacement will be made without charge. If the failure has been caused by misuse, neglect, accident or abnormal conditions or operations, repairs will be billed at a nominal cost. In such case, an estimate will be submitted before work is started, if requested.

The foregoing warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness or adequacy for any particular purpose or use. LeCroy Research Systems Corp., shall not be liable for any special, incidental or consequential damages, whether in contract, tort or otherwise.

IF ANY FAILURE OCCURS, notify LeCroy Research Systems Corp., or the nearest service facility, giving full details of the difficulty, and include the Model number, serial number, and FAN (Final Assembly Number) or ECO (Engineering Change Order) number. On receipt of this information, service data or shipping instructions will be forwarded to you. On receipt of the shipping instructions, forward the instrument, transportation prepaid. A Return Authorization number will be given as part of shipping instructions. Marking this RA number on the outside of the package will insure that it goes directly to the proper department within LeCroy. Repairs will be made at the service facility and the instrument returned, transportation prepaid.

ALL SHIPMENTS OF LeCROY INSTRUMENTS FOR REPAIR OR ADJUSTMENT should be made via Air Freight or "Best Way" prepaid. The instrument should be shipped in the original packing carton; or if it is not available, use any suitable container that is rigid and of adequate size. If a substitute container is used, the instrument should be wrapped in paper and surrounded with at least four inches of excelsior or similar shock-absorbing material.

IN EVENT OF DAMAGE IN SHIPMENT to original purchaser the instrument should be thoroughly inspected immediately upon original delivery to purchaser. All material in the container should be checked against the enclosed packing list. The manufacturer will not be responsible for shortages against the packing sheet unless notified immediately. If the instrument is damaged in any way, a claim should be filed with the carrier immediately. (To obtain a quotation to repair shipment damage, contact the LeCroy factory or the nearest service facility).

DOCUMENTATION DISCREPANCIES OR OMISSIONS. LeCroy Research Systems is committed to providing unique, reliable, state-of-the-art instrumentation in the field of high-speed data acquisition and processing. Because of this commitment, the Engineering Department at LeCroy is continually refining and improving the performance of products. While the actual physical modifications or changes necessary to improve a model's operation can be implemented quite rapidly, the corrected documentation associated with the unit usually requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying unit. There may be small discrepancies that were brought about by customer-prompted engineering changes or by changes determined during calibration in our Test Department. These differences usually are changes in the values of components for the purposes of pulse shape, timing, offset, etc., and only rarely include minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry. Whenever original discrepancies exist, fully updated documentation should be available upon your request within a month after your receipt of the unit.

ANY APPLICATION OR USE QUESTIONS, which will enhance your use of this instrument will be happily answered by a member of our Engineering Services Department, telephone 914-425-2000 or your local distributor. You may address any correspondence to:

LeCroy Research Systems Corp., 700 S. Main Street,
Spring Valley, New York 10977, ATTN: Engineering Services Dept. or
LeCroy Research Systems Corp., 14800 Central S.E.,
Albuquerque, New Mexico 87123

European Customers can contact:

LeCroy Research Systems Ltd.
Elms Court
Botley
Oxford OX9 2LP England

LeCroy Research Systems SA
Rue Cardinal-Journet 27
1217 Meyrin 1-Geneva
Switzerland

LeCroy Research Sys. S.a.r.l.
Avenue Du Parana
Z.A. De Courtaboeuf
F-91940 Les Ulis, France

LeCroy Research Systems GmbH
Treitschkestrasse 3
Postfach 10 37 67
69 Heidelberg
West Germany

A T T E N T I O N

GATE INPUTS OF THE 2249SG MUST BE DOUBLE NIM AMPLITUDE (-1.4 VOLTS). SEE SECTION 2.3.

CRATE POWER SHOULD BE TURNED OFF DURING INSERTION AND REMOVAL OF UNIT TO AVOID POSSIBLE DAMAGE CAUSED BY MOMENTARY MISALIGNMENT OF CONTACTS.

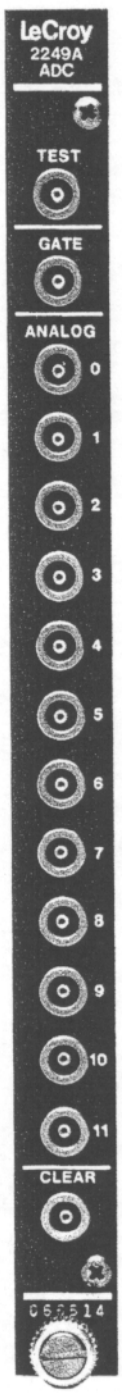
SEE POCKET IN BACK OF MANUAL FOR SCHEMATICS, PARTS LISTS, AND ADDITIONAL ADDENDA WITH ANY CHANGES TO MANUAL.

A T T E N T I O N

TABLE OF CONTENTS

TECHNICAL DATA

LeCroy



CAMAC Model 2249A

12 Channel A-to-D Converter

FEATURES:

- **COMPACT PACKAGING**
  12 channels per single-width module means fewer crates, smaller systems, less gate fan-out.
- **WELL-CONTROLLED PEDESTAL**
  Advanced hybrid circuit front end eliminates peak shifts and/or constant calibration.
- **EXCELLENT INPUT IMPEDANCE MATCH**
  Minimizes possibility of digitizing input reflections.
- **10-BIT RESOLUTION**
  One part in 1024.
- **WIDEST DYNAMIC RANGE**
  4 times the range of 8-bit ADC's allows broader spectra, better accuracy, simplified setup, prevents small gain shifts from exceeding range of ADC.
- **HIGH SENSITIVITY**
  0.25 picocoulomb per count.
- **NO FEEDTHROUGH**
  Up to 1,000-fold overloads are rejected by fast gate, eliminating spurious data due to out-of-time chamber firings, noise, etc.
- **UNIFORM SENSITIVITY THROUGHOUT GATE INTERVAL**
  No modulation of measurement with position of signal within gate.
- **NO INTERCHANNEL CROSSTALK**
  regardless of input amplitude.
- **WELL-VENTILATED MODULE**
  Low component count, less than one-fifth of competing designs, permits free circulation of air for cooler, more reliable, and longer-lasting operation.
- **FAST CLEAR INPUT**
  enables fast rejection of unwanted data.
- **FULL TEST CAPABILITY**
  F(25) simultaneously injects charge into all ADC's proportional to DC level on front panel (or patch pins on Dataway).
- **FULL LAM FUNCTIONS.**
- **HIGH DIGITIZING SPEED**
  without sacrifice in differential linearity.
- **LAM AND Q SUPPRESSION**
  eliminates readout of empty modules.

The LRS Model 2249A 12-Channel Analog-to-Digital Converter embodies all the operational characteristics which have proved important for general-purpose use in high energy particle physics, including expanded resolution (0.1%), higher sensitivity, excellent stability, faster digitizing rate, LAM and Q suppression, provision for fast clear, calibrating test mode, and flexible LAM options.

These ADCs are specifically intended for use in demanding applications such as particle identification using dE/dx counters, recording x-ray, neutron, or recoil proton energies using lead glass or other total energy absorbtion counters, improving time resolution by correcting for slewing due to variances in counter output amplitudes, monitoring gas threshold Cerenkov counters, and debugging or monitoring proportional or drift chambers.

The Model 2249A contains twelve complete ADC's in a single-width CAMAC module. Each ADC offers a resolution of ten bits to provide 0.1% resolution over a wide 1024-channel dynamic range. The factor of 4 wider range allows operations with broad signal spectra such as are encountered in experiments anticipating fractionally charged particles or covering extensive energy ranges. It also greatly reduces the necessity for careful adjustment of signal strengths to match the limited range of an 8-bit, 256-channel instrument. The input sensitivity of the Model 2249A is 0.25 pC/count for a full-scale range of 256 pc. This is compatible with most available signal sources and no additional buffering or reshaping of any kind is required to digitize nanosecond pulses.

The excellent long-term stability, temperature characteristics, and isolation between ADC channels assure accurate and reliable performance under the demanding conditions encountered in actual experiments. Confirmation of operation and calibration is provided by the unique test feature which allows all twelve ADC's or an entire system to simultaneously digitize a charge proportional to a dc level provided to a front-panel Lemo connector or patched into P_1, P_2 or P_5 of the Dataway connector.

The Model 2249A offers excellent event rate capability through the incorporation of a fast clear and a fast digitizing rate. The fast clear input enables the ADC to begin digitizing on the command of a prompt gate and be reset, if necessary, before the end of conversion on the basis of delayed logic or chamber information. This feature eliminates the long input delay cables now required in these situations.

End of conversion of modules which contain data is flagged by generation of a CAMAC LAM. Readout of modules which do not contain information can be eliminated either by use of the LAM signals or through Q suppression.

August 1982

Innovators in Instrumentation

LeCROY RESEARCH SYSTEMS CORPORATION • 700 SOUTH MAIN STREET • SPRING VALLEY, N.Y. 10977
TWX: 710-577-2832 CABLE: LERESCO TELEPHONE: (914) 425-2000

SPECIFICATIONS
Model 2249A
12 CHANNEL ADC

Analog Inputs: Twelve; Lemo-type connectors; charge-sensitive (current-integrating); direct-coupled, quiescently at approximately +4 mV; 50 Ω impedance; linear range normally −2 mV to −1 V; protected to ± 50 volts against 1 μsec transients.

Full-Scale Range: 256 pC ± 5%.

Full-Scale Uniformity: ± 5%.

Integral Non-linearity: ± .25% of reading ± 0.5 pC (12 pC to 256 pC) for >500 Ω source.

ADC Resolution: 10 bits actual, (0.1%).

Long-Term Stability: Better than 0.25% of reading ± 0.5 pC/week (at constant temperature).

Temperature Coefficient: Typical, 0; max., ± [.03% of reading (in pC) + .002t] pC/°C (where t = gate duration in nanoseconds, with 50Ω reverse termination).

ADC Isolation: A 5-volt, 20 ns overload pulse in any one ADC disturbs data in any other ADC by no more than 0.25 pC.

Gate Input: One gate common to all ADC's; LEMO-type connectors; 50 Ω impedance; −600 mV or greater enables; minimum duration, 10 ns; maximum recommended duration, 200 ns (actual limit approximately 2 microseconds with reduced accuracy; partial analog input must occur within 0.5 μsec after opening gate to preserve accuracy), effective opening and closing times: 2 ns; internal delay, 2 ns.

Fast Clear: One front-panel input common to all ADC's; LEMO-type connector; 50 Ω impedance; −600 mV or greater clears, minimum duration, 50 ns. (Caution: narrower pulses cause partial clearing.) Requires additional 2.0 μs settling time after clear.

Residual Pedestal: Typically 1 + 0.03t picocoulombs (where t = gate duration in nanoseconds) with 50 Ω reverse termination.

Test Function: With CAMAC I present, the positive DC level applied to front panel "Test" input (internal high impedance connection to +12 volts) or optional rear connector P1, P2, or P5 patch points will inject charge with a proportionality constant of −12.5 pC/volt into all inputs at F(25) • S2 time. (With CAMAC I not present, F(25) • S2 will generate the ≈80 ns gate only, providing a measure of residual pedestal only.)

Digitizing Time: 60 μs. By factory option, 8-bit operation at 12.5 μs digitizing time may be provided.

Readout Time: Readout may proceed at the fastest rate permitted by the CAMAC standard after digitization is complete.

Readout Control: Ready for readout when LAM signal appears. Refer to ESONE Committee Report EUR4100e and EUR4600e for additional timing details, voltages, logic levels, impedances, and other standards.

Data: The proper CAMAC function and address command normally gates the 10 binary bits plus overflow bit of the selected channel onto the R1 to R11 (2^0 to 2^{10}) Dataway bus lines.

CAMAC Commands:

Z or C: ADC's and LAM are cleared by the CAMAC "Clear" or "Initialize" command; requires S2. Z also disables LAM.
I: Gate input is inhibited during CAMAC "Inhibit" command. (Test Function is enabled.)
Q: A Q=1 response is generated in recognition of an F(0) or F(2) Read function or an F(8) function if LAM is set for a valid "N" and "A", but there will be no response (Q=0) under any other condition. The Q response for empty modules can be suppressed. (See Q and LAM suppression.)
X: An X=1 (Command Accepted) response is generated when a valid F, N, and A command is generated.
L: A Look-At-Me signal is generated from end of conversion until a module Clear or Clear LAM. LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable and Disable function command, and can be tested by Test LAM. Standard option causes LAM to be suppressed for empty modules.

CAMAC Function Codes:

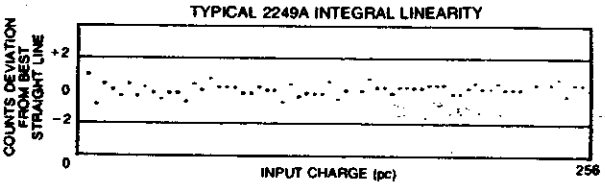
F(0): Read registers; requires N and A, A(0) through A(11) are used for channel addresses.
F(2): Read registers and Clear module and LAM; requires N and A; (Clears on A(11) only.)
F(8): Test Look-At-Me; requires N and any A from A(0) to A(11) independent of Disable Look-At-Me. Q response is generated if LAM is set.
F(9): Clear module and LAM; requires N, S2, and any A from A(0) to A(11).
F(10): Clear Look-At-Me; requires N, S2, and any A from A(0) to A(11).
F(24): Disable Look-At-Me; requires N, S2, and any A from A(0) to A(11).
F(25): Test module; requires N, S2, and any A from A(0) to A(11).
F(26): Enable Look-At-Me; requires N, S2, and any A from A(0) to A(11). Remains enabled until Z or F(24) applied.
Caution: The state of the LAM mask will be arbitrary after power turn-on.

Q and LAM Suppression: Adjustable potentiometer (accessed from side of module) sets count level required (from 0 to 100) before data is considered useful. A module in which all channels contain less than set amount will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The LAM suppress portion can be disabled with a solder jumper option.

Packaging: In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e). RF shielded CAMAC #1 module.

Current Requirements: +24 V at 35 mA; −24 V at 15 mA; +6 V at 850 mA; −6 V at 200 mA.

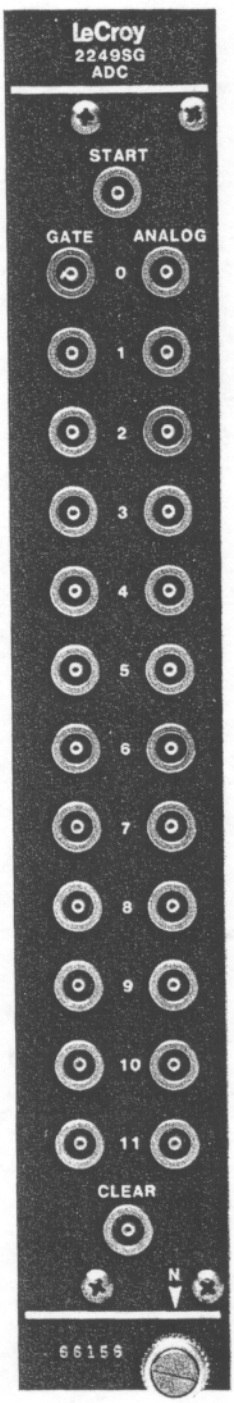
TYPICAL 2249A INTEGRAL LINEARITY



SPECIFICATIONS SUBJECT TO CHANGE.

TECHNICAL DATA

LeCroy



CAMAC Model 2249SG

12-Channel A-to-D Converter With Separate Gates

The LeCroy Model 2249SG 12-Channel Analog-to-Digital Converter is a separately gated version of the world's most widely used integrating ADC, the Lecroy Model 2249A. It embodies all the operational characteristics which have proved important for general-purpose use in high energy particle physics, including high resolution, high sensitivity, excellent stability, fast digitizing rate, LAM and Q suppression, provision for fast clear, calibrating test mode, and flexible LAM options.

The Model 2249SG contains twelve complete ADC's in a double-width CAMAC module. Each ADC offers a 10-bit conversion to provide a wide 1024-channel dynamic range. The input sensitivity of the Model 2249SG is 0.25 pC/count for a full-scale range of 256 pC. This is compatible with most available signal sources and no additional buffering or reshaping of any kind is required to digitize nanosecond pulses.

The excellent long-term stability, temperature characteristics, and isolation between ADC channels assure accurate and reliable performance under the demanding conditions encountered in actual experiments. Confirmation of operation and calibration is provided by a unique optional test feature which allows all twelve ADC's or an entire system to simultaneously digitize a charge proportional to a dc level provided to a front-panel Lemo connector or patched into P_1, P_2, or P_5 of the Dataway connector.

The Model 2249SG offers excellent event rate capability through the incorporation of a fast clear and a fast digitizing rate. The fast clear input enables each ADC to begin digitizing on the command of a prompt gate and be reset, if necessary, before the end of conversion on the basis of delayed logic or chamber information. This feature eliminates the long input delay cables now required in these situations.

End of conversion of modules which contain data is flagged by generation of a CAMAC LAM. Readout of modules which do not contain information can be eliminated either by use of the LAM signals or through Q suppression.

November 1982

Innovators in Instrumentation

LeCROY RESEARCH SYSTEMS CORPORATION • 700 SOUTH MAIN STREET • SPRING VALLEY, N.Y. 10977
TWX: 710-577-2832 CABLE: LERESCO TELEPHONE: (914) 425-2000

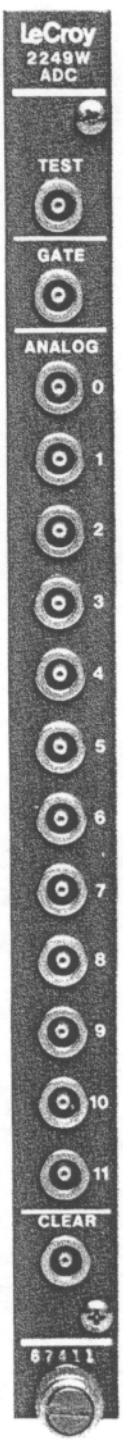
SPECIFICATIONS
MODEL 2249SG
12-CHANNEL ADC WITH SEPARATE GATES

Analog Inputs:	Twelve, Lemo-type connectors; charge-sensitive (current-integrating); direct-coupled, quiescently at approximately +4 mV; 50 Ω impedance; linear range normally −2 mV to −1 V; protected to ± 50 volts against 1 μsec transients.
Full-Scale Range:	256 pC ± 5%.
Full-Scale Uniformity:	± 5%.
Integral Non-linearity:	± 0.25% of reading ± 0.5 pC for > 500 Ω source.
ADC Resolution:	10 bits (0.1%) somewhat degraded to approx. 0.2% by clock unsynchronized with any specific linear gate input.
Long-Term Stability:	Better than 0.25% of reading ±0.5 pC/week (at constant temperature).
Temperature Coefficient:	Typical, 0; max., ±(.03% of reading (in pC) +0.002 t) pC/°C (where t=gate duration in nanoseconds, with 50 Ω reverse termination).
ADC Isolation:	A 5-volt, 20 nsec overload pulse in any one ADC disturbs data in any other ADC by no more than 0.25 pC.
Gate Inputs:	Twelve, one per ADC; Lemo-type connectors; 50 Ω impedance; −1.4 V or greater enables; minimum duration, 10 nsec; maximum recommended duration, 200 nsec (actual limit approximately 2 microseconds with reduced accuracy; partial analog input must occur within 0.5 μsec after opening each gate to preserve accuracy), effective opening and closing times; 2 nsec; internal delay, 2 nsec. All gates should occur within 2 μsec of the "start" pulse (other arrangements require internal resistor change). CAUTION: Subsequent gate signals are NOT INHIBITED after receipt of the first one, so care must be taken to externally prevent the application of more than one gate to each channel until a clear is applied.
Start Input:	A NIM level (> −600 mV) signal of a duration exceeding 10 nsec must be applied to start the internal oscillator. It should be applied simultaneous to the earliest gate pulse or should follow it by no more than 100 nsec.
Fast Clear:	One front-panel input common to all ADC's; Lemo-type connector 50 Ω impedance; −600 mV or greater clears, minimum duration, 50 nsec. (Caution: narrower pulses cause partial clearing.) Requires additional 1.5 μsec settling time after clear.
Test Function:	The standard 2249SG does not respond to F(25) and has no test feature. However, on-line test capability is optional at the expense of the CAMAC "Inhibit". With Q7 (the "inhibit" transistor) removed, the leading edge of a pulse applied to the "start" input will cause a fixed charge to be injected onto the 2249SG analog inputs. Coincident with the "start," the 12 gate pulses must be applied of duration approximately 80 nsec. Proportionality constant is −12.5 pC/volt of dc signal applied to P1, P2 or P5 patch points, for an 80 nsec gate. In this test mode, the gates must precede the "start" by 10 nsec.
Digitizing Time:	Approximately 60 μsec.
Readout Time:	Readout may proceed at the fastest rate permitted by the CAMAC standard after digitization is complete.
Readout Control:	Ready for readout when LAM signal appears. Refer to ESONE Committee Report EUR4100e and EUR4600e or IEEE #583 for additional timing details, voltages, logic levels, impedances, and other standards.
Data:	The proper CAMAC function and address command normally gates the 10 binary bits plus overflow bit of the selected channel onto the R1 to R11 (2^0 to 2^{10}) Dataway bus lines.
CAMAC Commands:	Z or C: ADC's and LAM are cleared by the CAMAC "Clear" or "Initialize" command; requires S2. Z also disables LAM. I: Gate input is inhibited during CAMAC "Inhibit" command. (Nonfunctional if unit is modified to provide "Test" feature.) Q: A Q=1 response is generated in recognition of an F(0) or F(2) Read function or an F(8) function if LAM is set for a valid "N" and "A", but there will be no response (Q=0) under any other condition. The Q response for empty modules can be suppressed. (See Q and LAM suppression.) X: An X=1 (Command Accepted) response is generated when a valid F, N, and A command is generated. L: A Look-At-Me signal is generated from end of conversion until a module Clear or Clear LAM. LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable and Disable function command, and can be tested by Test LAM. Standard option causes LAM to be suppressed for empty modules.
CAMAC Function Codes:	F(0): Read registers; requires N and A, A(0) through A(11) are used for channel addresses. F(2): Read registers and Clear module and LAM; requires N and A; (Clears on A(11) only.) F(8): Test Look-At-Me; requires N and any A from A(0) to A(11) independent of Disable Look-At-Me. Q response is generated if LAM is set. F(9): Clear module and LAM; requires N, S2, and any A from A(0) to A(11). F(10): Clear Look-At-Me; requires N, S2, and A from A(0) to A(11) F(24): Disable Look-At-Me; requires N,S2, and any A from A(0) to A(11). F(26): Enable Look-At-Me; requires N, S2, and any A from A(0) to A(11). Remains enabled until Z or F(24) applied. Caution: The state of the LAM mask will be arbitrary after power turn-on.
Q and LAM Suppression:	Adjustable potentiometer (accessed from side of module) sets count level required (from 0 to 100) before data is considered useful. A module in which all channels contain less than set amount will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The LAM suppress portion can be disabled with a solder jumper option.
Packaging:	In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e or IEEE Report #583). RF-shielded CAMAC #2 module.
Current Requirements:	+24 V at 35 mA; −24 V at 15 mA; + 6 V at 850 mA; −6 V at 200 mA.

SPECIFICATIONS SUBJECT TO CHANGE

TECHNICAL DATA

LeCroy



CAMAC Model 2249W
12 Channel Analog-to-Digital Converter

The LeCroy Model 2249W is a 12 channel, 11-bit integrating-type analog-to-digital converter. It features excellent linearity and unprecedented stability, thus allowing operation at wide gates of up to 10 μsec. Thus, the 2249W is compatible with CsI and NaI crystal detectors. Its minimum gate of 30 nsec makes its use with organic scintillators and Cerenkov detectors possible in all but the highest rate conditions.

The 2249W has been optimized for dynamic range and linearity. By AC-coupling the input, 11-bit (1980 counts) operation has been achieved with ± 2 count integral linearity. This excellent linearity is maintained from the smallest signal size to signals as large as -2 V.

The test feature allows all 12 ADC's to simultaneously digitize a charge proportional to a DC level provided to a front-panel connector or patched into the CAMAC Dataway connector. In addition, the pedestals alone can be checked on-line by the same test feature by removing the CAMAC inhibit (I) during the test.

The Model 2249W offers an excellent event rate capability through the incorporation of a 2 μsec fast clear, which permits the ADC's to begin digitizing and then be cleared upon receipt of later trigger information rather than delaying the analog signals with long cables while the trigger decision is being made. In addition, rapid readout is made possible by a convenient Q and LAM suppress feature, side-panel adjustable between 0 and 100 counts. This feature permits an empty 2249W to be overlooked in a CAMAC readout cycle.

Innovators in Instrumentation

LeCROY RESEARCH SYSTEMS CORPORATION • 700 SOUTH MAIN STREET • SPRING VALLEY, N.Y. 10977
TWX: 710-577-2832 CABLE: LERESCO TELEPHONE: (914) 425-2000

SPECIFICATIONS
CAMAC Model 2249W
12 CHANNEL ANALOG-TO-DIGITAL CONVERTER

Analog Inputs:	12; Lemo type connectors; charge sensitive (current integrating); AC coupled (2 msec time constant, field changeable); 50 Ω impedance; linear range normally 0 to − 2.0 V; protected to ± 50 V against 1 μsec transients.
Gain:	− 0.25 pC/count ± 5%
Full-Scale Range:	Approximately − 500 pC (maximum count ≅ 1980)
Integral Non-Linearity:	± 0.05% ± (0.5 pC + 0.1%)
ADC Resolution:	0.05% (1980 total counts)
Long Term Stability:	Better than 0.25% of reading ± 0.5 pC/week (at constant temperature)
ADC Isolation:	A 5 V, 20 nsec overload pulse in any one ADC disturbs data in any other ADC by no more than 0.5 pC (2 counts).
Gate Input:	One gate common to all ADC's; Lemo type connector; 50 Ω impedance; − 600 mV or greater enables; minimum duration, 30 nsec; maximum recommended duration up to 10 μsec; partial analog input must occur within 0.5 μsec after opening gate to preserve accuracy; effective opening and closing times, 5 nsec; internal delay, 7 nsec.
Fast Clear:	One front panel input common to all ADC's Lemo type connector; 50 Ω impedance; − 600 mV or greater clears, minimum duration, 50 nsec. Requires additional 2.0 μ sec settling time.
Pedestal:	Adjustable over approximately 100 counts via side-panel accessed trimmer capacitor. Somewhat higher for wide gate.
Test Function:	With CAMAC I present, the positive DC level applied to front panel "Test" input (internal high impedance connection to + 12 V) or optional rear connector P1, P2, or P5 patch points will inject charge with a proportionality constant of − 15 pC/V into all inputs at F(25)•S2 time. (With CAMAC I not present, F(25)•S2 will generate the gate only, providing a measure of the pedestal.)
Digitizing Time:	106 μsec
Readout Time:	Readout may proceed at the fastest rate permitted by the CAMAC standard after digitization is complete.
Readout Control:	Ready for readout when LAM signal appears. Refer to ESONE Committee Report EUR4100e and EUR4600e for additional timing details, voltages, logic levels, impedances, and other standards.
Data:	The proper CAMAC function and address command normally gates the 11 binary bits of the selected channel onto the the R1 to R11 (2^0 to 2^{10}) Dataway bus lines.
CAMAC Commands:	Z or C: ADC's and LAM are cleared by the CAMAC "Clear" or "Initialize" command; requires S2. Z also disables LAM. I: Gate input is inhibited during CAMAC "Inhibit" command. (Test function is enabled.) Q: A Q = 1 response is generated in recognition of an F(0) or F(2) Read function or an F(8) function if LAM is set for a valid "N" and "A", but there will be no response (Q = 0) under any other condition. The Q response for empty modules can be suppressed (see Q and LAM suppression). X: An X = 1 (Command Accepted) response is generated when a valid F, N, and A command is generated. L: A Look-At-Me signal is generated from end of conversion until a module Clear or Clear LAM. LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable and Disable function command, and can be tested by test LAM. Standard option causes LAM to be suppressed for empty modules.
CAMAC Function Codes:	F(0): Read registers; requires N and A; A(0) through A(11) are used for channel address. F(2): Read registers and Clear module and LAM; requires N and A: (clears on A(11) only). F(8): Test Look-At-Me; requires N and any A from A(0) to A(11) independent of Disable Look-At-Me. Q response is generated if LAM is set. F(9): Clear module and LAM: requires N, S2, and any A from A(0) to A(11). F(10): Clear Look-At-Me; requires N, S2 and any A from A(0) to A(11). F(24): Disable Look-At-Me; requires N, S2, and any A from A(0) to A(11). F(25): Test module; requires N, S2 and any A from A(0) to A(11). F(26): Enable Look-At-Me; requires N, S2 and any A from A(0) to A(11). Remains enabled until Z or F(24) applied. Caution: the state of the LAM mask will be arbitrary after power turn-on.
Q and LAM Suppression:	Adjustable potentiometer (accessed from side of module) sets count level required (from 0 to 100) before data is considered useful. A module in which all channels contain less than set amount will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accept response is still generated. The LAM suppress portion can be disabled with a solder jumper option.
Packaging:	In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e). RF shielded CAMAC #1 module.
Current Requirements:	143 mA at + 24 V; 75 mA at − 24 V; 725 mA at + 6 V; 155 mA at − 6 V

SPECIFICATIONS SUBJECT TO CHANGE

SECTION 2

OPERATING INFORMATION

2.1 General

The LeCroy Model 2249 Series 12-Channel ADC contains 12 complete analog-to-digital converters in a CAMAC module. The 2249A and SG offer 10 bits, and the W version offers 11 bits. The analog-to-digital conversion is accomplished by the Wilkinson-rundown method, which ultimately yields a digital output (in TTL negative logic binary format) which is proportional to the integral of the charge in the input pulse. By the Wilkinson technique, the input charge is delivered to an integrating capacitor from a linear gate, and then discharged at A constant rate. During the time this rundown is taking place, pulses from an oscillator are gated into a scaler resulting in the final count proportional to the charge originally stored in the capacitor.

2.2 Analog Inputs

The 12 analog inputs of the 2249 Series are of 50 Ω impedance and accept negative-going pulses only during an externally applied gate. To assure performance within the linear range, input signals should not exceed -1 volt for the 2249A and SG, or -2V for the W version. The actual amount of input charge that yields a full scale digital output (1024 counts) is 256 picocoulombs (or 12.8 volt-nsec) for the 2249A and SG; 512 pC (25.6 volt-nsec) for the W version. The full scales of the 12 channels of each 2249 are set up to match within ±5% of each other. Quiescent DC level of the analog inputs of the 2249A and SG are set at approximately +4 mV to assure that it does not go negative should any drift occur. The 2249W is AC coupled and does not require this critical biasing.

2.3 Gate

The built-in linear gate is common to all 12 analog inputs of the A and W, necessitating that analog-to-digital conversion for all channels be done in parallel. The 50 Ω impedance gate input of the 2249A and 2249W accepts pulses $\geq$ -600 mV in amplitude (the 2249SG requires twice this amplitude for the gate input as explained below). The gate duration may be between 10 nsec and 200 nsec for the 2249A and 2249SG (see next paragraph). The 2249 W may be used with gate widths between 30 nsec and 10 μsec. Because of the finite risetime and falltime of the internal gate pulse, the effective gating interval is not adequately defined to allow input gate pulses shorter than 10 nsec. The actual gate opening and closing times are approximately 4 nsec, and therefore the gate should precede the analog inputs by at least 4 nsec (A and SG versions) or 7 nsec (W version). Except when photomultiplier noise is a prime consideration, it is good practice to apply a gate pulse which is wider than the expected duration of the longest analog input. IMPORTANT NOTE - The duration of the effective gate will exceed that of the gate pulse by 4 nsec for the A and SG versions and 5 nsec for the W version. The 2249SG gate inputs require -1.4 V to be enabled. Deviations from this amplitude will result in pedestal variations as the charge injection is controlled by the gate pulse. The gate inputs are terminated in 50 Ω allowing one half of the 32 mA current source

output of a NIM module (such as the LeCroy Models 429A or 821) to be employed. The second half of the bridged pair should not be terminated in 50 Ω.

For the 2249A and SG, gate widths exceeding 200 nsec create excessive residual pedestal (1 + 0.03 t/pC, where t = gate duration in nsec) and reduce the overall accuracy of the ADC by magnifying the effects of the instability manifest in the temperature coefficient, which is directly dependent upon the gate width. That maximum is ± (.03% of the reading in pC + .002 t)pC/°C). In addition, longer gates will imply an increased susceptability to any DC offset of the analog input. The actual limit of the gate duration is 2 μsec provided the resultant decrease in accuracy can be tolerated. With a gate duration of >200 nsec, it is recommended that the inputs be AC-coupled if possible.

The excellent stability and linearity of the Model 2249W allows it to be used with gate widths up to 10 μsec. In order to maintain this linearity with wide gates, however, it is necessary for the input pulse to occur within 500 nsec of the gate opening. During this 500 nsec period, a fixed amount of charge is automatically injected onto the integrating capacitor to assure linear operation even for very small input charges which would otherwise deviate from the linearity maintained by the circuit for larger input charges. This injection lasts approximately 500 nsec, but the appearance of charge from the analog input will cause it to be extended. Without input charge appearing, the q inject will cease after 500 nsec (i.e., charge added will settle out), and subsequent input charge would be subject to a conversion graph which is non-linear at the low end (i.e., for small input charges).

Similarly, if it is necessary to use wide gates (>200 nsec) and the 2249W is not available, the 2249A may be used with reduced accuracy. In this case, the analog input should also occur within 500 nsec after the gate opening.

The 2249 Series gate is inhibited from shortly (100 nsec) after the trailing edge of the gate until any CAMAC clear (C, Z, F(9) or F(2)·A(11)) or a front panel clear is applied. This effectively locks out spurious analog signals and noise from the ADC while the desired signal is being processed. The ADC's internal oscillator is synchronized with the leading edge of the gate pulse (although it occurs somewhat later), eliminating inaccuracies which could be caused by the utilization of free-running oscillators.

2.4 Start Input (2249SG Only)

Because the gate inputs of the 2249SG are considered asynchronous, a separate signal is required to start the internal oscillator. This pulse should be a NIM level applied either simultaneously with the earliest gate pulse or should follow it by ≤ 100 nsec. The pedestal of a given channel will decrease by 1 count per 50 nsec start delay, with respect to the Gate time.

2.5 Fast Clear

A front panel fast clear input accepting NIM-level signals (≥ 50 nsec in width) forces all 12 channels to cease their conversions, be cleared and ready to accept another gate pulse after 1.5 to 2.0 μsec (see Technical Date sheets at the beginning of this manual). An internal monstable makes this

wait period mandatory. The fast clear feature allows ADC conversion to begin on a fast trigger and be completed only if the event satisfies a complete trigger requirement.

2.6 Test Feature

A built-in test feature checks all channels simultaneously with an F(25) command. If the CAMAC Inhibit (I) is present and a positive DC level is applied either to a front panel "Test" input (with internal high $Z \geq 10$ KΩ connection to +12 volts) or optionally to rear connector patch points P1, P2, or P5, then F(25)·S2 will inject charge with a proportionality constant of approximately -12.5 pC/volt into all inputs (20 pC for the W version). A 20 Volt test input will correspond to nearly full scale output. The internal gate generated by F(25)·S2 is approximately 80 nsec. If the user desires a measure of residual pedestal only, the CAMAC "I" should be removed; F(25)·S2 will then generate the 80 nsec gate only with no charge being injected into the analog inputs. This test feature permits the pedestal itself to be periodically checked for drifts. If two measurements are made, one with charge input and one without (i.e., with and without "I"), the total conversion characteristics could be checked. In this case, the "no charge" result gives the intercept and the "with charge" counts minus the "without charge" counts divided by the charge applied, gives the slope of the conversion plot. See Figure 2.1.

The test feature may be connected to the rear of the 2249 as mentioned previously. The rear of the 2249 printed circuit board contains 3 drilled holes labeled P1, P2, and P5. Soldering a feedthrough at any one of these holes electrically connects the front panel "Test" input to the CAMAC connector pins P1, P2, or P5. In this way, many units can be grouped for simultaneous calibration.

It should be noted that the standard 2249SG does not respond to F(25) and has no "Test" feature. It is possible, however, to do on-line testing of the 2249SG if necessary. The price of this feature is the elimination of the inhibit feature. With the standard 2249A, the CAMAC "Inhibit" enabled the test circuit while disabling the gate circuit. Since the 2249SG has no internally generated "Test" function, the "Start" circuit must be used. To permanently enable this "Start" circuit to permit a test function to be performed, Q7, or the inhibit transistor, must be removed.

With Q7 removed, the leading edge of a pulse applied to the "Start" input will cause a fixed charge to be injected into the 2249SG analog inputs. Coincident with the "Start", the 12 gate pulses must be applied, which should have a duration between 80 nsec and 100 nsec. An exact 80 nsec gate will yield a proportionality constant of -12.5 pC/volt of DC signal applied to whichever rear patch point (P1, P2, or P5) you choose to use for the test input. For shorter gate widths, a smaller net amount of charge is injected into each input, i.e., on the order of 90% ± 1% for a 40 nsec gate.

If a test function is to be used, care must be taken to be sure the "gates" precede the "Start" by 10 nsec.

CAUTION: Since the "Test" is not a designated feature of the 2249SG, its utilization is not factory tested.

2.7 Linearity

The integral linearity of the 2249 Series is typically < ± 2 counts (see specifications in Technical Data Sheet, Section 1). This is defined by LeCroy as the maximum deviation from the best straight line fit to measured points. Every ADC is computer tested before being shipped to make certain it meets linearity and functional operation specifications. Each channel is tested for linearity at 21 points across its range by a 16 bit digital to charge converter.

2.8 Pedestal

The residual pedestal is the number of counts obtained when a gate pulse is applied with a no analog input (i.e., input merely terminated in 50 Ω). Pedestal is a result of several factors, the largest of which is the charge injection (also contributing to the A and SG versions is a factory-set positive DC offset) the purpose of which is to assure proper operation of the front end in case the quiescent DC level of the input should drift. It is this DC offset contribution which largely comprises the gate-dependent portion of the residual pedestal specification. The fixed amount of pedestal indicated on the technical data sheet results largely from the charge injection.

Due to DC coupling of the A and SG inputs, the gate-dependent portion of the pedestal has a temperature coefficient associated with it. This effect is magnified by a factor of 2 if the input is DC shorted to ground as it would be when driven from a pulse transformer, for example, used to cater photomultiplier dynode signals to the negative input requirements of the 2249A. For short gate widths, the resultant potential temperature drift is small. However, it is nevertheless recommended that AC-coupling be used wherever rate conditions can permit it. This will nearly eliminate all but the fixed pedestal and its associated temperature coefficient.

The pedestal of the 2249A is factory adjusted to approximately 8 counts for a gate duration of 50 nsec and to 50 counts for the SG version. The pedestal of the 2249W is factory adjusted to approximately 16 counts for a gate duration of 400 nsec. The adjustment is made with 50 Ω termination of each analog input. The pedestal of each channel of the 2249A is separately screwdriver adjustable through the side panel. Each adjustment screw is accessed through a hole adjacent to the input for the channel. (NOTE: When making adjustments, use a non-conducting screwdriver.)

2.9 Conversion Time

Since the full scales of the 12 channels of each 2249 may differ from each other by up to ± 5%, the time for each channel to achieve a full scale conversion may also differ from that of the other channels. Total conversion time is roughly 50 μsec for the A and SG versions and 100 μsec for the W version. Manufacturing variances in clock frequency, ramp currents, and the necessity to allow for overflow as well as a wait interval incorporated in the design, require that a 20% margin in conversion time be allowed for. As a result, the 2249A clock is internally held on for a maximum time of 60 μsec, the SG for 55 μsec, and the W for 100 μsec (for

any size conversion). Due to the fast clear feature of the 2249, however, this conversion time need be awaited only for valid events.

IMPORTANT: Care should be taken when using the 2249SG to ensure that all gates come within 2 μsec of the "Start" pulse. If this will not be true, the duration of the active clock may be increased by changing the 20K Ω resistor on IC "TD" (9602) to a larger value. Then the maximum allowable time between any two gates should be the new value of the monostable delay minus approximately 53.5 μsec.

2.10 Q and LAM Suppression

The 2249 Series was designed to permit one to eliminate the readout of empty modules if maximum readout rate is desired. An adjustable potentiometer (accessed from the side of the module) permits the user to define an "empty" module by setting a count level from 0 to 100 that must be exceeded before data is considered useful. A module in which all channels contain less than the set amount will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. An X, Command Accepted, response is still generated.

Some branch drivers (interfaces between computer and CAMAC crate) require a Q response or a LAM from any module that occupies a station (N) in the CAMAC crate. For these situations, the L suppress feature may be defeated by removing the jumper XZ and replacing it with jumper YZ. (See schematic sheet 3 and Figure 2.2). In this situation the LAM is not suppressed and a LAM is obtained after any Read command. The Q-response suppress can be defeated by removing jumper VW and replacing it with jumper UW. To defeat both Q and L Suppress, it is only necessary to set the count level to 0. (NOTE: 2249's and older 2249A's do not have all the jumper options available on the P.C. board. These units will require the bus be cut and a jumper added on the solder side of the board).

2.11 Data and Readout

The output data of the 2249 Series is standard CAMAC compatible (TTL negative logic) in binary format. The 2249A and SG have 10 data bits plus an overflow bit. The 2249W has 11 databits and indicates an input greater than or equal to Full Scale by giving Full Scale (1980 counts) output. The digitized information plus overflow bit are gated onto the Dataway bus lines by F(0)•N•A, where F(0) signifies the read function, N signifies the 2249 to be read and A (from A(0) to A(11)) signifies which ADC channel in the 2249 is to be read out. Generally the unit is ready for readout when LAM appears. The function F(2) (Read and Clear) may also be used to read information from chosen ADC channels. However, this readout is destructive only when A(11) is addressed, the F(2)•N•A(11) clearing all channels at one time. The F2 command on addresses A(0) through A(10) will cause the ADC contents to be read with no clear and the input gate will remain disabled.

2.12 LAM

A LAM (Look-At-Me) signal is generated from end of conversion until a module Clear or Clear LAM (Z, C, F(2), F(9) or F(10)). LAM is disabled for

the duration of N, can be permanently enabled or disabled by the Enable F(26) or Disable F(24) function command, and can be tested by Test LAM F(8). LAM may be suppressed for empty modules as indicated in "Q and LAM Suppression" section above.

The test function F(8) allows the LAM to be tested. In response to application of F(8)·N·A (where A is from A(0) to A(11)) independent of Disable LAM, a Q response will be generated if LAM is set. Although the LAM is disabled while the 2249 in question is being addressed (i.e., for the duration of N), once latched it will produce a Q response when an F(8)·N·A is applied.

IMPORTANT: When current is applied to the 2249 (such as would occur when plugging a module in and turning the crate power supplies on), the states of the LAM latch and LAM enable are arbitrary. The unit must always be initialized with an F(24) (Disable LAM) or an F(26) (Enable LAM), and an F(10) (Clear LAM).

2.13 Packaging and Current Requirements

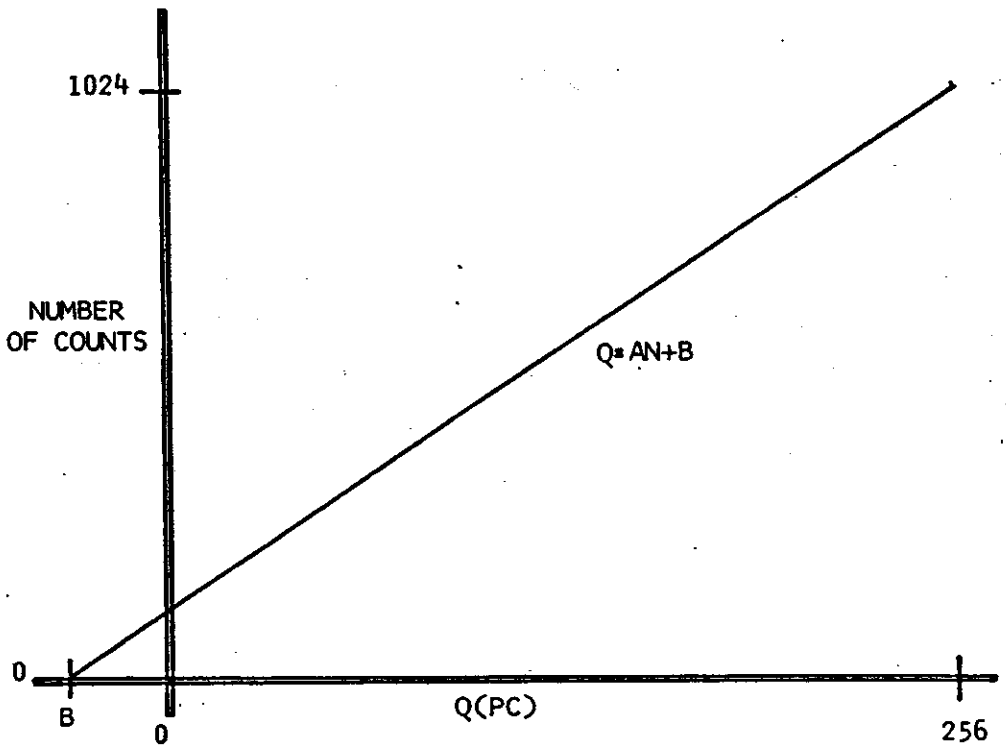
The 2249A and 2249W are packaged in a standard #1 width CAMAC module (conforming to ESONE Committee Report EUR4100). The 2249SG is #2 width. The A and SG versions dissipate a total of 7.5 watts and the W, 10.6 watts.

CAUTION: Because of the adjacency of the various voltage bus connector contacts in the CAMAC crate, plugging in any CAMAC unit may cause a momentary short of the power pins. This can cause severe damage to the module inserted, especially since the 24 volt pins are adjacent to the 6 volt pins. THUS, THE CRATE POWER SHOULD BE OFF WHEN A MODULE IS INSERTED OR REMOVED.

2.14 Inhibit Circuit

The standard 2249A and W have an automatic inhibit that prevents subsequent gate pulses from allowing more charge to enter the QTC after a first gate pulse is applied. This "self inhibiting" feature is not offered on the 2249SG. Therefore, caution must be taken to permit only one gate pulse per channel per event.

The Inhibit line of the 2249SG only affects the "Start" input, not the individual gates. Thus, gate pulses received during an inhibit period will cause charging of the integrating capacitor of the QT100C but no counts will be observed at the digital output. The gate pulse source should be externally inhibited whenever a CAMAC inhibit is applied. This function is easily performed if LeCroy Model 821 Quad Discriminator with Veto is chosen to drive the ADC gates.



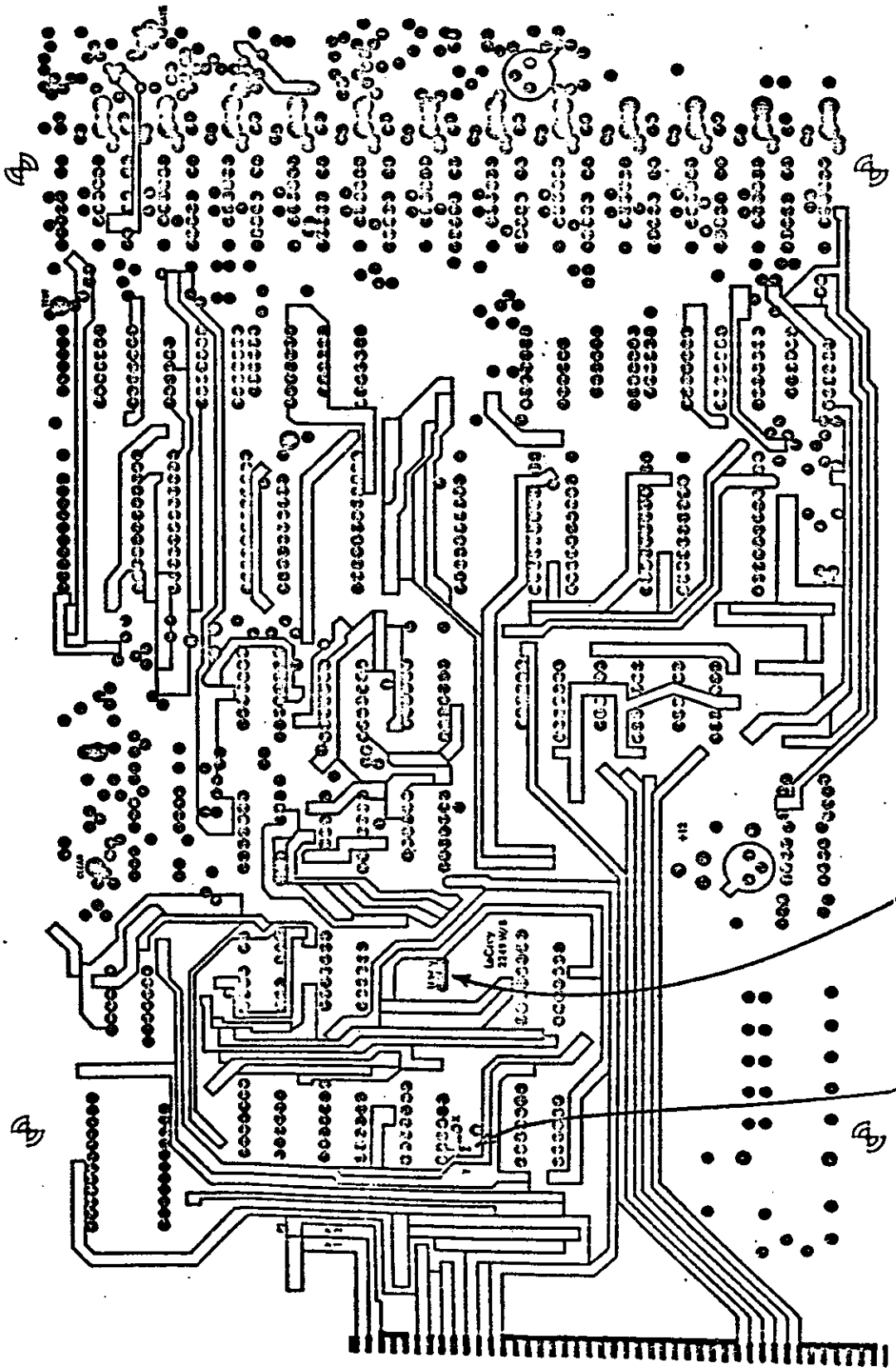
B IS AMOUNT OF PEDESTAL

Q IS CHARGE APPLIED TO ADC ANALOG INPUTS

N IS TOTAL NUMBER OF COUNTS

A IS CONVERSION SLOPE
I.E. A=(Q+B)/N

FIGURE 2.1



JUMPER LOCATION SIMILAR ON ALL 2249 SERIES UNITS

FIGURE 2.2

SECTION 3

TECHNICAL DESCRIPTION

3.1 General

The Model 2249 consists of 12 independent identical ADC's and associated circuitry. Referring to the 2249 Block Diagram in Figure 3.1, the 2249 circuitry is divided into 6 basic parts:

* Twelve QTC (charge-to-time converter) channels
* A gate, test, and pedestal circuit for distributing the gate signal to the separate linear gates of the QTC's
* Twelve clock synchronizers and scalers
* A controlled oscillator
* A Q response and L suppress circuit
* A CAMAC control section

Separate descriptions of each of these circuit blocks follow.

3.2 Charge-To-Time Converter

Each of the 12 inputs employs a hybrid change-to-time converter (QTC). A block diagram and waveforms for the QT100C are shown in Figure 3.2. The QTC consists of a virtual ground input amplifier, a linear gate driving a stable integrating capacitor, a current source, and an output differential amplifier.

The analog input of the 2249A and SG is a virtual ground with approximately 5 to 6 Ω impedance. It can be driven either from the front panel analog input via a 44 Ω resistor or from the common test input bus (which supplies each channel with an amount of charge proportional to the test input level supplied at the front panel or rear patch pin. (Without any TEST input, a high impedance connection to +12 volts generates an approximate 60% of full scale reading).

The QT100C and QT100B are identical and interchangeable. The letter change indicates only a change in method of manufacturing. These are used in the 2249A and SG. The QT102 is used in the 2249W and may not be interchanged with the QT100 series.

The front panel input has 44 Ω of resistance divided into two parts with input clamp diodes at their junctions to provide input protection and reduce crosstalk on large overloads. These resistors, in series with the low input resistance of the linear gate, terminate the input cable to 50 Ω. The stored charge is therefore $Q = \int_{T_g} (V_{in}/50\ \Omega)\, dt$ where V_{in} is the time dependent voltage on the analog input and T_g is the duration of the gate pulse. For the 2249A and 2249SG the current handling capability of the

input limits the linear range of the analog signal to -20 mA (or -1.0 volt across the 50 Ω input). On the 2249W the limit is -2.0 volts.

For the 2249A and 2249SG the required gate input signal is a standard NIM logic level, with recomended duration of 10 nsec minimum to 200 nsec maximum. The analog input is enabled for the duration of the gate.

The QT102 used in the 2249W employs a similar circuit, also with a 50 Ω input impedance. The input is, however, AC coupled via a 6.8 μF capacitor on the circuit board and minimum gate width is 30 nsec.

The charge delivered to the integrating capacitor through the linear gate is subsequently removed by means of a stable current source (see Figure 3.2). Thus, the voltage across the integrating capacitor is returned to its quiescent level at a constant rate. This rate is proportional to the difference between the +24 and V_{REF} inputs (Gain Adjust and +12 respectively, on block diagram). The output amplifier senses the voltage across this capacitor and generates an output level as long as this voltage is greater than a reference level (which is set by the 30 mV bias voltage). The output time duration (T) is therefore proportional to the input charge Q, where time T in microseconds is approximately 0.4 times the charge Q in picocoulombs (i.e., T = 0.4 Q μsec/pC). Operation of the QTC is assured by on-board stabilized ± 5 V supplies, keeping a perfect balance in the QTC. The V_{REF} (approximately +12 VDC) tracks the +24 VDC supply, causing the difference (used as the current source reference) to be independent of external supply variations. A small fixed amount of charge is always put into the analog input when a gate pulse is generated. The pedestal of each ADC channel has been factory calibrated to be equivalent to a few picocoulombs input (for gate pulse widths of 50 nsec) when all the inputs are externally loaded with 50 Ω terminations. If the inputs are not terminated, a slightly lower reading will be observed.

A Clear command can be used if desired to clear the 2249 during a conversion cycle. It not only initializes all the digital control and scaler stages, but also, via a leading edge R-C differentiator, clears the analog ramp of the QTC to its quiescent level. The analog clear pulse width is about 300 nsec, leaving the remainder of the digital clear time for settling in the QTC.

3.3 Gate, Test and Pedestal Circuit

The gate generator is operated by either a front panel NIM input signal or by an increment signal supplied by the CAMAC controller. The internal gate pulse will actually enable the analog inputs of the A and SG versions about 4 nsec after application and the W version, 7 nsec after. It should, therefore, precede any input by at least that amount. The actual duration will be equal to the input plus about 4 nsec for the A and SG versions, 5 nsec for the W. The increment pulse supplied by the CAMAC control section generates an approximately 80 nsec wide gate pulse (see schematic, sheet 3, and Figure 3.3 upon application of an F(25). Its action is to enable the gate and generate a test pulse.

The test input of the 2249A and W is connected through a precision resistor to a common capacitor in the test circuit. The charge which is stored in

this capacitor is equally shared by all channels. The CAMAC Inhibit must be used when testing the unit with F(25). On an INRC command, $\overline{F(25)} \cdot S2$, the CAMAC control generates a pulse which is OR'd into the gate circuit. In addition, if an inhibit condition exists, INCR discharges the test capacitor equally into the 12 QTC's during the gating interval. The test input accepts a positive DC level of 0 to 20 volts to produce a zero to approximately full scale digital output of each ADC.

The trailing edge of the output of the gate generator also produces an initiate pulse which is used to set the busy latch and generates the delayed pulse which starts the conversion cycle. The busy latch feeds back to inhibit the gate within 100 nsec of the trailing edge and is cleared by the reset pulse.

The pedestal is adjusted by injecting charge via a trimmer capacitor (C_{PED}) into the virtual ground of the QTC from the leading edge of the gate pulse where the amount of charge is proportional to the C_{PED} in pFd times the voltage swing of the gate pulse. The trailing edge of the gate is not coupled in because the gate closes and blocks the charge. Because of the charge injection time constant, gate widths narrower than 50 nsec (500 nsec) will not allow all of the injected pedestal charge to be accumulated by the 2249A (2249W). This causes a reduction of the pedestal reading somewhat faster than indicated by the gate dependent term in the specifications.

3.4 Clock Synchronizer and Scaler

The output of each QTC hybrid in the 2249 Series is used to gate an oscillator into one half of a LeCroy hybrid SC100 Dual Eleven-Bit Scaler. The oscillator is synchronously started with respect to the leading edge of the gate (see section 3.5). This ensures no fractional pulses during the beginning of the rundown cycle, but care must be taken at the end of the rundown. This is done by the synchronizing stage. Each gate circuit (see schematic sheet 2, and Figure 3.4) supplies an integral number of clock pulses even if the QTC output returns to its quiescent state in the middle of a clock pulse as shown in the figure.

When the conversion cycle is complete, readout of the addressed scaler can be done by enabling the proper SC100 (using decoded A2, A4, and A8 subaddress lines) and selecting the proper half of the SC100 (using the A1 subaddress). The data will be gated out in parallel to the CAMAC dataway.

3.5 Controlled Oscillator

The clock circuit is a modified Colpitts oscillator employing a highly temperature stable choke and a mica capacitor as its resonant elements. Its frequency is 20 MHz. The oscillator is gated on 2.2 μsec after the leading edge of the gate pulse. Gating the oscillator in this way eliminates the uncertainty of one count associated with an asynchronous oscillator and eliminates noise and nonlinearities caused by not delaying the turn-on (see Figure 3.5). The conversion time is set to 60 or 105 μsec allowing more than enough time for the nominal 50 μsec or 100 μsec full scale conversion to occur for the 2249A and SG or W, respectively. This allows for the ±5% differences from channel to channel, slight temperature drifts, module to module variations, etc., and still ensuring that an overflow can occur for

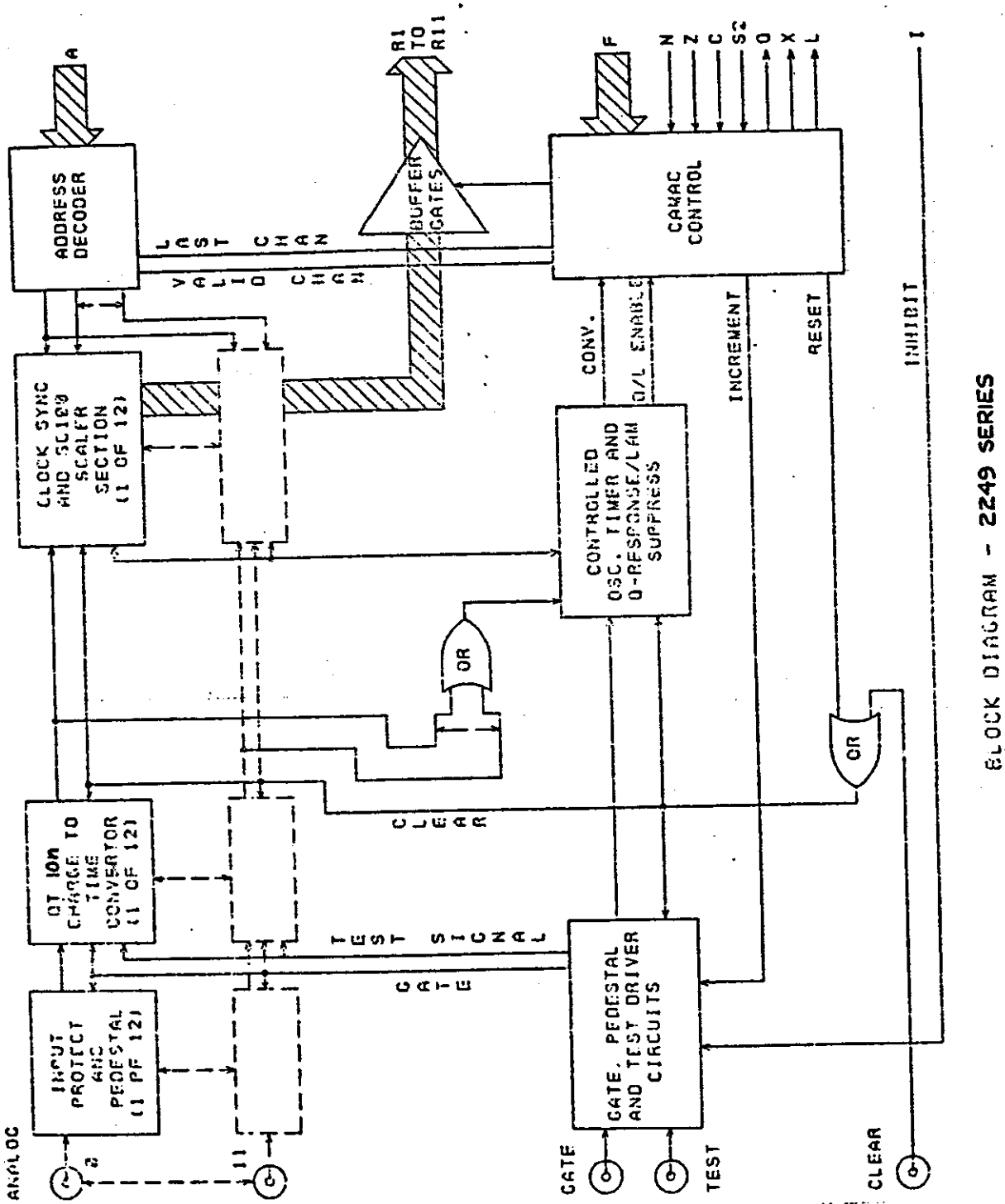
oversized input pulses.

3.6 LAM and Q-Response Suppress Circuit

At the beginning of the gate pulse, a monostable is set (see Figure 3.5). The RC time constant of this monostable is adjustable by a side panel potentiometer labeled Q and L SUPPRESS LEVEL ADJUST. When the monostable resets, a latch is reset if one or more of the QTC outputs is still on. If set, this latch disables the Q-response circuit (that normally indicates valid data on an F(0) or F(2) Read Command) and clears the LAM. Disabling of the suppress function can be done for either Q-response or L. See Operating section 2.10 for more information.

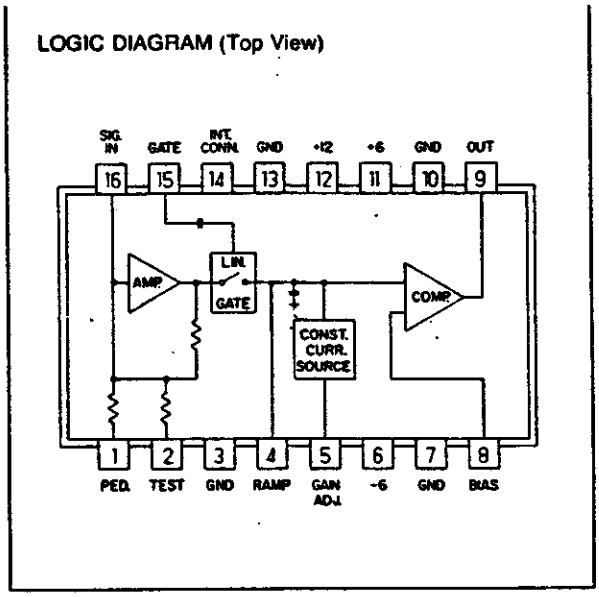
3.7 The CAMAC Control

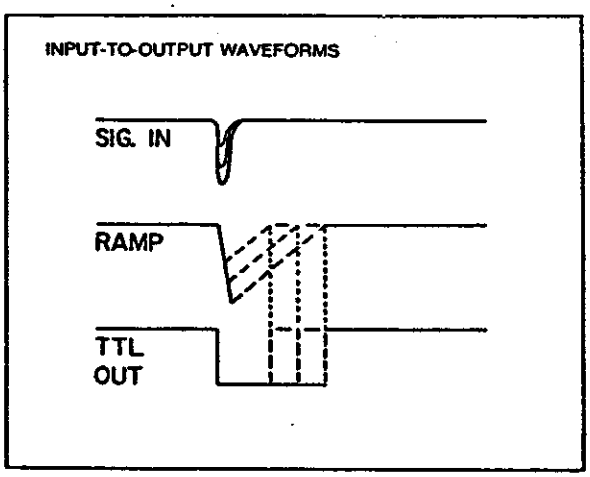
The decoding of CAMAC "F" functions and N is performed by a 4 line to 16 line decoder (an SN74154). A DC level is generated at the appropriate pin for each valid CAMAC command. Scaler addressing is accomplished using a 4 line to 10 line decoder (an SN7442) on A2, A4, and A8, to enable the appropriate SC100 scaler hybrid and the A1 bit is used to select the appropriate half of the SC100. X-response is generated for all valid commands, and Q-response and LAM are generated as described in the Q and L Suppress Circuit section.



BLOCK DIAGRAM - **2249 SERIES**

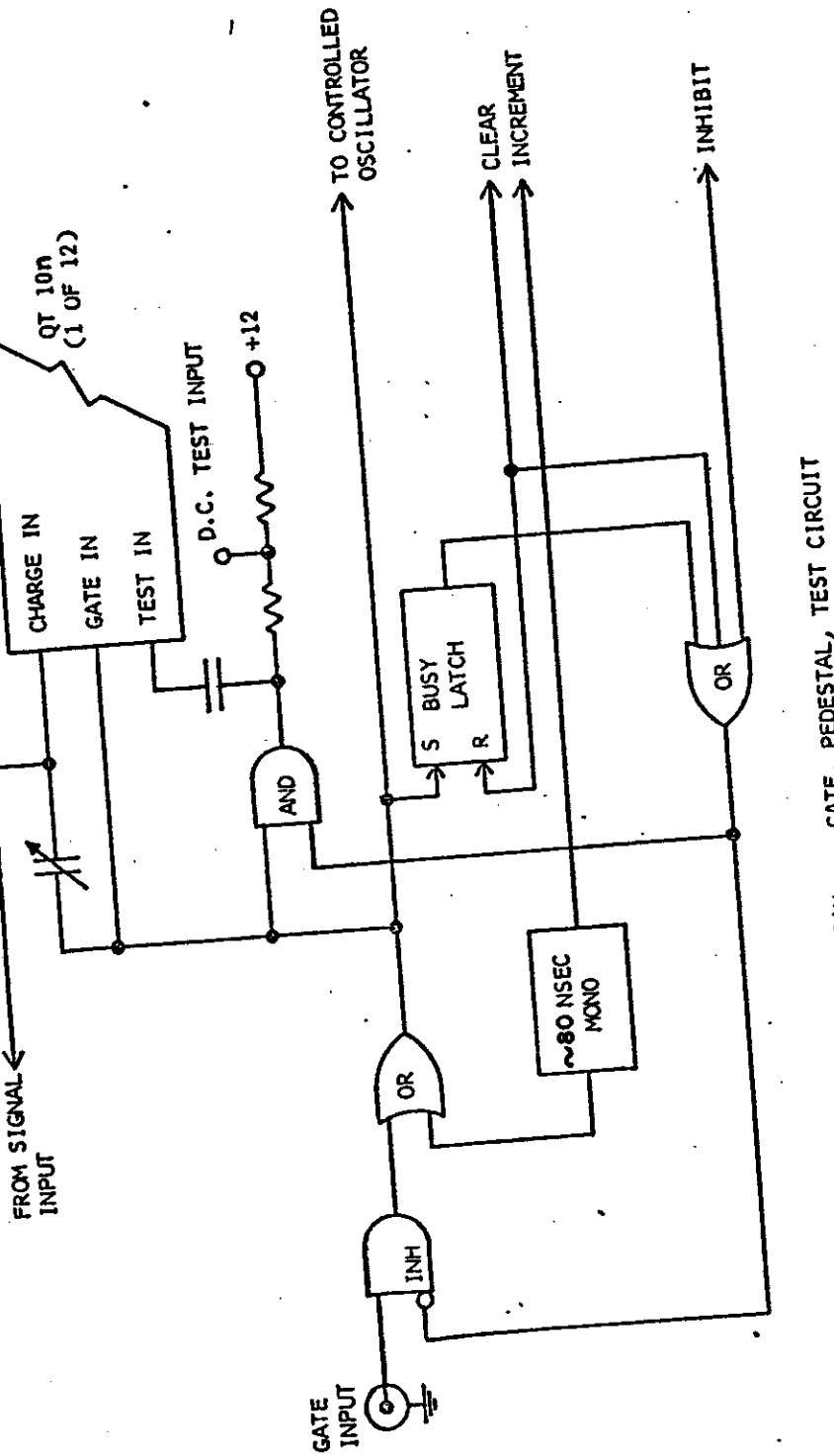
FIGURE 3.1





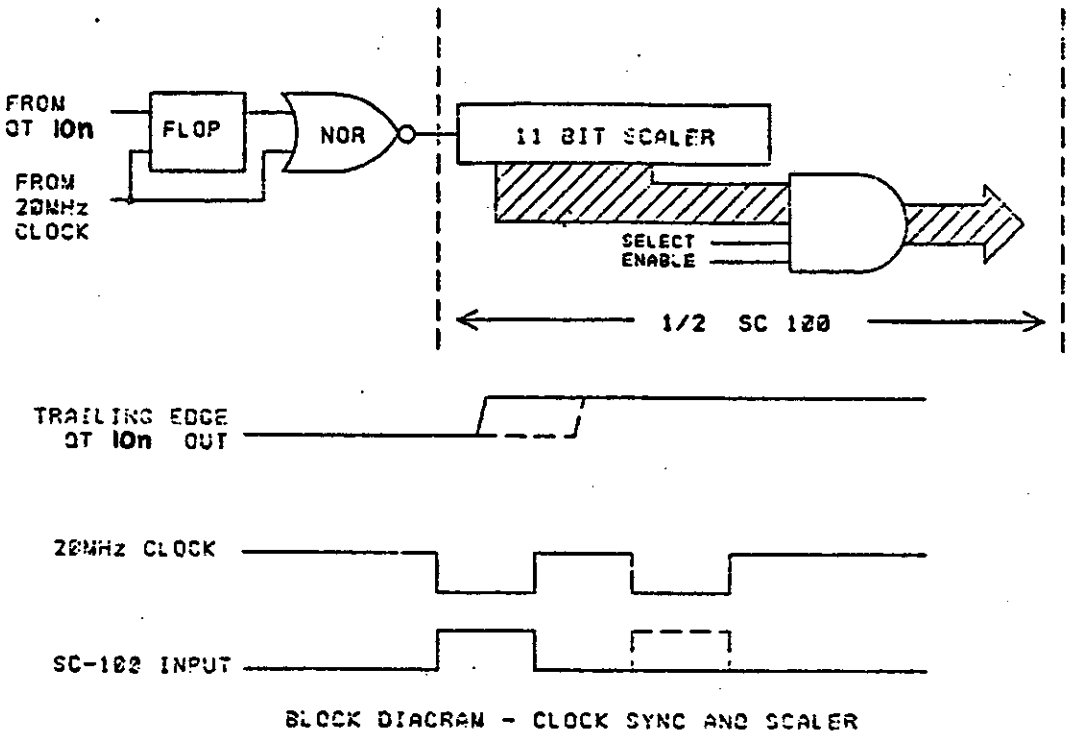
QT100C

FIGURE 3.2



BLOCK DIAGRAM - GATE, PEDESTAL, TEST CIRCUIT

FIGURE 3.3



BLOCK DIAGRAM - CLOCK SYNC AND SCALER

FIGURE 3.4

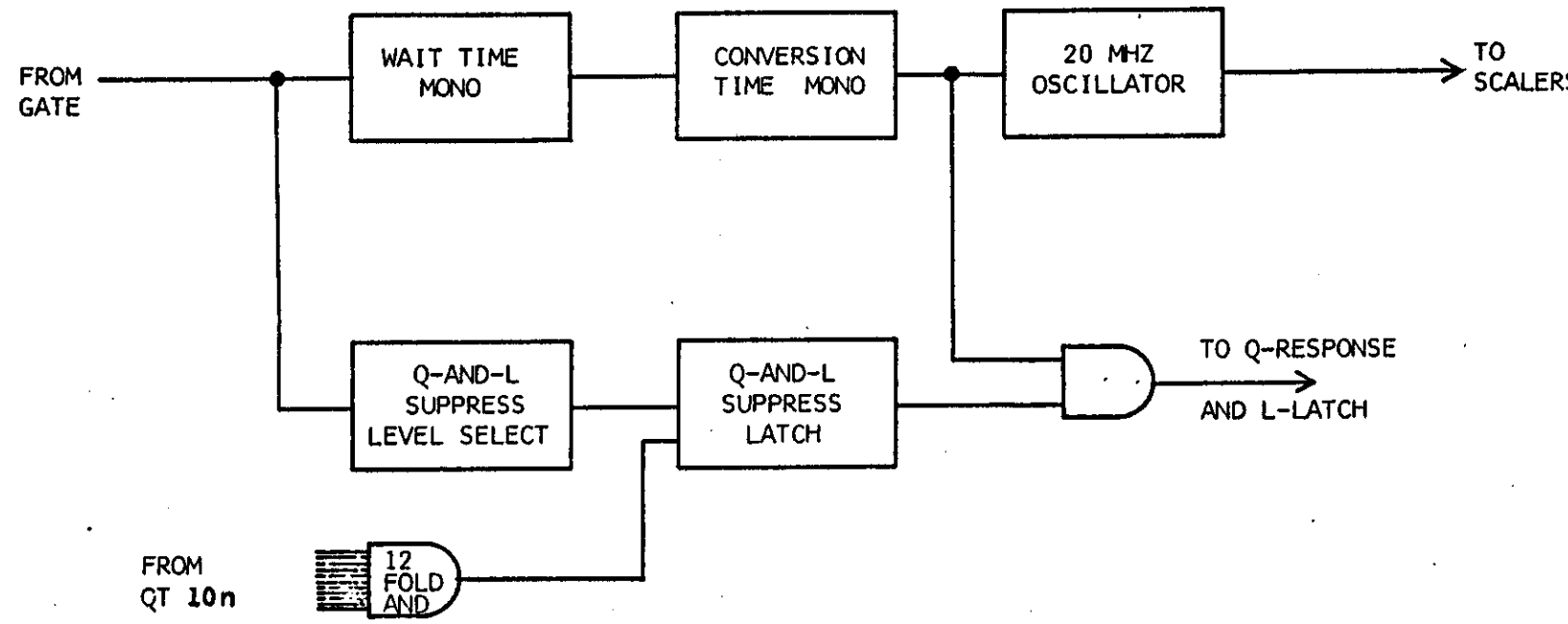


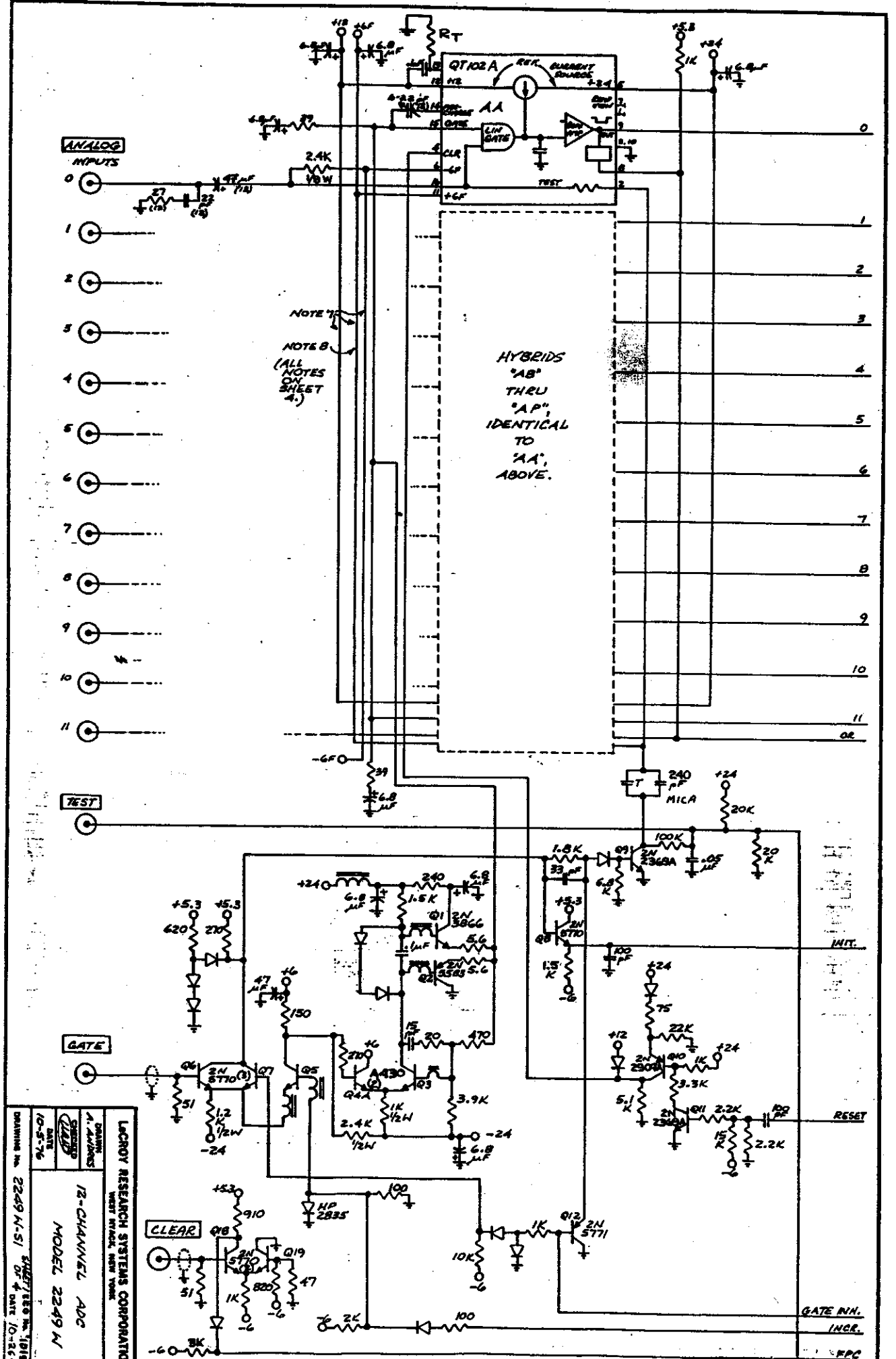
FIGURE 3.5

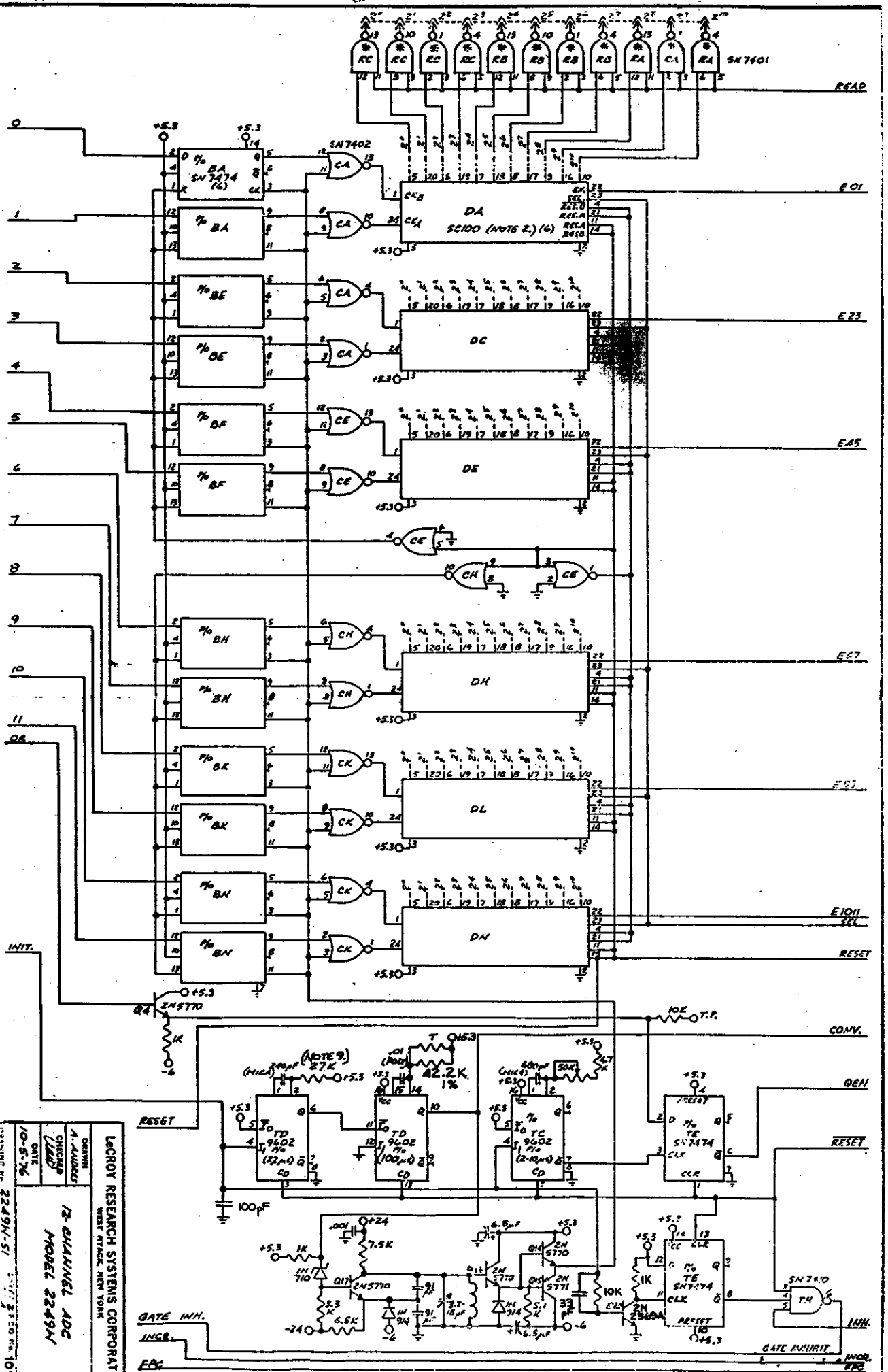
BLOCK DIAGRAM - CONTROLLED OSCILLATOR AND Q-RESPONSE AND L SUPPRESS

REPLACEMENT PARTS

MODEL NO 2249W — 12-CHANNEL ADC — PRINTED 14-Feb-86
ECON 1015 — REV DATE 26-Oct-83
MCN 2 — MCN DATE 07-Nov-83

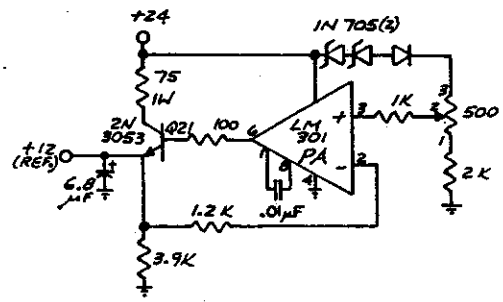
LeCROY PART NO	DESCRIPTION	
102 145 104	CAP CERA DISC 12V .1 U PT-FDCL-1/32 LEADS 3/8 AWG 22	*
102 245 103	CAP CERA DISC 25V .01 U PT-FDCL-1/32 LEADS 3/8 AWG 22	
102 245 503	CAP CERA DISC 25V .05 U PT-FDCL-1/32 LEADS 3/8 AWG 22	*
102 444 101	CAP CERA DISC 100V 100 P 10% S3N	
102 444 220	CAP CERA DISC 100V 22 P 10% S2L	
102 444 330	CAP CERA DISC 100V 33 P 10% S2L	
102 745 102	CAP CERA DISC 500 .001 U PT-FDCL-1/32 LEADS 3/8 AWG 22	*
102 944 150	CAP CERA DISC 1KV 15 P 10% S2L	
103 437 104	CAP CERA MONO 100V .1 U 20% GEN PURP/LEADS FULL LENGTH	
116 000 910	CAP DIP MICA SPECL 91 P 5% TC: 0 TO +70 PPM/C	
116 515 151	CAP DIP MICA DM10 150 P	
116 515 241	CAP DIP MICA DM10 240 P	
116 525 681	CAP DIP MICA DM15 680 P	
125 535 103	CAP POLYCARB FILM .01 U 50V 5%	
141 494 225	CAP TANT (MINI) 2.2 U AXIAL LEADS/ .075 X .250	
142 124 476	CAP TANT DIP CASE 47 U 6.3V 20% .335 X .394	*
142 824 685	CAP TANT DIP CASE 6.8 U 35V 20% .256 X .374	*
147 147 090	CAP ALUM METAL CAN 90 U 6V -10 +75% .328 X .578	*
158 639 001	CAP VARI CERA 5.0 - 25 P PURPLE MARK .240 HI .220 DIA	
158 819 001	CAP VARI CERA 3.5 - 18 P BLUE MARK .240 HI .220 DIA	
161 030 000	RES COMP ZERO OHM	
161 225 242	RES CARBON FILM 2.4 1/8W 5%	
161 335 047	RES CARBON FILM 4.7 OHM 1/4W 5%	
161 335 056	RES CARBON FILM 5.6 OHM 1/4W 5%	
161 335 101	RES CARBON FILM 100 OHM 1/4W 5%	
161 335 102	RES CARBON FILM 1 1/4W 5%	
161 335 103	RES CARBON FILM 10 1/4W 5%	
161 335 104	RES CARBON FILM 100 1/4W 5%	
161 335 121	RES CARBON FILM 120 OHM 1/4W 5%	
161 335 122	RES CARBON FILM 1.2 1/4W 5%	
161 335 151	RES CARBON FILM 150 OHM 1/4W 5%	
161 335 152	RES CARBON FILM 1.5 1/4W 5%	
161 335 153	RES CARBON FILM 15 1/4W 5%	
161 335 182	RES COMP 1/4W 5% 1.8 1/4W 5%	
161 335 200	RES CARBON FILM 20 OHM 1/4W 5%	

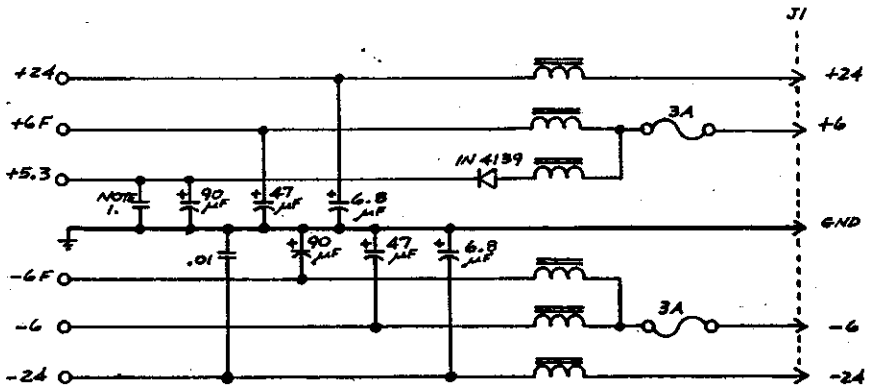

ANALOG INPUTS
0
1
2
3
4
5
6
7
8
9
10
11
TEST
GATE
CLEAR
NOTE 7
NOTE 8
(ALL NOTES ON SHEET 4.)
HYBRIDS "AB" THRU "AP", IDENTICAL TO "AA", ABOVE.
QT102A
RST.
CURRENT SOURCE
LIN GATE
CLR
TEST
2.4K
1/2W
-6F
39
6.8 µF
T
240 pF MICA
+24
20K
100K
1.8K
33 pF
Q9
2N 2368A
.05 µF
20 K
6.8 K
+5.3
Q8
2N 5710
1.5 K
100 pF
INIT.
+5.3
620
270
+24
240
1.5K
Q1
2N 3866
5.6
Q2
2N 3563 S.C.
47 µF
+6
150
15 pF
20
470
Q6
2N 5710 (3)
Q7
Q5
Q4
A430 (2)
Q3
Q4A
210
51
1.2 K 1/2W
-24
1K 1/2W
2.4K 1/2W
3.9K
6.8 µF
+24
75
22K
+12
Q10
2N 2907A
1K
3.3K
5.1 K
Q11
2N 2369A
2.2K
100 pF
15 K
2.2K
RESET
+5.3
910
HP 2835
100
Q18
2N 5770
Q19
1K
820
47
-6
3K
10K
Q12
2N 5771
2K
GATE INH.
INCR.
RDC
LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK
DRAWN A. RAVIKIRES
CHECKED CLARK
DATE 10-5-76
12-CHANNEL ADC
MODEL 2249 W
DRAWING No. 2249 W-SI
SHEET 3 OF 4
DATE 10-26-76


SN7401
READ
SN7402
DA
SC100 (NOTE 2.)(6)
DC
DE
DH
DL
DN
E01
E23
E45
E67
E1011
RESET
INIT.
Q4
2N5770
CONV.
GEN
RESET
42.2K 1%
27K
100pF
7.5K
GATE INH.
INCR.
EOC
12-CHANNEL ADC
MODEL 2249W
LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK
DRAWN
A. AMOROSO
CHECKED
DATE
10-5-76
DRAWING No. 2249W-51

VOLTAGE PWS:

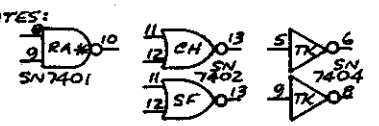
I.C.	REFERENCE	+24V	+12V	+6V	+5.3V	-6V	GND	-24V
LM 301	PA	7					4	
Q1102	ZA, AB, AC, AD, AE, AF, AH, AJ, AK, AL, AM, AN, AP	6	12	11		9	8, 10	
3C100	DA, DF, DE, DB, DL, DJ				1		3	
SN 7400	SD, SE				14		7	
7401	RA, RB, RC, SH				14		7	
7402	CA, CE, CH, CK, SF, YF				14		7	
7404	SL, YK				14		7	
7410	SM				14		7	
7420	SA				14		7	
7430	SK				14		7	
7473	SC				4		11	
7474	RA, RE, RF, RH, RK, RM, YK				14		7	
74LS164	SB				24		12	
9602	YC, YD				16		8	





NOTES:

1). ADDITIONAL CAPACITORS ON VOLTAGE BUSES, NOT SHOWN
2). ALL SC100-S ARE WIRE ORED.
3). "T" DESIGNATES VALUE TO BE CHOSEN AT TEST.
4). * DENOTES OPEN COLLECTOR.
5). UNUSED GATES:



6). ALL UNIDENTIFIED DIODES ARE IN4448 OR IN914.
7). NOT SHOWN: 2.2 µF CAPACITORS ON +6V, -6V AND +12 BUSES TO GROUND.
8). 6.8 µF CAPACITORS ON +6V BUS, NOT SHOWN.
9). THIS RESISTOR VALUE MAY VARY, IF HYBRIDS OTHER THAN QT 1024-3 ARE USED.

LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK

DRAWN A. ANDRES
SUPERSEDES
DATE 10-5-76

12-CHANNEL ADC
MODEL 2249W

DRAWING No. 2249W-51 SHEET 6 OF 7 DATE