

2731

PCOS III

DELAY AND LATCH MANUAL

July 1982

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A T T E N T I O N

THE CRATE CONTAINING THIS MODULE SHOULD ONLY BE TURNED ON WHEN A PCOS III SYSTEM CONTROLLER IS IN THE CONTROLLER POSITION OF THE CRATE.

SEE SECTION 2: INSTRUCTIONS FOR INITIAL USE OF THE 2731.

CRATE POWER SHOULD BE TURNED OFF DURING INSERTION AND REMOVAL OF UNIT TO AVOID POSSIBLE DAMAGE CAUSED BY MOMENTARY MISALIGNMENT OF CONTACTS.

THE LEFTMOST MODULE WITHIN THE CRATE MUST CONTAIN A TERMINATOR. ALL OTHER 2731 MODULES MUST NOT. SEE SECTION 2.1.

SEE POCKET IN BACK OF MANUAL FOR SCHEMATICS, PARTS LISTS AND ADDITIONAL ADDENDA WITH ANY CHANGES TO MANUAL.

A T T E N T I O N

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LeCroy

PCOS III

Dedicated CAMAC Model 2731 32-Channel Delay and Latch

- Programmable *Ripplethru* Delay: 300–682.5 nsec
- Edge Triggered Latch: For Minimum Coincidence Resolving Time
- Prompt OR Outputs: User configured
- Latched OR outputs: User configured
- Programmable: Threshold For Chamber Cards
- Programmable Test Registers: For Hardware Processor Tests

The LeCroy Model 2731 has been designed as a central element for MWPC encoding. Each 2731 module accepts 32 differential ECL inputs on two LeCroy ECLine standard 17 pair front panel headers. Using LeCroy's unique *RIPPLETHRU* delay, each Wire-In input is delayed by a programmable amount in the range of 300–682.5 nsec. The delayed data is presented to a Latch which can be activated by coincidence gates as short as 30 nsec.

Computer control of the threshold of chamber discriminators is provided in the Model 2731 via an eight-bit digital-to-analog converter. This threshold programming voltage is provided at both Wire-In input headers. The LeCroy Models 2735 and 7791 chamber cards use this voltage for setting the chamber threshold.

The Model 2731 has provisions for inclusion of the wire chamber data in the first and second level triggers. Prompt ungated logic signals, taken before the *RIPPLETHRU* delay, are presented as two-fold ORs on the 2731 card. Also, latched logic levels are presented as four-fold ORs on the card. The Prompt and Latched ORs may be arbitrary user ORed with up to 16 logic signals assigned to the front panel differential ECL line driver outputs. Wire wrap posts are provided for this purpose. These provisions allow the Model 2731 to be custom-tailored to the experimental trigger.

LeCroy's *RIPPLETHRU* circuit provides delay without adding deadtime. It offers 300 nsec to 682.5 nsec of delay with a double pulse resolution of <100 nsec. This unique delay scheme offers excellent stability and interchannel matching (± 10 nsec) while providing CAMAC programmability or "electronic cable cutting." The Coincidence Gate, Test Input Signal, and Fast Clear inputs are applied to the 2731 module via the CAMAC Dataway, eliminating the need for costly fanout. The signals are applied to the Model 2738 PCOS III controller which drives the Dataway.

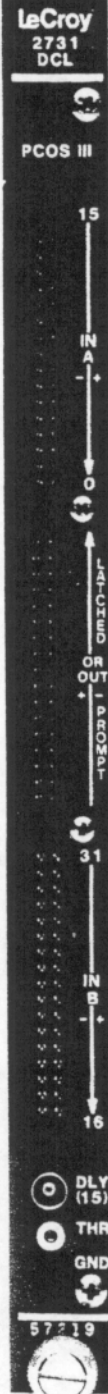
The Coincidence Gate defines the time interval for which the wire latches are active. Wire discriminator signals which are received and passed through the *RIPPLETHRU* delay are latched within the Model 2731 by a Coincidence Gate.

Comprehensive test facility has been built into the PCOS III System. In addition to test inputs on the chamber card, the 2731 can be separately tested. Two 16-bit registers on the 2731 card allow selected inputs to be enabled. The application of a 2738 TEST pulse applies an input to all enabled channels. In this way, the 2731 circuitry and the track recognition circuitry can both be tested.

The Model 2731 is to be used in a dedicated CAMAC crate using the Model 2738 in the controller station. In this configuration, the 2731 modules can be read out at 10 times CAMAC speed, 100 nsec per 32-bit word. Data may then be cluster-compacted by the Model 2738. The concentrated cluster data may then be transferred to a LeCroy standard DATABUS for readout via a Model 4299 DATABUS Interface. Up to 16 system controllers may be connected to a single 4299. In addition, other LeCroy DATABUS systems may be read out along with the 2738 crates.

April 1982

Innovators in Instrumentation



SPECIFICATIONS

Dedicated CAMAC Model 2731

32-CHANNEL DELAY AND LATCH

INPUTS

- Wire-in:** 32 differential ECL inputs via 17-pair front panel headers. Input impedance 112 ± 20 . Input configuration compatible with LeCroy ECLine logic standard. Minimum pulse width 10 nsec.
- Coincidence Gate:** Two differential ECL inputs applied from the Model 2738 via the CAMAC connector. Board mounted jumper selects E1 or E2. Minimum width 30 nsec.
- Test Input:** Two differential ECL inputs applied from the Model 2738 via the CAMAC connector. Board mounted jumper selects E3 or E4. Minimum width 60 nsec. Applies a test input via the 32 pattern gates to the *RIPPLETHRU* inputs. Test level must be logical "zero" for data acquisition. Model 2731 should be inhibited during Test.
- Clear:** Applied via CAMAC Dataway. ECL pulse transmitted via the CAMAC Dataway. Clears all latch within 30 nsec. Minimum width 100 nsec.
- Wire Inhibit:** Applied via the CAMAC Dataway. Common inhibit line set via programmable bit in the 2738. Should be set when applying Test pulse.

RIPPLETHRU CIRCUIT

- Channel-To-Channel Delay Variations:** $< \pm 10$ nsec.
- Delay Temperature Coefficient:** Typically 100 psec/ $^{\circ}$ C
- Delay Range:** 300-682.5 nsec.
- Programming:** 8 bits, 1.5 nsec steps. Set via the Model 2738. Separate delay register per 2731 module.
- Double Pulse Resolution:** 100 nsec or 20% of delay setting, whichever is greater.
- Delay 15:** One front panel output. Lemo connector. Provides channel 15 logic signals of amplitude ≈ 5 mV at the *RIPPLETHRU* delay. Used to check approximate *RIPPLETHRU* delay. Must be terminated in 5 Ω for correct output pulse shape. May be unterminated when not in use.

THRESHOLD CONTROL

- Threshold Programming:** 8 bits, 0.06 μ A steps when used with the Model 2735 or 6 μ V steps when used with the Model 771. Set via the Model 2738. Separate threshold register per 2731 module. Programming level and ground applied to the chamber cards via a single pair of pins on each of the Wire-in input headers. Pin 33 ground and Pin 34 is the programmed level.
- Threshold Monitor:** Two front panel dc test points (threshold and ground). Provides a level of 0.5 V/ μ A when used with the Model 2735 Chamber Card or -5 V/mV when used with the Model 7791 Chamber Card. Polarity selectable by internal jumper, 30 mV per step.
- Threshold Polarity Select:** Internal wire-wrap option. Selects compatibility with 7791 or 2735 cards. Factory wired for Model 2735.

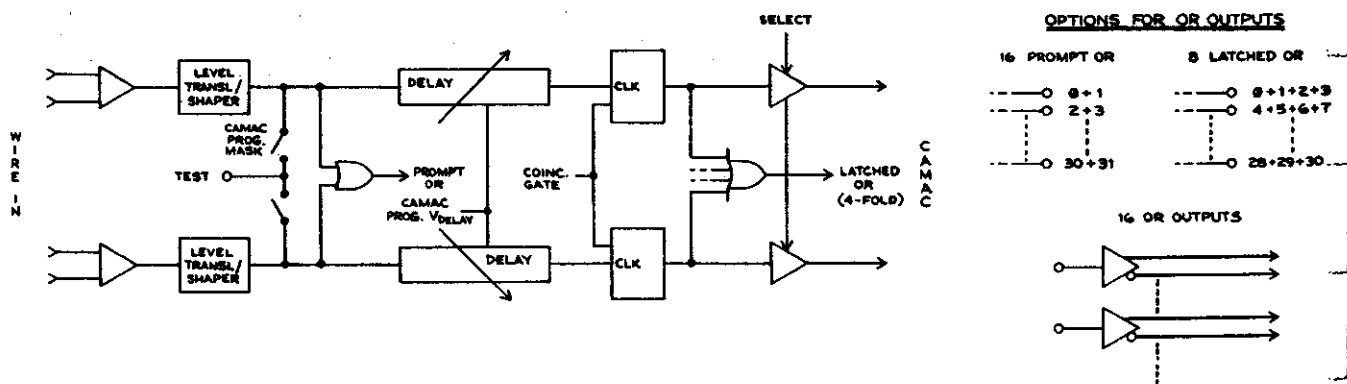
OUTPUTS

- OR Outputs:** 16 differential ECL outputs. Internal wire wrap options allow prompt or latched OR signal (2-fold or 32-fold) to be connected to any of the OR outputs.
- Prompt OR:** Sixteen 2-fold OR signals preceding the *RIPPLETHRU* delay. Available on wire wrap posts within the Model 2731. May be arbitrarily wire ORed to the 16-position internal options connector. Signals approximately equal to the input width plus 35 nsec, available within < 30 nsec of the input.
- Latched OR:** Eight 4-fold OR signals representing the logical OR of the status of 4 adjacent latches. Available on wire wrap posts within the Model 2731. May be arbitrarily wire ORed to the 16-position internal options connector. Levels are valid within 30 nsec of the trailing edge of the coincidence gate.

GENERAL

- Controls:** Leftmost module must have termination of all control lines. Termination via two 8-pin SIP resistors. All modules shipped with SIP's installed. See side panel for location.
- Voltages Used:** +6 V, 950 mA If prompt and latched ORs are not required, ECL drivers may be removed saving 360 mA @ -6 V and 70 mA @ +6 V.
 -6 V, 900 mA
 +24 V, 120 mA
 -24 V, mA
- Packaging:** In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e) RF shielded CAMAC #1 module.
- Caution:** Power up this module only when a PCOS III System Controller, Model 2738, is in the control position.

SPECIFICATIONS SUBJECT TO CHANGE



SECTION 1

SPECIFICATIONS

1.2 System Overview

The LeCroy Model 2731 has been designed as a central element for MWPC encoding. Each 2731 module accepts 32 differential ECL inputs on two LeCroy ECLine standard 17 pair front panel headers. Using LeCroy's unique Ripplethru delay, each Wire-In input is delayed by a programmable amount in the range of 300-682.5 nsec. The delayed data is presented to a Latch which can be activated by coincidence gates as short as 30 nsec.

Computer control of the threshold of chamber discriminators is provided in the Model 2731 via an eight-bit digital-to-analog converter. This threshold programming voltage is provided at both Wire-In input headers. The LeCroy Models 2735 and 7791 chamber cards use this voltage for setting the chamber threshold.

The Model 2731 has provisions for inclusion of the wire chamber data in the first and second level triggers. Prompt ungated logic signals, taken before the Ripplethru delay, are presented as two-fold ORs on the 2731 card. Also, latched logic levels are presented as four-fold ORs on the card. The Prompt and Latched ORs may be arbitrarily user ORed with up to 16 logic signals assigned to the front panel differential ECL line driver outputs. Wire wrap posts are provided for this purpose. These provisions allow the Model 2731 to be custom-tailored to the experimental trigger.

LeCroy's Ripplethru circuit provides delay without adding deadtime. It offers 300 nsec to 682.5 nsec of delay with a double pulse resolution of < 100 nsec. This unique delay scheme offers excellent stability and interchannel matching (<+10 nsec) while providing CAMAC programmability or "electronic cable cutting." The Coincidence Gate, Test Input Signal, and Fast Clear inputs are applied to the 2731 module via the CAMAC Dataway, eliminating the need for costly fanout. The signals are applied by the Model 2738 PCOS III controller which drives the Dataway. The Coincidence Gate defines the time interval for which the wire latches are active. Wire discriminator signals which are received and passed through the Ripplethru delay are latched within the Model 2731 by the Coincidence Gate.

A comprehensive test facility has been built into the PCOS III System. In addition to test inputs on the chamber card, the 2731 can be separately tested. Two 16-bit registers on the 2731 card allow selected inputs to be enabled. The application of a 2738 E3 or E4 NIM pulse applies an input to all enabled channels. In this way, the 2731 circuitry and the track recognition circuitry can both be tested.

The Model 2731 is to be used in a dedicated CAMAC crate using the Model 2738 in the controller station. In this configuration, the 2731 modules can be read out at 10 times CAMAC speed, 100 nsec per 32-bit

word. Data may then be cluster-compacted by the Model 2738. The concentrated cluster data may then be transferred to a LeCroy standard DATABUS for readout via a Model 4299 DATABUS Interface. Up to 16 system controllers may be connected to a single 4299. In addition, other LeCroy DATABUS systems may be readout along with the 2738 crates.

1.3 General Description

The 2731 receiver module accepts differential ECL wire signals from a wire chamber and latches those signals if their leading edge occurs during a gate pulse applied via the CAMAC Dataway. A system controller, i.e., a 2738, supplies the gate signal to the CAMAC dataway for use in each 2731 plugged into the crate. Figure 1.1 illustrates this feature and other features of the 2731. Figure 1.2 shows the timing relationship between ECL wire inputs and the GATE supplied by the 2738 system controller.

The two front panel input connectors are ECLine compatible (see rear pocket for ECLine standards) and provide 32 differential ECL wire inputs. The reserved pair of pins, 33 and 34 on each connector, supply in common to the cards driving these inputs an analog voltage capable of driving 400 ohms to ± 7.65 volts. The 2735 time over threshold discriminator card and the 7791 fixed width discriminator card use this voltage for threshold control. The polarity is internally selectable to either 0.0 volts to +7.65 volts or 0.0 volts to -7.65 volts. The voltage is controlled by an eight bit digital to analog converter in .03 volt steps. The 2375 is programmable to a threshold of 15.3 μ A in 0.06 μ A steps and the 7791 to 1.53 mV in 0.006 mV steps. A threshold test point is available at the front panel for verification of the threshold voltage setting of that module.

The output connector is also ECLine compatible and provides 16 differential ECL outputs from an uncommitted array of drivers. The drivers can be connected to any combination of internal wire ORs of prompt or latched signals.

DLY (15) is an attenuated sample of the output of the internal delay on channel 15. This signal should only be used to verify the approximate delay setting for the module.

The programmable delay requires a minimum width signal input of 60 nsec. This insures that the signal will propagate through the delay to the output. This is similar to a twisted pair cable which requires a minimum input width in order to be recognized at the output of the cable. As a consequence, to accept 10 nsec wide ECL pulses at the input connector, each pulse is stretched an additional 50 nsec. The stretched pulses are OR'ed with the output of a 32 bit pattern register at the input to the programmable delay. A test signal received from the system controller via the CAMAC dataway enables the output of the pattern register onto the input of the delay. The wire signals must be inhibited while the test signal is applied. This can be done via a command in the system controller. The test signal must have a minimum width of 60 nsec. The signals at the input to the programmable delay

are OR'ed together in pairs and then are available for wire ORing to the uncommitted ECL driver array at the front panel output connector. These are the prompt OR signals. Up to 16 pairs may be wired to the output connector in any order the user may choose.

The delay is programmable in 1.5 nsec steps from 300.0 nsec to 682.5 nsec. The delays within a module are trimmed with discrete capacitors to a maximum variation within the module of ± 10 nsec at any delay setting. The delay is measured from the input connector of the 2731 and the gate applied to the E1 input of the system controller. The gate received from the system controller via the CAMAC dataway latches the input signal if the leading edge of the input occurs during the gate. The system controller supplies four different control pulses to the dataway. The gate of the 2731 module can be jumpered to either of two pulses E1 or E2.

The test input of the 2731 module can be jumpered to either of two control pulses E3 or E4. Normally E1 and E3 are selected together and E2 and E4 together.

The outputs of the signal latches are OR'ed together in groups of four and then are available for wire OR'ing to the uncommitted array of ECL drivers at the front panel output connector. These are the latched OR signals and may be wired to the output connector in any order the user may choose.

All 32 latched signals are OR'ed together to produce a LAM for the system controller. The LAM indicates the presence or absence of latched data in the 2731 module. The LAM is not cleared until the latches are cleared by a CLEAR pulse from the system controller via the CAMAC dataway.

Seven commands are accepted by the 2731 module from the system controller: write to the delay, threshold, and 4 pattern registers and read the 32 latches. The write commands, received from the system controller, are controlled by the DATABUS interface. The read command is controlled solely by the system controller during the readout of the crate. Reading occurs at a maximum rate of 10 MHz.

1.4 Functional Description

1.4.1 Wire-In:

Inputs IN A and IN B form the 32 differential ECL inputs to the 2731. The minimum acceptable width is 10 nsec. There is no maximum width. The 17th pair of IN A and IN B are tied together as a programmable voltage output from the 2731. These pairs are the reserved pins as defined in the LeCroy ECLine application note for these ECLine compatible headers.

1.4.2 Coincidence Gate:

Chamber wire signals appearing at IN A and IN B are delayed by the internal delay chips and can be latched if their leading

edge is in coincidence with E1 or E2 supplied via the CAMAC Dataway. E1 or E2 is selected by an internal jumper in the 2731 module. The side panel indicates the position of these jumpers.

The coincidence gate need only overlap the leading edge of the input pulse. The width of the input pulse is not important in determining the gate width. The minimum width of the gate is 30 nsec.

1.4.3 Test Input:

Test pulses can be applied to the 2731 module via a test line jumpered to E3 or E4 at the rear of the 2731 module. The test pattern, previously loaded (see Section 1.4.8), is OR'ed with the wire-in signals when the test line is pulsed. To insure that only the test pattern is latched by the gate, the wire-in signals must be inhibited with the wire inhibit command described in Section 1.4.5.

Since the test pattern is OR'ed before the delay, the coincidence gate must be delayed with respect to the test pulse by the amount of the delay setting in order to latch the pattern. The test pattern will also appear at the prompt outputs if the prompt OR's have been pre-wired. Complete hardware trigger processor testing can then be done using the pattern register and the test pulse inputs. Section 1.4.9 contains a description of the prompt and latched OR pinouts of the 2731.

1.4.4 CLEAR

Module CLEAR, which resets only the data latches, can come from three sources; the System Controller front panel CLEAR and RESET inputs and the master reset generated by the DATABUS Interface. All three sources produce a CLEAR pulse of minimum duration 100 nsec. A new coincidence gate can be generated 20 nsec after the trailing edge of the CLEAR pulse. Minimum width 100 nsec.

1.4.5 Wire Inhibit:

A programmable bit in the 2738 will inhibit wire signals at the input to the 2731. Wire inhibit should be used when testing the 2731 modules via the test pulse and pattern registers since the Test pulse is wire OR'ed with the wire signals.

1.4.6 Ripplethru Delay

Register RO is an 8 bit register that can be loaded by the 2738 System Controller. This register sets the common delay for all 32 channels of the 2731. The delay range is 300 nsec to 682.5 nsec in 1.5 nsec steps. This register can be cleared by loading it with zero via the 2738.

A front panel LEMO output samples the output of channel 15 providing an approximate indication of the delay. If this output is used the cable must be terminated in 50 Ω to provide the correct shape. The amplitude is approximately 5 mV.

1.4.7 Threshold Control

Register R1 is an 8 bit register that can be loaded by the 2738 System Controller. This register sets the common threshold for both ECLine input headers. This register can be cleared by loading it with zero via the 2738. The threshold voltage range is 0 to + 7.65 volts in .03 volt steps. The polarity is jumper selectable at the side panel. The 2731 is shipped with positive polarity selected for use with the 2735 preamp discriminator card.

The programmed level appears on pin 34 of both A and B input headers. Pin 33 is ground. Pin 34 should not be grounded unless the internal wire wrap wire is removed, otherwise an internal 200 Ω current limiting resistor will overheat.

A front panel Threshold monitor allows verification of the Threshold setting.

1.4.8 Pattern Registers

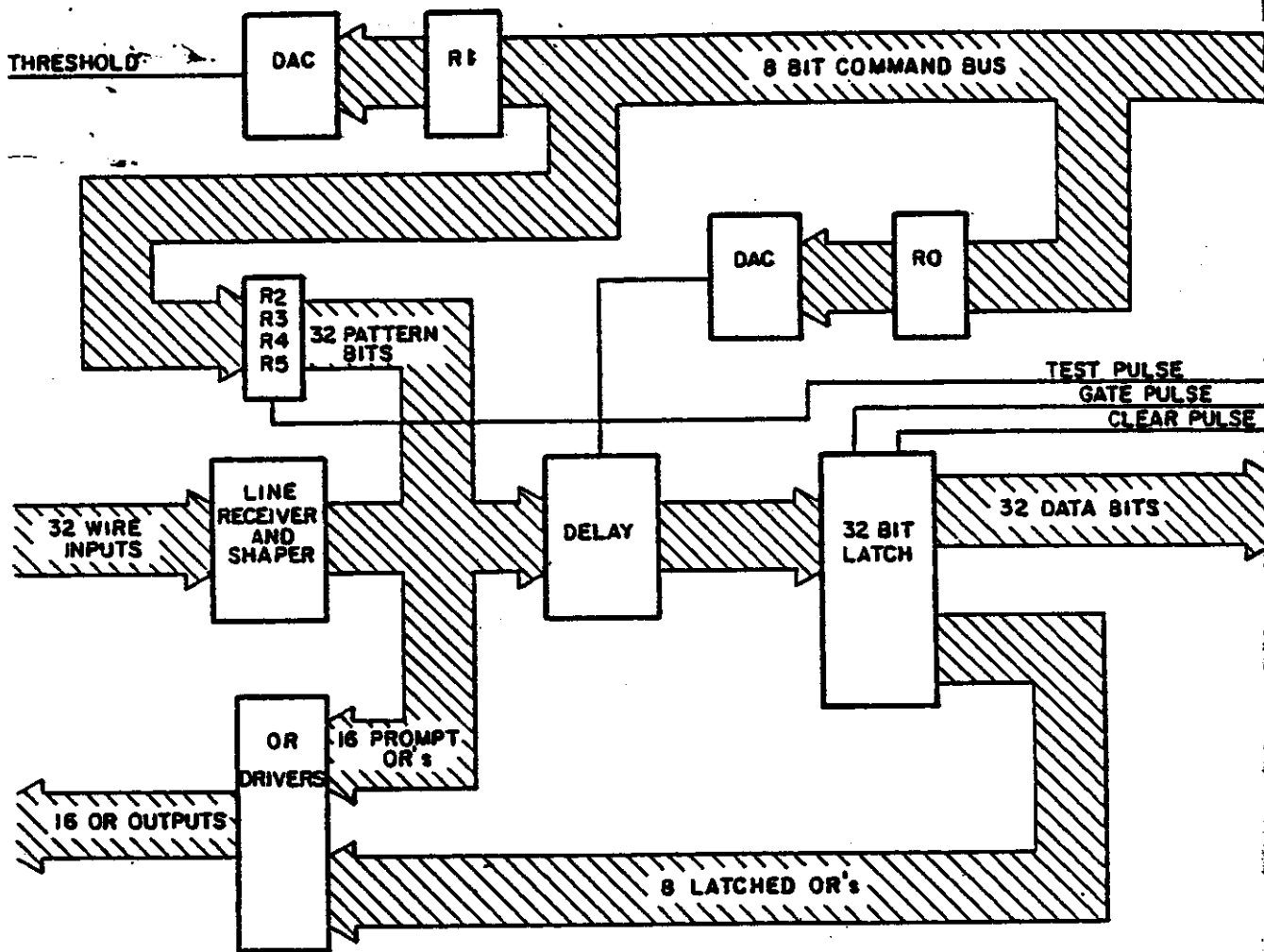
Registers R2, R3, R4, and R5 are 8 bit registers that can be loaded by the 2738 System Controller. These registers determine the pattern to be strobed into the wire signal path by the Test pulse. These registers can be cleared by loading them individually with zero via the 2738.

The strobed pattern appears at the input of the internal programmable delay and at the internal prompt OR's.

1.4.9 User option OR's

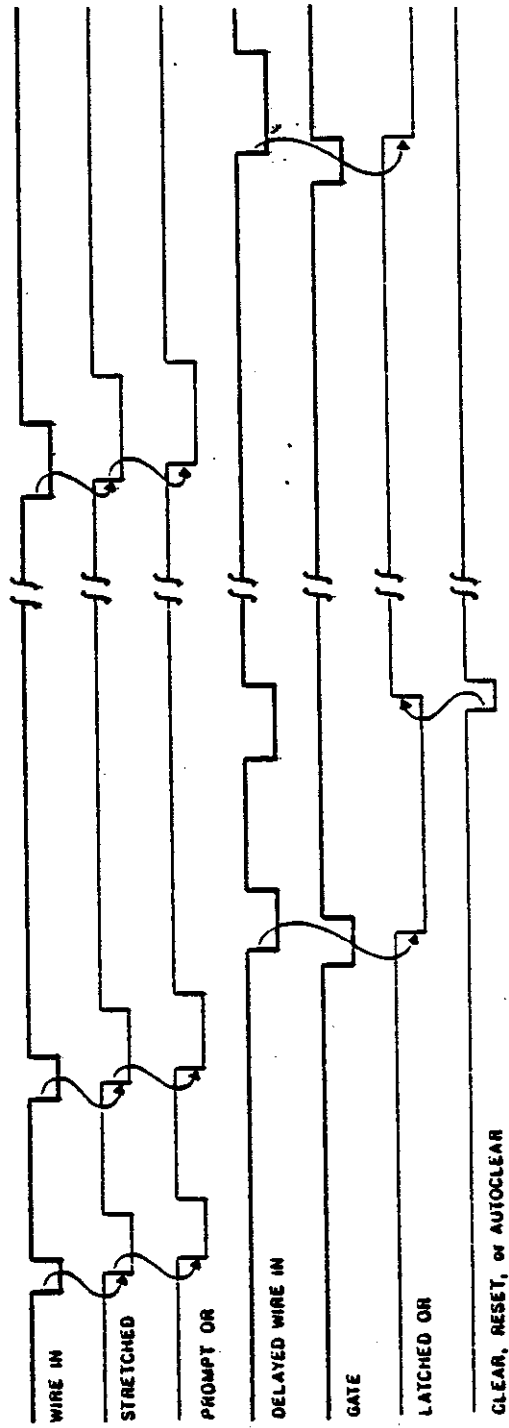
Figure 1.3 gives the location of the latched OR, prompt OR, and OR output wire wrap headers. These internal OR's are TTL open collector outputs which may be wire ORed in any combination to the OR output drivers near the front panel. TTL pullups for these open collector OR's are at the inputs to the OR output drivers.

TTL to ECL drivers dissipate approximately 650 mw including output pulldown resistors. Removing the drivers can reduce the module power consumption by 2.5 watts: 360 mA at -6 volts and 70 mA at + 6 volts.



2731 BLOCK DIAGRAM

Figure 1.1



TIMING DIAGRAM FOR ECL WIRE INPUTS

Figure 1.2

2731 OR W/W Posts

Latched OR's (Pin 1 is ground)

Channels		
12,13,14,15	$\begin{matrix} 2 \\ \circ \\ \circ \end{matrix}$	P6
8,9,10,11	$\begin{matrix} 2 \\ \circ \\ \circ \end{matrix}$	P7
4,5,6,7	$\begin{matrix} 2 \\ \circ \\ \circ \end{matrix}$	P8
0,1,2,3	$\begin{matrix} 2 \\ \circ \\ \circ \end{matrix}$	P9
28,29,30,31	$\begin{matrix} 2 \\ \circ \\ \circ \end{matrix}$	P10
24,25,26,27	$\begin{matrix} 2 \\ \circ \\ \circ \end{matrix}$	P11
20,21,22,23	$\begin{matrix} 2 \\ \circ \\ \circ \end{matrix}$	P12
16,17,18,19	$\begin{matrix} 2 \\ \circ \\ \circ \end{matrix}$	P13

Prompt OR's
(Pins 1,2,11,12 of P14 and P15 are ground)

Channels	Pin	$\begin{matrix} 11 \\ \circ \\ \circ \end{matrix}$	$\begin{matrix} 1 \\ \circ \\ \circ \end{matrix}$
8,9	3	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$
2,3	4	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$
10,11	5	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$
0,1	6	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$
14,15	7	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$
4,5	8	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$
12,13	9	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$
6,7	10	$\begin{matrix} 11 \\ \circ \\ \circ \end{matrix}$	$\begin{matrix} 1 \\ \circ \\ \circ \end{matrix}$
24,25	3	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$
18,19	4	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$
26,27	5	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$
16,17	6	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$
30,31	7	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$
20,21	8	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$
28,29	9	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$
22,23	10	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$

P14

P15

ECL OR outputs

This column is ground

	$\begin{matrix} 1 \\ \circ \\ \circ \end{matrix}$	$\begin{matrix} 02 \\ \circ \\ \circ \end{matrix}$	
	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$	0
	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$	1
	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$	2
	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$	3
	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$	4
P16	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$	5
	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$	6
	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$	7
	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$	8
	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$	9
	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$	10
	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$	11
	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$	12
	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$	13
	$\begin{matrix} \circ \\ \circ \end{matrix}$	$\begin{matrix} \circ \\ \circ \end{matrix}$	14
	$\begin{matrix} 290 \\ \circ \\ \circ \end{matrix}$	$\begin{matrix} 030 \\ \circ \\ \circ \end{matrix}$	15

Latched OR's are in groups of four
Prompt OR's are in groups of two

Any combination may be wire ORed to the ECL OR output header.

For example, wire wrapping pins 4 and 6 of P14 together then to pin 2 of P16, wire OR's channels 0,1,2,3 together as a prompt OR to the front panel of the 2731.

The ECL OR outputs are an uncommitted array of ECL line drivers. The Latched ORs and Prompt ORs can be assigned to any of the 16 OR outputs.

USER OPTION OR's

Figure 1.3

SECTION 2

INSTRUCTIONS FOR INITIAL USE OF THE 2731

2.1 Inspection

Upon receipt of the 2731 it is recommended that a careful inspection be performed to insure that no damage occurred during transit.

The shipping box has been custom designed for this unit and should be saved should shipping be necessary.

After removal from the box, the unit should be examined for physical damage to the front panel, rails, or rear connector.

It is recommended that at this time the 120 ohm terminators at the rear of the module be removed from the unit. Only the module in slot one of the CAMAC crate should contain these terminators.

2.2 Power Requirements

The 2731 uses +24V, -24V, +6V, and -6V in a standard CAMAC Crate configuration.

The worst case power dissipation of 14.0 watts occurs when the input ECLine connectors are not connected or when the power supplies to the 2735 or 7791 cards are off. Proper ECL signals at the 2731 module input connectors causes the least power dissipation. In that case the power dissipation is typically 9.5 watts.

Removing the TTL to ECL OR drivers can reduce this power dissipation by another 2.5 watts.

The crate containing this module should only be turned on when a PCOS III System Controller is in the controller position of the crate.

2.3 Cable Requirements

The 2731 uses standard ECLine 17-pair twisted pair cable.

These cables are optionally supplied with the system as per user requested length specifications.

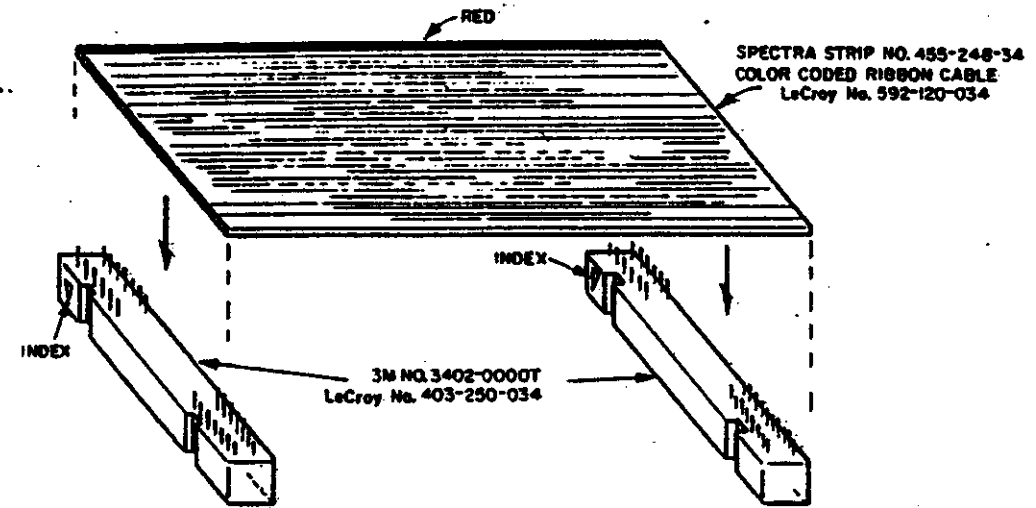
Connectors and cable are available through LeCroy or directly from the manufacturers listed (as well as many others)

Conn Flat Cable/PC 34-Pos for cable w/.050 centers.	- LRS#403-250-034 3-M #3402-0000T
Cable Flat 17 twist pairs Twist 'N' Flat/AWG 28/PVC	- LRS #592-120-034 Spectra-strip 455-248-34

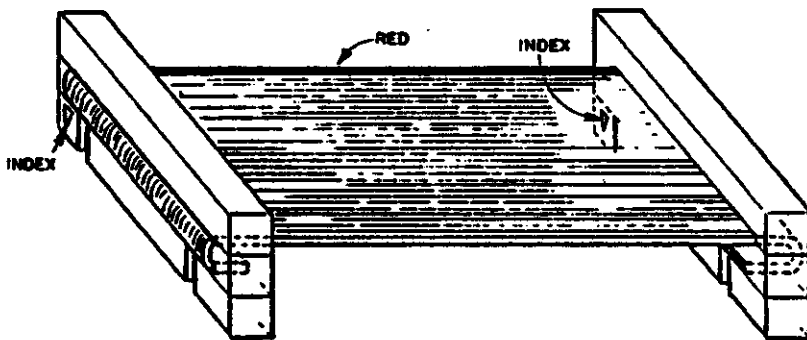
Assembled cable
(See Fig 2.1)

- LRS #DC2/34

Contact your local LeCroy Representative for complete cable ordering information.



ASSEMBLED CABLE WITH STRAIN RELIEF



ECLINE CABLE ASSEMBLY

Figure 2.1

SECTION 3

TECHNICAL DESCRIPTION

3.1 General Comments

High speed readout of the 32 bits latched in the flip flops and use of precision pulses such as GATE and CLOCK required redefining some of the standard CAMAC dataway signals and specifications.

Read and write lines R1 through W8 are used for reading 32 bits at one time. Six pairs of other bus lines transmit differential ECL signals to each 2731 module. A8 and I are equivalent to Z and S1 in normal use. W9 through W16 function as an 8 bit databus for loading the six different registers in the 2731. N, F, A, and I address the appropriate register.

In normal operation less than 5% of the inputs have data. The application of a read cycle by the 2738 System Controller enables 32 drivers to the CAMAC Dataway. Due to termination of these lines in the 2738 and capacitive loading, a large current surge is generated during the read cycle. Inverting one half of the 32 data lines results in a semi-balanced driving of the CAMAC Dataway. The Thevenin equivalent of the terminator is 1.8 volts and 132 ohms. One half of the drivers pull this resistor to ground and the other half to 3.5 volts. Therefore the net current on the dataway is zero. Since radiation, capacitive coupling, ground currents and power supply currents are minimized with this technique, ten megahertz readout rate can be achieved.

Balanced ECL lines for critical signals insures good pulse fidelity at every module. The module in slot one Terminates all the ECL balanced lines with removable 120 Ω terminators.

3.2 Circuit Description

All CAMAC Dataway interfacing is on sheets 1 and 2 of the schematic. Sheet 1 contains the CAMAC decoders, line drivers, and line receivers. The CLEAR ECL input has a low pass filter to minimize sensitivity to glitches on this balanced line. Note that half of the 32 data lines use an inverting buffer 74LS240 and the other half a non-inverting buffer 74LS244.

Sheet 2 contains the power supply filtering and on board regulators. In addition, sheet 2 contains the programmable registers for threshold and delay. Register U16 and DAC U26 comprise a programmable current source for the current to voltage converter consisting of U86, Q1, and Q2. The 200 Ω resistors in the collectors of Q1 and Q2 provide current limiting. The output polarity is selectable by switching U86 from a current to voltage converter to a voltage follower with gain.

Delay is set by register U15 and DAC U25. U86 is a current to voltage converter with offset and gain adjustment potentiometers. The delay range is 300 nsec to 682.5 nsec. The offset pot is adjusted to give a

300 nsec delay between the ECL inputs of this module and the E1 inputs of the 2738 System Controller. Calibration is easy to perform if a computer program is written to display the number of hit channels while driving all 32 ECL inputs. Adjusting offset at 300 nsec delay and gain at 682.5 nsec delay to give 16 channels on calibrates the unit.

The ECL OR output drivers are illustrated on sheet 3. These TTL to ECL converters are driven by the open collector TTL OR's generated from the prompt and latched outputs.

Each monolithic delay chip contains four signal channels and one reference channel. Since every channel is identical in function, schematic sheets 4 and 5 do not include every channel. Each sheet illustrates four channels and the reference channel of one delay chip. The drawings list the chip numbers and the channel number.

The delay of the MDD500 chip is set by adjusting the power supply to the chip. The fifth channel or reference channel is identical to the four signal channels, therefore controlling the delay of the reference channel is equivalent to controlling the delays of the signal channels. A crystal controlled clock (500 KHz) resets the LS 279 (U40) in the reference channel, after the delay the LS 279 is set. This negative going pulse from U40 has a width equal to the delay and period equal to the clock. The CMOS inverter 4069 (U 41) inverts this pulse. The output pulse of the inverter will have a duty cycle proportional to the delay. The power supply to the CMOS Hex inverter is derived from a 5 volt reference and therefore stable with time and temperature. A simple average of the output of the inverter will produce a voltage proportional to the delay. Op amp U42 compares this voltage with voltage VDEL from the delay DAC and generates an error voltage which corrects the MDD500 power supplies. Changing VDEL changes the delay of the reference channel and in turn the delays of the four signal channels.

As manufactured matching of the MDD500 channels is +20 nsec requiring a trim procedure to meet the 2731 specification of +10 nsec. A small capacitor of value 2.2 pf to 39 pf placed at the output of each channel of the MDD500 increases the delay by approximately 2 nsec to 39 nsec respectively if the programmed delay is set for 590 nsec. A computer program is available for trimming 2731 modules which generates a table of capacitors to be added to each chip. The Fortran program currently runs on LeCroy's 3500 CAMAC Acquisition and Control System. Changing an MDD500 or an LS112 will require retrimming those four channels.

A signal channel operates as follows: The differential ECL wire input is received by a 10115 line receiver, stretched by a resistor capacitor network, level shifted by a transistor, wire ORed with the pattern generator output, delayed by the MDD500, and latched by the LS112 if a gate occurs in time with the delayed leading edge of the wire in signal. A prompt OR is picked off at the input to the delay and the latched OR at the Q output of the LS112. Both ORs are buffered before further wire ORing by the user. The Q output of the LS112 drives the CAMAC Dataway line drivers.

The MDD500 is subject to latch-up if the power supplies turn on in the

wrong sequence. The 2738 System Controller supplies two start signals on power up to sequence the power to the MDD500's in the right order. START 1 disables the inputs for 0.5 sec by raising the -2 V supply of the level shifting transistors to -1.5 volts. START 2 forces all delays to minimum delay for 1 sec. This ensures startup under all power supply sequencing. Programmed inhibit from the 2738 also raises the -2 V supply to -1.5 V.

ECLine APPLICATION NOTE

WHAT IS ECL?

The emitter coupled logic (ECL) is a standard followed by several integrated circuit manufacturer and it is the today's fastest form of digital logic. The logic levels here used are respectively:

0 = LOW = -1.75 V

1 = HIGH = -0.9 V

with a logic swing then of 0.85 V. This can be easily compared with, for instance, the more popular NIM standard where the logic levels are:

0 = HIGH = 0 V

1 = LOW = -0.8 V

with a logic swing of 0.8 V.

The two standards have then almost the same logic swing even if different DC levels.

WHY ECL?

In today's electronics, most of the NIM and CAMAC fast logic circuits, largely make use of ECL integrated circuits. In order to make input and output levels compatible with NIM standard, NIM to ECL and ECL to NIM level adapters, have to be introduced as input/output stages, making the circuits, to no purpose, more costly and power consuming. The natural solution is then to use as standard input/output logic levels, the ECL levels themselves.

Furthermore, the ECL standard easily provides and easily accepts complementary pulse pairs thus allowing, for interconnections, the use of cheaper twisted pair cables and high density connectors.

Other straightforward advantages using ECL complementary levels are:

- a better noise immunity without any appreciable loss in bandwidth;
- the possibility to avoid ground currents and ground loops as occurs with single ended pulses;
- the input impedance of ECL circuits being intrinsically high, many circuits may in principle be fed by the same pulse, a termination being needed only on the last circuit fed.

INNOVATORS IN INSTRUMENTATION

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WHY ECLINE?

ECLine stands for a new line of CAMAC logic units, handling fast signals at ECL levels, motivated particularly by the new generation of high energy physics experiments involving extremely high counting rates and/or large detector arrays. There indeed, new needs impose severe limits on cost and space per channel as well as an automatic computer control as extended and flexible as possible.

Recognizing these new needs and in order to answer them, LeCroy has developed a new line of ultra fast, high density programmable modules, allowing the experimenter to achieve full computer control and monitoring of his data acquisition system within a single instrumentation standard.

The new ECLine features:

- Low cost,
- High density,
- High performance,
- CAMAC programmability,
- Complementary ECL inputs/outputs,
- simple, reliable system interconnection via inexpensive twisted pairs or flat cables.

ECLINE ORGANIZATION

From the user point of view, the following points in ECLine organization should be pointed out:

- a) Connectors used and pin allocation,
- b) Front panel organization of modules,
- c) Module interconnections,
- d) Interconnections with old standards.

a) CONNECTORS USED AND PIN ALLOCATION

Lemo type connectors are used for inputs everywhere long coax cables are expected to bring signals, as in the case of the 4416 discriminator, or when signals are expected to come from a simple logic, as in the case of strobe or test or veto inputs.

Lemo type connectors and NIM levels are used for outputs, every time signals are expected to go to a simple logic, as in the case of majority outputs or of synchronization outputs.

Everywhere else, to build up logic confined in the ECLine frame work, 34 pin (2x17) connectors are used, suitable for twisted pair cables. These connectors are largely produced by several manufacturers, for instance: AMP, 3M, BERG. The pin allocation is shown in Fig. 1, an arrow on the front panel is always indicating first channel in a connector and channel sequence. Pins 33 and 34 are unconnected and unused at the moment (reserved for future applications). The pin allocation is compatible with the "Specification for ECL front panel interconnections in counter logic" given by CERN.*

*) CERN, EP-Electronics Note 79-01

b) FRONT PANEL ORGANIZATION OF MODULES

All modules actually produced in the ECLine are single width CAMAC modules. The front panel is organized in four sections, each of them being able to house a 34 pin connector. The pin allocation in each section is shown in Fig.2 and it has been chosen with the purpose to make interconnections between different modules as easy as possible. When needed one or more sections are devoted for housing different components, as for instance Lemo type connectors, LED displays, trimmers, etc.

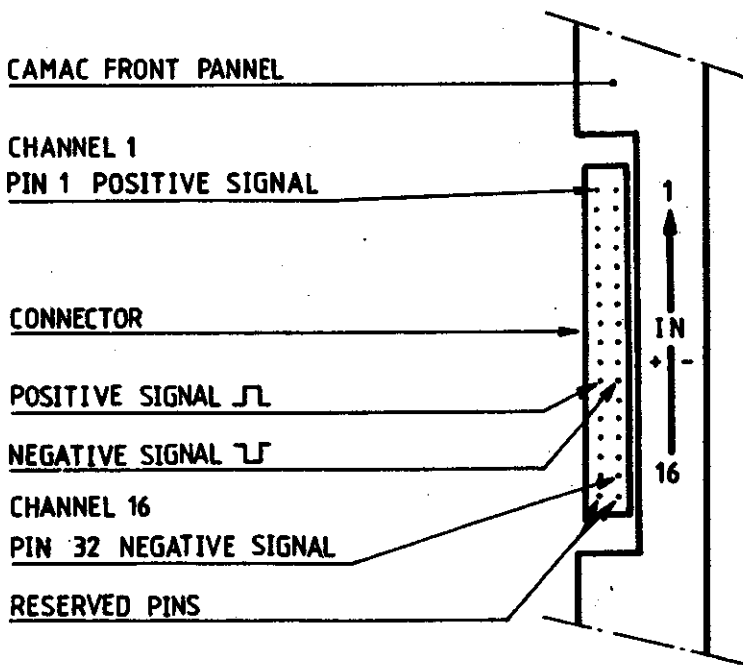


Fig. 1

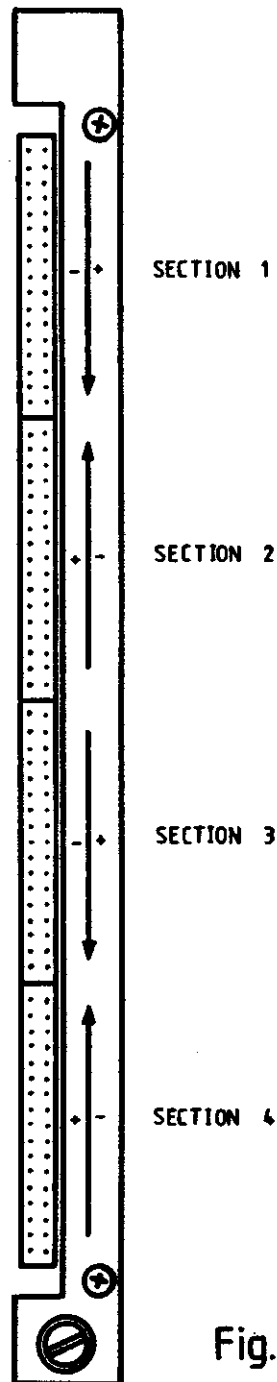


Fig. 2

c) MODULE INTERCONNECTIONS

According to the needs, interconnections between module can be made either with single twisted pairs cables and connectors, or with flat multiwire cables. Non-twisted multiwire flat cables may be used for distances not in excess of few tens of centimeters, or when fast risetimes are not essential and higher crosstalk is acceptable. Twisted pair cables of nominal 100 Ω impedance, should otherwise be used.

Input connectors are always followed inside the module by a SIL connector housing the standard resistor array for input termination. The resistor array can be removed to make a high input impedance thus allowing several modules be driven by the same source, in a bus configuration. Last module in a bus should keep of course the resistor array termination.

Fig. 3 shows an example of bus where circuit 1 is the pulse source feeding circuits 2, 3, 4 and 5. In this example modules 2 and 5 should contain the termination resistors.

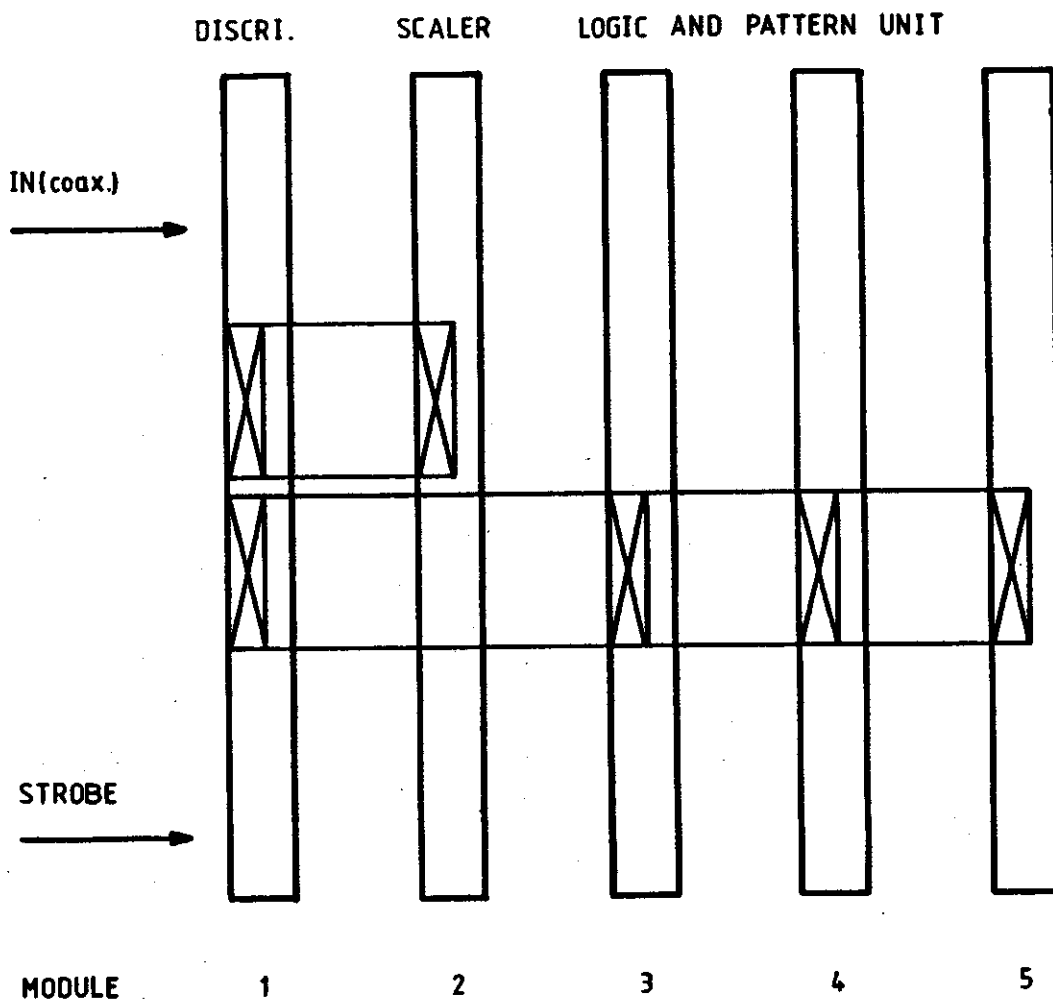


Fig. 3

d) INTERCONNECTIONS WITH OLD STANDARDS

The ECL standard is not directly compatible with grounded connectors used for instance in classic NIM circuits or in oscilloscopes. That's why the LRS ECLine provides also modules for NIM to ECL and ECL to NIM translation, and a specially designed differential active probe.

But where frequency is not a problem, a very simple translator can be home made as shown in Fig. 4.

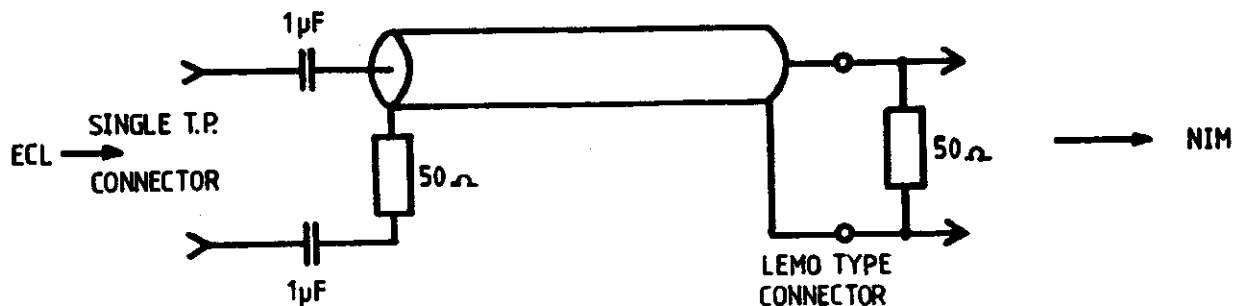


Fig. 4

APPLICATION EXAMPLES

The potentiality of the ECLine is so strong, that we don't hesitate to say that it represents a step forward in the conception of logic for experiments. Any logic problem can in principle be solved in a compact way and under computer control. We will give few examples showing this, but a better way to get in touch with ECLine will be to propose us your logic problem, we will then help to solve it.

a) Automatic coincidence curves.

That's a typical application of the model 4416 discriminator and of the model 4418 programmable logic delay. Two possible set-ups are shown in Figs. 5a and 5b in order to show two different topologies for the interconnecting cables. The application presumes a unique light source for the PM's, triggered by the same pulse generator giving the strobe pulse.

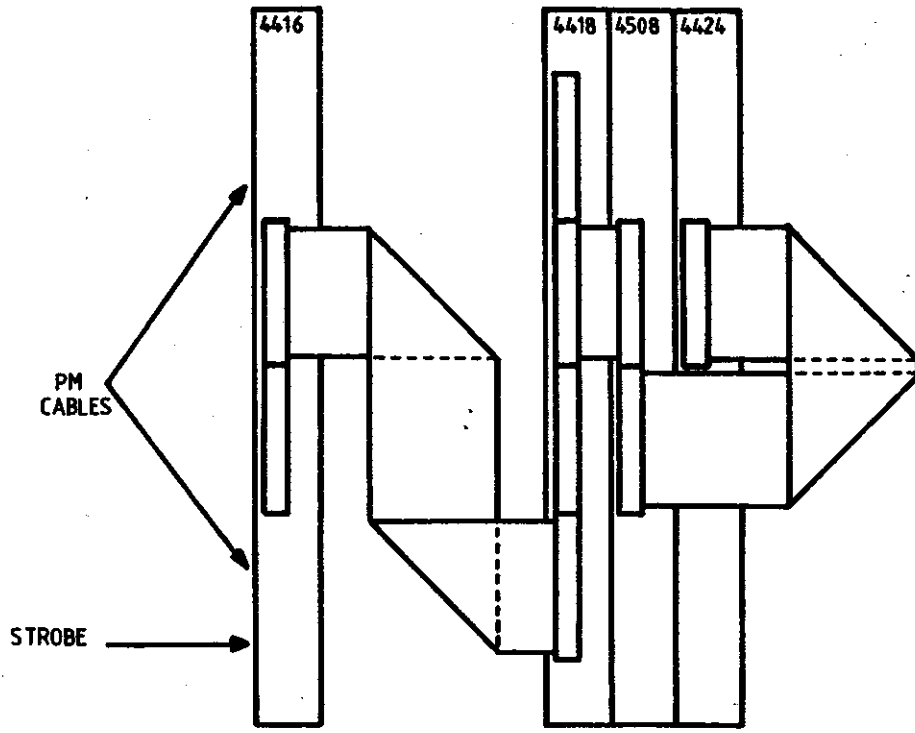


Fig. 5a

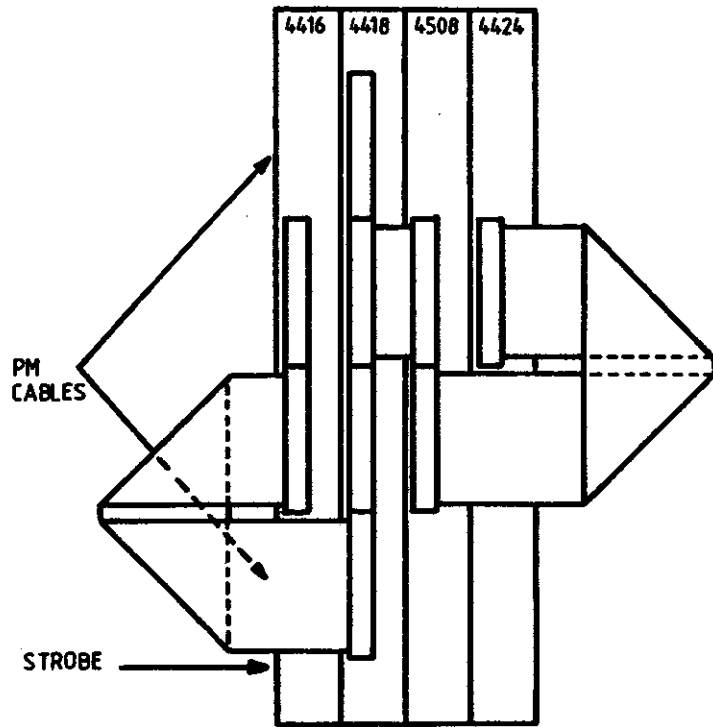


Fig. 5b

b) Mixed logic.

Let's consider the bloc diagram shown in fig. 6. This could be a typical example of a trigger, built on eight counters plus a strobe. There are two ways to implement it using ECLine. The slower one consists of using the 4516 3-fold logic unit; in this case interconnections have to be made between outputs and inputs via single twisted pair cables. Four sections ($\frac{1}{4}$ of the module) will do the job (enclosed in dotted lines in Fig.6) but the dotted outputs will not be available. The fanout of two can be made using a bus configuration for those outputs; the complementary output can be obtained just inverting the cable connection. The input to final output delay will be of the order of 22 nsec plus interconnecting cables.

Another way to solve the problem is to use one section (half a module) of 4508 fully programmable logic unit. There the only operations required will be to connect the inputs and program the Boolean expression via CAMAC. The eight outputs will then be available. The input output delay will be of the order of 20 nsec. A strobe input is equally available.

A nice feature of the module is also that the input pattern is latched at the strobe arrival, so that an off-line reconstruction of the trigger is always possible.

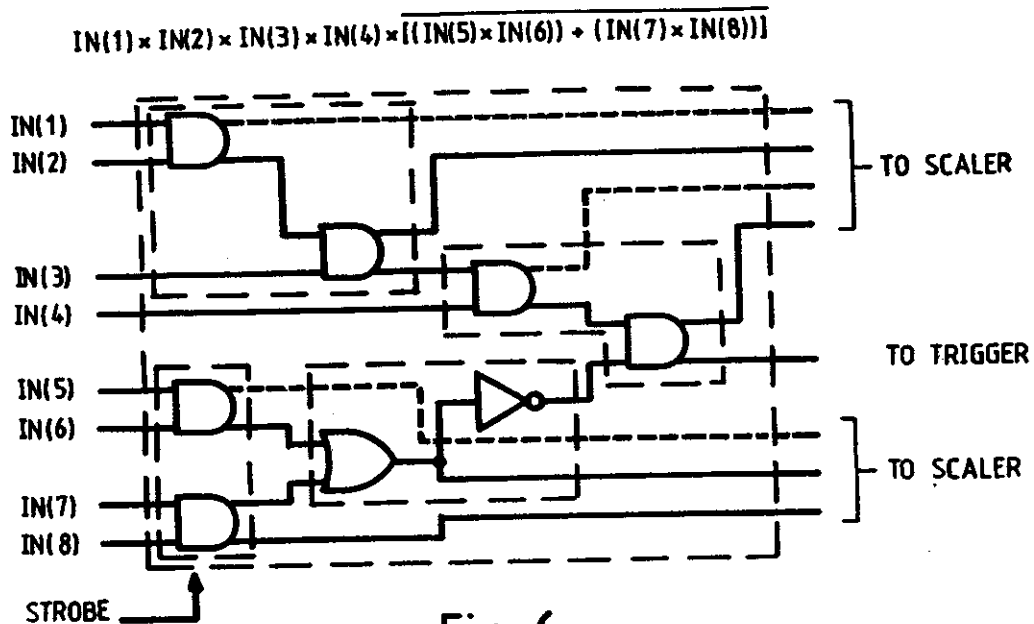


Fig. 6

c) Coincidence matrix.

That's another typical application in high energy physics where two hodoscopes of counters have to be correlated in order to have a trigger only when collinearity criteria have been respected. The example we want to discuss is the one of two hodoscopes of 16 counters each.

The implementation of the problem by ECLine, which uses two modules 4508 fully programmable logic units and one 4516, 3-fold logic unit, is based on the idea of generating for a given pattern of counters on the first hodoscope plane a predicted pattern for the second one. Then make a comparison of the predicted with the real pattern on the second hodoscope by a bit to bit coincidence. The result of this operation will be a 16 bit word, containing one's where collinearity has been respected, which can either be sent to a pattern unit, or the 16 bits can be OR-ed to give a trigger.

The realization is shown in fig. 7. Each 4508 section produces in output an 8-bit predicted pattern. On the other hand, each group of eight counters of A-plane can have an influence, a priori, on each of the sixteen counters of plane B. This is due either to the set-up geometry, and/or to the possibility of a bending magnet between the two planes. This explains the bit-to-bit OR. The predicted pattern has to take care also of the fact that the shadow of each A counter could cover more than one B counter.

All that can be easily introduced into the computer program loading the 4508 program. The bit to bit AND is made in the second half of the 4516. The 4516 will provide in output both the 16 bit final pattern and the 16 bit general OR. The total decision time will be less than 40 nsec. The method shown is able to handle any multiplicity of tracks in the hodoscopes, as well as it can be in principle extended to any number of counters.

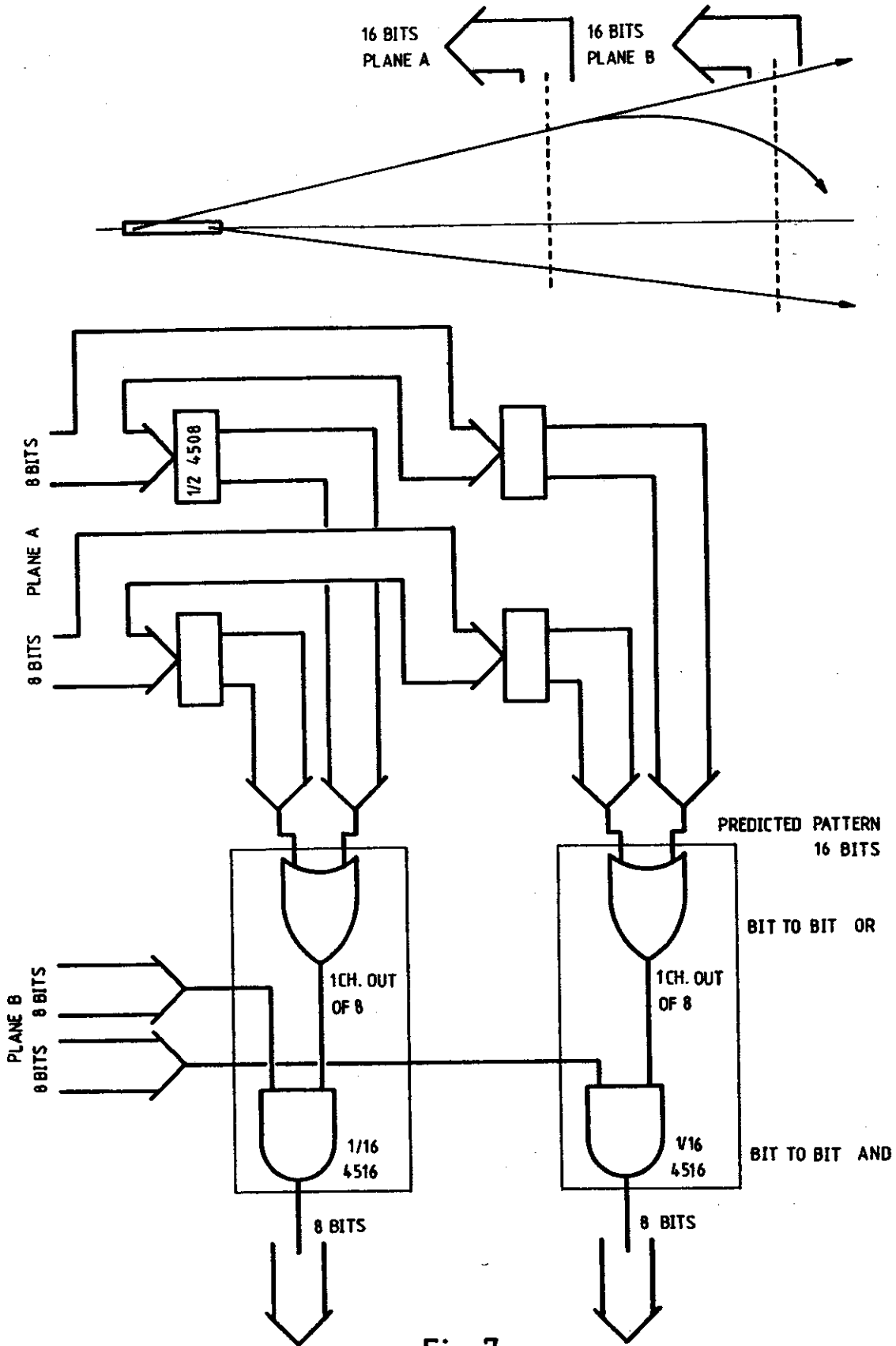


Fig. 7