2738

PCOS III

CONTROLLER MANUAL

March, 1982

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TECHNICAL DATA

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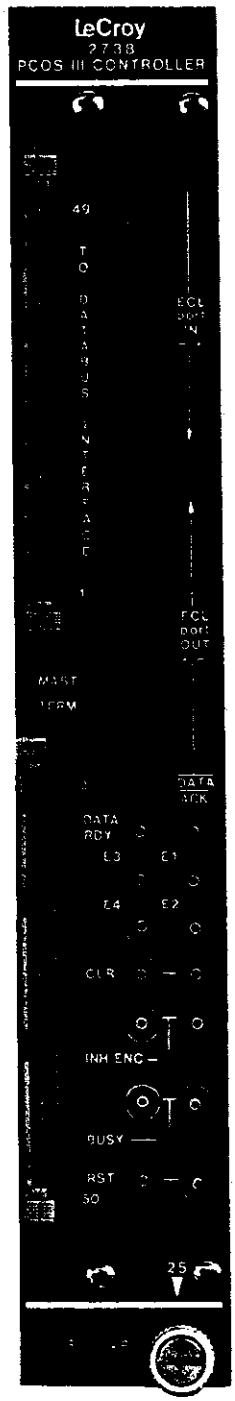

PCOS III
Dedicated CAMAC Model 2738
MWPC Digital Readout Controller

The LeCroy Model 2738 is the system controller for MWPC encoding with the PCOS III System. One Model 2738 double width CAMAC module occupies station numbers 24 and 25 of a dedicated crate of LeCroy Model 2731 32-Channel Delay and Latch modules for a maximum of 736 wires per crate. The Model 2738 System Controller performs the readout, encoding, and control functions for the 2731 modules and serves as a interface to the LeCroy DATABUS. Communication is achieved via either a LeCroy Model 4299 DATABUS Interface and Memory Module which is resident in the CAMAC data acquisition system or a user-supplied fast ECL interface using the Model 2738 ECLport out connector.

The Model 2738 offers both ECLport readout encoding and data compacting at 10 megawords per second, ten times the maximum CAMAC data transfer rate. The Model 2738 determines the addresses of all wires which were hit and then stores these addresses in a 1k by 16 buffer memory which is interfaced to the LeCroy DATABUS for lower rate transmission of the hit wire addresses via the Model 4299. Internal switches in the Model 2738 allow the implementation of a hardwired cluster centroid calculator. In this mode of operation, the address of the cluster centroid (14 bits) and the width of the cluster (4 bits) are transmitted as successive data words. The internal switches determine whether clusterized or unclusterized data is available at both the DATABUS port and the ECLport.

The ECLports of the Model 2738 PCOS III System Controller can be used for both cluster calculations that transcend dedicated crate boundaries and track recognition logic. Master/Terminal switches set the status of each 2738 module in a multicrate system. Cluster calculations transcending a crate boundary can then be achieved by connections between the ECLport OUT and ECLport IN of the crates in question. If all of the crates in a PCOS III System were connected together via the ECLports, the master crate (the crate closest to the Model 4299) becomes a master controller. Even with this arrangement it is still possible to communicate to the track recognition logic via the ECLport OUT of the master crate.

The Model 2738 accepts NIM control signals and distributes them to the 2731 modules via the CAMAC Dataway. The system accepts four control lines: E1, E2, E3, E4 and a bridged high-impedance Clear Input. The receiver modules may be assigned to the control lines via internal jumpers.

The value of the chamber discriminator card thresholds (LeCroy Models 2735 or 7791), the value of the delay settings for the LeCroy Model 2731 Delay and Latch, the module addresses for the Model 2731s, and the test patterns are transmitted as datawords from the data acquisition system via the LeCroy Model 4299 DATABUS Control Module to the PCOS III System Controller. This protocol allows the user to determine chamber plateaus, to optimize the required delay ("electronic cable cutting"), to assign any 9-bit address to any 2731 module for complete system control, and to OR a test pattern with the, model 2731 wire inputs for system tests.

February 1982

Innovators in Instrumentation

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SPECIFICATIONS
Dedicated CAMAC Model 2738
PCOS III CONTROLLER

CONTROL INPUTS AND OUTPUTS

E1, E2, E3, E4:	NIM level inputs (≤ – 600 mV). Input impedance 50 Ω; selection of E1, E2, E3, E4 via jumper option in receiver modules; trailing edge of E1 initiates encoding. See receiver module specifications for minimum widths and usage.
Clear Encode:	NIM level input (≤ – 600 mV) clears the encoder section of the Model 2738 and 2731 latches within 100 nsec. High impedance front panel bridged Lemo pair suitable for daisy chain operation may be applied at any time. Minimum width 100 nsec.
INH Encode:	NIM level input (≤ – 600 mV) prevents encoding; may not be asserted after encoding has begun. High impedance front panel bridged Lemo pair suitable for daisy chain operation.
Busy Encode:	NIM level output (≥ 16 mA) indicates encoding in process. Lemo connector bridged suitable for daisy chain to indicate total system status. Busy is asserted ≤ 100 nsec after the trailing edge of gate 1 until the encode cycle is complete.
Reset:	NIM input (≤ – 600 mV) clears Model 2731 latches and 2738 memory within 100 nsec. High impedance front panel bridged Lemo pair suitable for daisy chain operation. If applied during DATABUS readout, the Model 4299 must be reset via its RT input.

USER OPTION SWITCHES—SIDE PANEL ACCESSED

Address:	Four, 2-position switches, #1, 2, 3, 4. Defines the address of Model 2738 for communication via DATABUS. Address = 4321. "Open" = "1".
LAM Enable:	Two position switch, #5. Generates LAM Request in 4299 at end of readout cycle. "Closed" to disable LAM Request.
DATABUS Control:	Two position switch, #6. Automatic readout of the data in the buffer memory to the Model 4299. The 2738 local memory can be at any time read by using the 2738 Reread Command. "Closed" for automatic readout.
Terminal:	Two Position Switch, #7. Turns on the front panel "Terminal" LED. This indicates that this controller is furthest from Master. It serves to terminate Data Encoding. If there is no ECLport daisy chain both Master and Terminal switches must be on. "Closed" turns on Terminal LED.
Master:	Two Position Switch, #8. Turns on the front panel "Master" LED. This indicates that this controller processes all data on the ECLport daisy chain and stores the data for readout. "Closed" turns on Master LED.
ECLport Source:	Two position switch, #9. Selects data before or after Data Pipeline. "Closed" to select data before Data Pipeline.
Pipeline Mode:	Two position switch #10. Enables the clusterizing mode of the Data Pipeline. Internal memory always reads the output of the Data Pipeline. "Closed" for non-clusterizing mode.

ECLport:

Data Ready:	NIM level (≥ 16 mA) indicates data at ECLport are valid. Data Ready is asserted 30 nsec after ECLport data are valid.

Data ACK: NIM level (≤ – 600 mV) inhibits data transfer to ECLport. Left open, data appear at ECLport at 10 M words/sec. If Data ACK is driven to the 0 mA state for 20 to 80 nsec, one word is transmitted to ECLport output. If Data ACK is in the 0 mA state for > 80 nsec, > 1 word may be presented at ECLport.

ECLport In: 17-pair header; accepts 16-bit differential ECL signals from ECLport out of the previous Model 2738 in an ECLport chain.

ECLport Out: 17-pair header provides 16-bit differential ECL signals in same format as CAMAC data, see below (delimiter word not transmitted). Output configuration defined by the ECLine standard. See LeCroy ECLine application note.

2738 COMMANDS

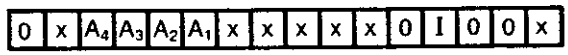
Commands via the Databus cable are based upon simple binary coding as follows:

Symbol Definitions:

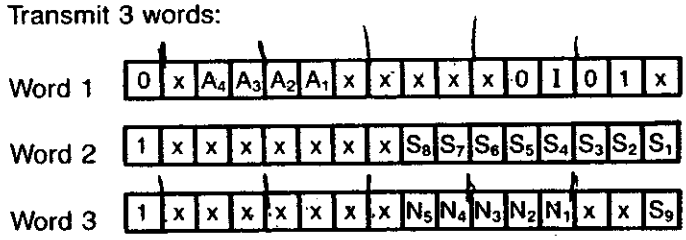
A : 4-bit Controller Number:	A_1-A_4
S : 9-bit Logical Address:	S_1-S_9
N : 5-bit CAMAC Station:	N_1-N_5
V : 8-bit Register Value:	V_1-V_8
R : 3-bit Register	R_1-R_3
X : Don't Care	

Consult the DATABUS Interface manual for details of data transfer.

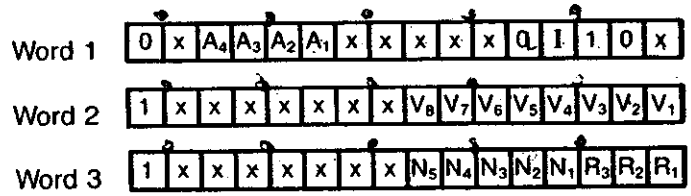
Wire Inhibit: Disables all data inputs. used during exercise of test pattern.
I = 1 implies wire inhibit. I must be maintained in all subsequent command words.



Assign Logical Address: Transmit 3 words:

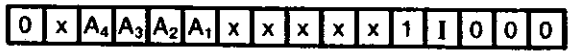


Module Write: Eight-bit value, V, sets Threshold, Delay, or pattern. Transmit 3 words:



Register (R)	Description
0 (000)	Delay 300-682.5 nsec in 1.5 nsec steps.
1 (001)	Threshold 0-15.3 μA in 0.06 μA steps
2 (010)	Test patterns wires 0-7
3 (011)	Test patterns wires 8-15
4 (100)	Test patterns wires 16-23
5 (101)	Test patterns wires 24-31

Reread Command: Causes transfer of present contents of buffer memory to the Model 4299.

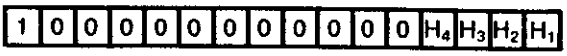


Master Reset: Used to clear 2738 and enable for data taking. Initialed by F(9)•A(0) + A(1)) applied to Model 4299.

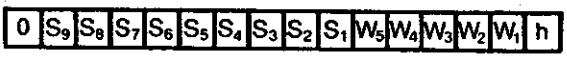
OUTPUT FORMAT

Returns wire address, W, plus logical module address S. Wire address includes "half wire" bit, h, from centroid calculation. H is width of Cluster.

Clusterized Data:



width



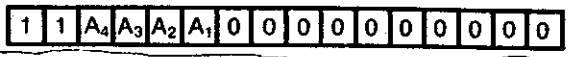
address

:

width

:

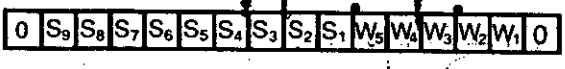
address



delimiter word

HEADER WORD — WORD COUNT

Non-Clusterized Data:



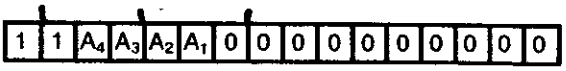
address

:

address

:

address



delimiter word

GENERAL

Voltages Used: +6 V at 5.3 A.
−6 V at 1.0 A.

Packaging: In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR 4100e) RF shielded CAMAC #2 module.

SPECIFICATIONS SUBJECT TO CHANGE.

LeCroy

TABLE OF CONTENTS

SECTION 1

PCOS III SYSTEM OVERVIEW

1.1 System Description

1.1.1 Introduction

PCOS III is a complete, proportional chamber operating system. It is a third generation system built upon the experience gained with PCOS I and PCOS II. High performance and simplicity are achieved through the use of new, large-scale custom integrated circuits. Four-channel amplifier, discriminator, and delay circuits have each been designed to give PCOS III the ultimate simplicity. Its design structure will allow the system to be easily upgraded to the FASTBUS standard in the future.

PCOS III employs chamber-mounted amplifier/discriminators and remote delay, latch, and readout. This configuration allows much of the electronics to be located remote from the detector if access is restricted. The delay, latch, and encoding circuitry can also be located near the detector to minimize cable runs and hence, overall cost.

Special emphasis has been placed on the system's ability to handle high rates. A unique RIPPLETHRU circuit offers programmable delay of up to 682.5 nsec and allows input rates to 10 MHz. Use of a fast parallel encoding allows the system to process valid events extremely rapidly. Multiple levels of digital buffering affords the fastest possible CAMAC readout.

PCOS III allows use of chamber signals in the trigger decision. It offers prompt and latched logic outputs. Both are provided to match the LeCroy ECLine logic system, allowing maximum flexibility and speed. A test input allows any pattern to be gated to the wire inputs after the line receivers.

The versatility of PCOS III is further enhanced by a high-speed ECLport, allowing addresses of hits or clusters to be transmitted to a modern trigger processor for track recognition analysis.

PCOS III offers computer control of discriminator thresholds and of the RIPPLETHRU delays. This allows for "plateau" of the chamber cards and "electronic cable cutting" for coincidence timing, both under software control.

1.1.2 General Description

PCOS III contains the circuitry to amplify, discriminate, delay, latch and encode multiwire proportional chamber signals. The system includes chamber-mounted amplfier/discriminator cards, 32-channel receiver modules Model 2731 and a System Controller (Model 2738). Up to 23 of the Model 2731 modules (736 wires) can be operated in a dedicated CAMAC crate with a Model 2738 System Controller.

Chamber Discriminators

PCOS III employs industry-standard ECL levels between the chamber discriminators and the latch modules. These digital signals are suitable for driving long cables. They are differential, providing good noise immunity and they are of standardized amplitude, eliminating leading-edge slewing effects.

Because of the diverse nature of MWPC systems, LeCroy provides a variety of products designed for the application. Both multi-channel chamber cards and components are available. These are summarized below.

Chamber Cards

Three 16-channel chamber cards are available. All accept inputs via a PC edge connector either negative or positive and provide differential ECL outputs via a 17-pair header.

Model 7791 - The largest of the chamber cards (14 cm x 32 cm) and also the highest performance. This card offers 200 Ω input impedance, differential inputs, excellent sensitivity (± 250 μV) and low slewing (< 2.5 nsec, 2x to 20x). The 7791 provides monostable-set output width of 100 - 800 nsec. Wide output widths are particularly useful for driving long cables. Power dissipation < 0.5 w/channel.

Model 7790N - Identical electrically to the Model 7791 but optimized for small size (9.4 cm x 28 cm) at the slight expense of sensitivity (± 350 μV).

Model 2735 - The smallest and most economical of the chamber cards, only 9.1 cm x 12 cm overall. The unit provides a true current - sensitive input (< 100 Ω) with 2 μA sensitivity and jumper - selectable input polarity. The output width is equal to the time over threshold. This card is well suited for large detector applications. Power dissipation < 0.32 w/channel.

Components

LeCroy has designed three integrated circuits for chamber discriminator applications. These components allow the chamber discriminator to be custom taylored to the application. circuits can be arranged to match the modularity of the chamber, to minimize power dissipation or to minimize the number of chamber-mounted components when access is limited or background radiation is high. A summary of the components is given below.

TRA401 - A low noise (< 0.25 μA rms), 4-channel amplifier designed for wire chambers. The unit offers fast < 4.4 nsec - rise and fall times. Each channel provides a current-sensitive input (< 100 Ω), a gain of 12.5 mV/μA and a single-ended output suitable for driving a 100 Ω line. May be mounted on a chamber with remote discriminators, minimizing the chamber mounted electronics while achieving a power dissipation of < 140 mW/channel. When used with

the MVL406 quad discriminator an exceptionally compact overall circuit can be constructed. Packaged in an 18-pin DIP.

MVL406 - A 4-channel discriminator designed for use with the TRA 401. Provides ECL line driver outputs and threshold sensitivity of less than 20 mV. Packaged in an 18-pin DIP.

MVL100 - A complete wire chamber discriminator, provides amplifier, discriminator, output width monostable and ECL line driver in 16-pin DIP. Feature $\pm$ 250 μV sensitivity and $<$ 2.5 nsec slewing (2x to 20x). Used in the Models 7790N and 7791.

Reciver Modules

The Model 2731 is a 32-channel wire input receiver module designed for MWPC applications which require the wire chamber data in the system trigger. User-configured prompt 2-Fold OR's and Latched 4-Fold OR's are available for first and second level trigger decisions. The unique software programmable Ripplethru delay provides delay for each channel accounting for trigger logic delay. The Ripplethru offers a range of 300 to 682.5 nsec.

Readout

The hit-wire data contained within the Receiver Modules are stored as a 32-bit word. The Models 2731 and 2738 communicate via 32-bit data transfers 15 times in excess of the maximum rate defined by the CAMAC standard. The Receiver Modules provides LAM signals to allow only those modules containing hits to be read.

Test Feature

A 32-bit pattern may be down-loaded into each Model 2731, causing the selected inputs to be strobed by the test input of the Model 2738. This allows the hardware processors and the 2731-2738 encoding logic to be completely exercised. The Model 2738 provides NIM-to-ECL conversion and distributes the test signal via the Dataway. Coincidence Gates must be provided with the appropriate delay.

Fast Clear

A CLEAR pulse applied to the Model 2738 is distributed to the receiver modules via the Dataway. The action of this pulse is to clear the latches within 100 nsec, making the PCOS III system ready to accept another event.

Trigger Aids - The PCOS III system has been designed to allow it to support most trigger processor systems. This is a feature of the Model 2738 and 2731.

The Model 2731 provides signals which allow the wire chambers to be used both in the fast trigger and in the second level trigger. The PCOS III System also has been designed to be used with fast track recognition circuits.

For first-level trigger applications, the Model 2731 provides up to 16 Prompt OR outputs. These are regenerated ORs of two to thirty-two wire discriminator inputs taken before the Ripplethru delay. Internal wire wrap posts allow the user to pairwise wire-OR the inputs. The Model 2731 provides 16 differential ECL outputs via a front panel header. These may be used for both Prompt and Latched ORs. These outputs are compatible with LeCroy's growing ECLine family of logic units.

For second-level trigger applications, the Model 2731 provides up to 8 Latched OR outputs. Levels are valid, within 50 nsec of the trailing edge of the coincidence gate. Internal wire wrap posts allow the user to configure four-fold to thirty two-fold Latched ORs on the OR output header along with the Prompt ORs.

System Readout

The LeCroy DATABUS System is employed for CAMAC readout of the PCOS III System. Up to 16 dedicated crates can be read out via CAMAC using a single Model 4299 DATABUS Interface located on the data acquisition branch. Dedicated crates of other LeCroy DATABUS Systems may be used along with the PCOS III crates.

The Model 2738 in each dedicated crate rapidly scans the LAM status of the 2731 and encodes the address of clusters of hit wires. Only those containing hits are read. Data are loaded into a memory for subsequent CAMAC readout. Addresses are also presented at a front panel ECLport, allowing the data to be transmitted to a trigger processor for track analysis.

The Model 2738 performs the readout and encoding of the hit wires. The unit compacts the data by encoding up to 15 adjacent hits as a cluster. If clusters of more than 15 adjacent hits are encountered, they are treated as multiple clusters. The ECLport Wire In/Out on the Model 2738 allows multiple crates to be cascaded. The ECLport allows the data to be transmitted to a high speed data handler, such as trigger processor or a fast readout system.

The four NIM signals E1, E2, E3, and E4 and Clear Signal received by the Model 2738 are restandardized and transmitted to the 2731 modules via the Dataway. They are normally used as Coincidence Gate and Test signals, however they have been given generalized names as other forms of receiver modules are planned for the future. The trailing edge of E1 activates the readout sequence. E2 could be used as the coincidence gate for the receiver modules while E1 starts the encoding cycle. The modules containing hit wires request readout via the L lines within the CAMAC crate. The Model 2738 can scan the LAM status of all modules in 100 nsec. Readout of hit modules is then performed under control of the Model 2738 at a readout rate of 100 nsec per module. Thirty-two bits are transmitted to the processor at once. The Model 2738 is double-buffered, allowing a second module to be read immediately while data from the first module are being processed by a fast priority encoder. The addresses of hit wires are generated at the rate of 100

nsec per cycle. Because of the double-buffering, hit addresses are generated at 10 megawords per second. Owing to the bus structure of the ECL port system, 100 nsec is required to skip each crate containing no hits.

The time between the trailing edge of E1 and the first hit word transmitted to the ECLport of Crate 1 is 400 nsec. Each of the successive hits presented requires an additional 100 nsec. An additional 100 nsec is introduced into the datastream for each empty crate after Crate 1. If the clusterized data is sent to the ECLport, it is valid 200 nsec after the last hit of the cluster (i.e. the first cluster is presented 600 nsec after the gate). Two words (width and centroid respectively) are presented sequentially, separated by 100 nsec. DATA RDY indicates the presence of valid data in all cases.

The Model 2738 contains a look-up memory to allow the user to assign logical addresses to the modules within the PCOS III crates. This system offers several advantages:

1. The readout format can be tailored to the experiment. For example, the system wire address scheme can be assigned to match the scheme used for a Monte Carlo simulation.

2. Wire addresses of a system using one crate for two or more wire planes can be assigned to eliminate the possibility of confusing the cluster/centroid calculator by events at the boundary.

3. Wire addresses of a chamber which requires more than one crate of PCOS III circuitry can be numbered sequentially over crate boundaries.

The encoded 14-bit addresses of hit wires (logical module address and wire subaddress) are transmitted to a cluster scanner as they are encoded. When activated, the circuit identifies clusters, two or more contiguous hit wires. Two 16-bit words define the cluster. The first contains the 4-bit cluster width and a flag bit to identify it as a cluster word. The second contains the logical address of the cluster centroid. It consists of the 14-bit logical address of the cluster centroid as well as an additional half wire bit set to 1 if the cluster width is even and to 0 if the width is odd.

The Wire In/Out ECLport allows the internal 16-bit digital databus of the Model 2738 to be extended external to the controller. See Figure 5. Multiple crates of PCOS III may therefore be cascaded by connecting their ECLports. A control-daisy chain arbitrates with priorities determined by the position on the bus. Upon receipt of an E1 pulse encoding of all crates begins in parallel. After the LAMs are processed and the first module read is performed, the highest priority 2738 module takes control of the ECL bus, transferring data to the cluster compacters. After the first crate is entirely read, the second crate follows. Because all the 2738 modules perform their first read in parallel, encoded data from the second crate follow as soon as control of the ECL bus is transferred.

The Cluster/Centroid calculator of the highest priority Model 2738 receives the encoded logical addresses of all hit wires. As a result, the cluster-compacted data can be presented at the ECLport of the 2738 module and loaded into its 1K X 16-bit 2738 memory.

Conventional communication with the PCOS III crates is made via the LeCroy DATABUS. It allows the compacted, formatted data to be automatically transferred from the memory in the Model 2738 to the Model 4299 and then to the attendant computer by CAMAC readout. Data may also be written into the Model 2738 from the DATABUS accepting the logical addresses of the 23 modules it controls and the readout options. In addition, CAMAC commands are transmitted to the 2731 modules via the 2738 to set threshold and delay settings as well as the Test Pattern.

Interface to a Trigger Processor

Hit wire or cluster data from a PCOS III crate can be presented at the ECLports of each 2738 module. Data are 16-bit differential ECL with a Data Ready strobe. The addresses are presented as they are calculated, affording highest speed operation of the track recognition logic and eliminating the speed limitations of conventional CAMAC readout.

An unconditional transfer or double handshake scheme can be selected for the ECLport System allowing the readout to be controlled by the user. Data and strobe are presented at the ECLports at a rate determined by the internal scan rate of the PCOS III System. For unconditional transfer, cable delay due to extended bussing will cause the output data-stream to be displaced in time but will not have any effect on the readout rate. This configuration, along with the operational characteristics afforded by the PCOS III receiver modules makes feasible the remote operation of the system.

PCOS III can accomodate wire chambers which have more wires than can be processed by one CAMAC crate of PCOS III receiver modules. Multiple crates can be daisy-chained via the ECLports. The master 2738 receives logical hit wire addresses from all crates which are daisy-chained via their ECLports. It processes the data, identifies clusters, and presents them at its ECLport.

1.1.3 Additional Information

1.1.3.1 E1, E2, E3, E4, and CLEAR inputs at the front panel:

These inputs are translated to differential ECL levels and transmitted over the CAMAC dataway to the Receiver Modules in the crate. The Receiver Module in CAMAC Station 1 must contain the 120 Ω terminations for these lines. See the data sheet for details. All other receiver modules in the crate must have their terminations removed before installing them in the crate.

The propagation delay of these control signals to the receiver modules in the crate is included in the calibration of the

receiver modules where appropriate. For example, the delay in the 2731 modules is calibrated assuming a particular delay between the E1 input of the 2738 and its arrival time at the flip-flops in the 2731.

The propagation delay of these control signals to the end of the CAMAC dataway is 7 nsec $\pm$ 2 nsec. This delay depends on the type of crate and the number of modules in the crate.

1.1.3.2 INH Encode Input at the front panel:

If this input is ON before the end of E1, the encode cycle will be inhibited until this input returns to the OFF state. A CLEAR asserted during this time will clear the 2738 encoder section and all Receiver Modules. The INH Encode input does not inhibit the Receiver Modules.

1.1.3.3 BUSY Encode Outputs at the Front Panel:

The encoding section of the 2738 becomes busy approximately 100 nsec after the end of E1 unless INH Encode is ON. In that case, the encoder becomes busy approximately 10 nsec after INH Encode returns to the OFF state. Busy Encode is ON until the entire crate or crates connected via ECLports have been encoded. At that time BUSY Encode returns to the OFF state and the DATABUS communication section of the 2738 is notified that all the data is stored internally in the 1k x 16 buffer memory.

While the 2738 communicates with the DATABUS Interface, BUSY Encode is not ON. The DATABUS Interface busy line is ON during the communication between the 2738 and the DATABUS interface. The DATABUS Interface will indicate this at its front panel BUSY output.

The BUSY Encode outputs can be daisy chained to other controllers so a system busy can be generated. The system busy would be an OR of all the BUSY Encodes. Readout is enabled when the external BUSY returns to ground.

1.1.3.4 User Option Switches at the Side Panel:

Figure P.1.1.1 contains a drawing of the option switch and the switch labels. Switches 1 thru 4 are the address switches for the 2738 controller. Each controller on the same DATABUS must have a unique address. Up to 16 controllers may be used. Other LeCroy DATABUS systems may be mixed with PCOS III.

LAM Request, switch number 5, enables the 2738 to generate a LAM after its data has been transferred to the DATABUS Interface.

DATABUS control, switch number 6, determines whether data are to be automatically transferred to the DATABUS Interface. Data are always loaded into the buffer memory and presented at the ECLport out connector. If the data is not automatically sent to the DATABUS Interface, it can still be transferred by using the reread command described in 1.1.3.6.

TERMINAL and MASTER, switch numbers 7 and 8, tell the encode section of the 2738 where the controller is located in the ECLport daisy chain. The status of these two switches are indicated by front panel LEDs. If there is no ECLport daisy chain, both MASTER and TERMINAL LEDS must be on. When several controllers are connected via their ECLports, the controller with its ECLport out connector not in the chain is the master controller. The controller with its ECLport IN connector not in the chain is the Terminal controller. The master controller should have only its MASTER LED on and the terminal controller should have only its TERMINAL LED on. All other controllers in the daisy chain (up to 16 total) should have their MASTER and TERMINAL LEDS off. The master controller will read encoded data from the other controllers on the daisy chain. The master controller can then clusterize data across crate boundaries if a chamber exceeds 736 wires. Figure P.1.3.2. illustrates a typical system with daisy chained controllers.

Figure P.1.1.2 illustrates part of the data flow in the 2738. Switches 9 and 10 control the data source for the ECLport Out connector and the clusterize mode of the data pipeline. The data pipeline contains three clocked registers which introduce a 300 nsec delay in the data path. The 1k x 16 bit buffer memory always receives its data from the output of the data pipeline. Switch 10 selects the Clusterize Mode or Pass Mode of the data pipeline. The memory can receive clusterized data while the ECLport is supplying non-clusterized data for use by a trigger processor.

1.1.3.5 ECLport Inputs and Outputs:

The DATA RDY output indicates the presence of valid ECL data at the ECLport Out connector. Figure P.1.1.3 shows the timing relationship between DATA RDY, ECL data, and DATA ACK. In a) DATA ACK is not used so new data appears every 100 nsec. An external memory or trigger processor must be able to accept data at this 10 MHz rate. If clusterized data is selected for the port, there will be gaps in the DATA RDY and data while the clusters are calculated, (see b of Figure 1.1.3). In the clusterize mode the centroid of a cluster is preceeded by its width. The width word is identified by bit 15 being on. If there is only a single wire hit the width is not generated.

User devices that cannot operate at 10 MHz can use DATA

ACK to request each word from the 2738. There is a timing restriction for the time at zero volts. The input should be at zero volts for less than 50 nsec to ensure only one DATA RDY is generated for every DATA ACK. The maximum transfer rate using this handshake scheme is 5 MHz. This Timing is shown in c) of Figure P.1.1.3. Data transfer to the DATABUS Interface will not begin until after all the data has been presented at the ECLport.

The ECLport Out connector conforms to the ECLine standard described in the LeCroy ECLine application note. A copy is provided in the Appendix.

1.1.3.6 2738 Commands via the DATABUS:

Wire Inhibit sets the value of I. If a command does not maintain the current value of I then the state of wire inhibit will change.

Assign Logical Address loads an internal 23 x 9-bit memory in the 2738 with a 9-bit logical address to be assigned to all data received from a particular slot in the crate. The slot number is the address of the 9-bit logical address to be assigned to that slot.

Module Write loads any of 8 registers in any slot in the crate with an 8-bit value. Used to set delay, threshold, and pattern registers in the 2731 Receiver Modules for example.

Reread causes the 2738 to transfer the data in the 1k x 16 buffer memory to the DATABUS Interface. This command is useful when auto transfer of the buffer to the interface has been disabled by the DATABUS Control switch.

Master Reset is a DATABUS Interface command that clears all registers in the 2738 and generates a CLEAR on the CAMAC Dataway. This command should be used to initialize the 2738.

1.1.3.7 Output Format:

The data format as seen by the DATABUS Interface is shown on the data sheet. The format presented at the ECLport Out connector differs only in the absence of the delimiter word.

Each wire in the PCOS III system can be assigned a unique 14-bit address. In the clusterize mode an even number of wires in a cluster would have a centroid between two wires. That centroid would have an odd 14-bit address i.e., half way between two even addresses. This odd address is accomplished by adding a 15th half-wire bit.

The most significant two bits denote the three types of data

words presented to memory or the ECLport.

Width	10
Address	0X
Delimiter	11

where X is don't care. The delimiter does not appear at the ECLport. A hardware processor could scan for Addresses only by looking for MSB = 0.

In the clusterize mode a single wire appears only as an address. A single wire has a "width" of one so it does not need an associated width word.

1.2 Installation

1.2.1 Inspection

Upon receipt of the 2738 it is recommended that a careful inspection be performed to insure that no damage occurred during transit.

The shipping box has been custom designed for this unit and should be saved should shipping be necessary.

After removal from the box, the unit should be examined for physical damage to the front panel, rails, or rear connector.

1.2.2 Power Requirements

The 2738 uses +6 V and -6 V in a standard CAMAC crate configuration. The +6 V requires 32 watts and the -6 V requires 6 watts. The power is distributed roughly equally between slots 24 and 25 in the CAMAC crate.

1.2.3 Cable Requirements

The 2738 requires two types of flat cable for system interconnection. Standard ECLine 17-pair twisted pair and 25 pair flat ribbon cable. See figures P.1.2.1 and P.1.2.2.

These cables are optionally supplied with the system as per user requested length specifications.

Connectors and cable are available through LeCroy or directly from the manufacturers listed (as well as many others).

Connector for Flat Cable/PC 34-POS for cable w/.050 CTRS -	LRS # 403-250-034 3-M # 3402-0000T
Connector for Flat Cable/PC 50-pos for cable w/.050 ctrs -	LRS # 403-250-050 3-M # 3426-0000
Flat Cable - 50-Cond	LRS # 592-011-050

.050 ctrs/color-coded/AWG 28/PVC -	3-M # 3302/50
Assembled Cable	LRS # DAT-DI/50-LL
Flat Cable 17 twisted pairs Twist 'N' Flat/AWG 28/PVC -	LRS # 592-120-034 Spectra - Strip 455-248-34
Assembled Cable	LRS # DC2/34

Contact your local LeCroy Representative for complete cable ordering information.

1.3 Operating Instructions

1.3.1 Initial Checkout

A set of scenarios is given which illustrate all of the basic DATABUS based features of the system and gives a new user a "canned" procedure which will allow immediate use of the system.

1.3.1.1 Setting up a System (Mechanically): Begin with a DATABUS Interface which is placed in a standard CAMAC crate. Set side panel switches to: SBR, DOP, and COP off; RWC on; CLEAR to DRC. Also check that the read and write patch pins are set to F(16), F(0) respectively, see 4299 SPEC SHEET or figure P.1.3.1.

In a dedicated CAMAC crate place a 2738 in slots 24 and 25. Make sure that the side panel switches are set as follows:

1. Set Controller address to - #1 open; #2, #3, #4 closed.
2. Disable LAM - #5 closed.
3. Enable Automatic Readout - #6 closed.
4. Set TERMINAL - #7 closed.
5. Set MASTER - #8 closed.
6. Set ECLport source before pipeline #9 closed.
7. Set PIPELINE in pass mode #10 closed.

Place one or more 2731's in the remaining CAMAC slots of the dedicated crate. Only the 2731 in slot number one should contain line terminators for the CAMAC Dataway. See the 2731 Data Sheet for location.

Connect the 50 wire 4299 interface cable from the 4299 to the top DATABUS port of the 2738. The cable should connect pin 1 of the 4299 with pin 1 of the 2738.

1.3.1.2 Using the System (Software)

NOTE 1: As you read the following series of commands, notice that a modular approach to your software will be found appropriate in carrying out the required commands. This is especially true in Assigning Logical Addresses and in setting thresholds, delays and test patterns.

NOTE 2: The notation (F, A, W(orR)) will be used to describe a CAMAC command where appropriate. F and A are decimal numbers and W(orR) is a bit string of 16-bits (unless all are zero then ∅ will be used). These bits would be transmitted on the CAMAC write (read) lines. All CAMAC commands go to the 4299.

Scenario 1 - READ OUT SYSTEM CHECK, USING E3 and PATTERN REGISTER.

(1) SEND: (9, 0, 0). This command initializes the 2738 and the 4299. It also clears the 4299 memory and generates a Q and X response. Termed "MASTER RESET".

(2) SET Logical Addresses

SEND: three CAMAC commands 23 times as defined below.

		Notes:
(16,0,0XAAAAXXXXXXX001X)	-	(defines command)
(16,0,1XXXXXXXSSSSSSSS)	-	(data)
(16,0,1XXXXXXXNNNNNXX0)	-	(data)

Where: AAAA equals 0001 to define controller one as the receiver.

SSSSSSSS (8 bits) should be incremented from 1 to 23 thereby assigning the crate slot number as the logical address.

NNNNN (5 bits) should be incremented from 1 to 23 to select each slot. (i.e. NNNNN = SSSSSSSS).

Note that 9 bits are available for logical addresses. The final zero in the third word is the most significant bit. (SEE SPEC. SHEET).

(3) Transmit a TEST PATTERN

SEND: three CAMAC commands 23 times as defined below.

Notes:

(16,0,0XAAAAXXXXX0010X) - (command word)

(16,0,1XXXXXXXVVVVVVVV) - (data)

(16,0,0XXXXXXXNNNNNRRR) - (data)

Where: AAAA = 00001 to denote crate 1

VVVVVVVV = 10000000 (8-bits) to set bit 15 in each pattern register of the 2731 module .

NNNNN should be incremented from 1 to 23 (5-bits) to set the pattern register in all 23 modules. If 23 modules are not plugged in, the extra commands will be ignored.

RRR = 011

Then SEND: 3 more sets of 23 with

VVVVVVVV = 00000000 (8 zeros)

RRR changes to 010, then 100, and then 101 for each set of 23

This zeros all of the remaining test bits.

After this step the system has been set up to return one test data bit from each module (bit 15).

(4). Inhibit the inputs to the 2731's.

SEND: (16,0,0X0001XXXXX0100X)

(5) SEND: one 1 μsec. pulse to E1 and E3 simultaneously.

(6) READ 4299 memory

SEND: (11, 1, 0) This initializes 4299 memory address counter for a new readout cycle.

SEND: (0, 1, R) This command generates a Q response if valid data is present to be read out. Continue sending this command until Q goes away and store the 16 bit R's returned.

(7) Print out the R's in binary.

The result:

	Binary	Integer
Number of words:	0000000000011000	24
DATA:	0000000001011110	94
DATA:	0000000010011110	158
DATA:	0000000011011110	222
	.	
	.	
	.	
DATA:	0000010111011110	1502
DELIMITER:	1100010000000000	-15360

The DATA format is 0SSSSSSSSSWWWWW0 where the most significant bit is on the left. W is the pattern register address (i.e. the channel tested in the respective module) and S is the assigned logical address. Note that S ranges from 1 to 23 and W is a constant at 15. The final word is the delimiter which contains the controller address in bits 11 to 14.

Scenario 2 - DELAY CHECKOUT (Assumes pattern register set as in Scenario 1).

(1) SEND: three CAMAC commands as defined below.

		Notes:
(16,0,0XAAAAXXXXX0110X)	-	(defines command)
(16,0,1XXXXXXXVVVVVVVV)	-	(data)
(16,0,1XXXXXXXNNNNN000)	-	(data)

Where: AAAA = 0001 to denote controller 1

VVVVVVVV = 00000000

NNNNN = the slot number in which the 2731 to be examined is present.

(2) Examine the delay set by pulsing the E3 line of the 2738 at about 1Khz and observe the E3 input and the DELAY output simultaneously on an oscilloscope. Set the oscilloscope vertical channel to .05 volts/div and 50 Ω to see the delayed pulse. V = 0 implies the minimum delay of approximately 300 nsec.

(3) Repeat step (1) with V = 11111111 (all eight bits 1)

(4) Repeat step (2) the delay should now be approximately 682.5 nsec.

(5) This scenario merely shows how to change the delay it is not an accurate measure of the actual delay. See 2731 Technical Specifications. The DELAY output only gives a rough measure of where the delayed pulse is located relative to the signal.

Scenario 3 threshold checkout

(1) SEND: three CAMAC commands as defined below:

		Notes:
(16,0,0X0001XXXXX0010X)	-	(defines command)
(16,0,1XXXXXXXVVVVVVVV)	-	(data)
(16,0,1XXXXXXXNNNNN001)	-	(data)

Where: VVVVVVVV = 00000000

NNNNN= the slot number in which the 2731 to be examined is present.

(2) Examine the threshold pin (THR) on the 2731 front panel it will read 0 volts.

(3) Repeat step (1) with V = 11111111 (all eight bits on).

(4) Examine THR, it will read 7.65 volts.

1.3.2 System Assembly

There are many configurations available when using the PCOS III system. Two possibilities are illustrated in figures P.1.3.2 and P.1.3.3.

Figure P.1.3.2 shows a system with 3 (or more) chambers of less than 736 wires. The 2738 crates are daisy chained from the 4299 via the LeCroy DATABUS. One 4299 can provide control signals for up to 16 dedicated crates. The figure shows all of the crates with both the MASTER and TERMINAL LED's lit. This indicates that each crate is independent and will in turn take control of the DATABUS and read out when it is enabled. Enabling can be either automatic or by computer control after a fast processor decision. A fast trigger processor connection is shown from the ECLport out of each crate. The signals at this level are wire logical addresses or clusterized addresses.

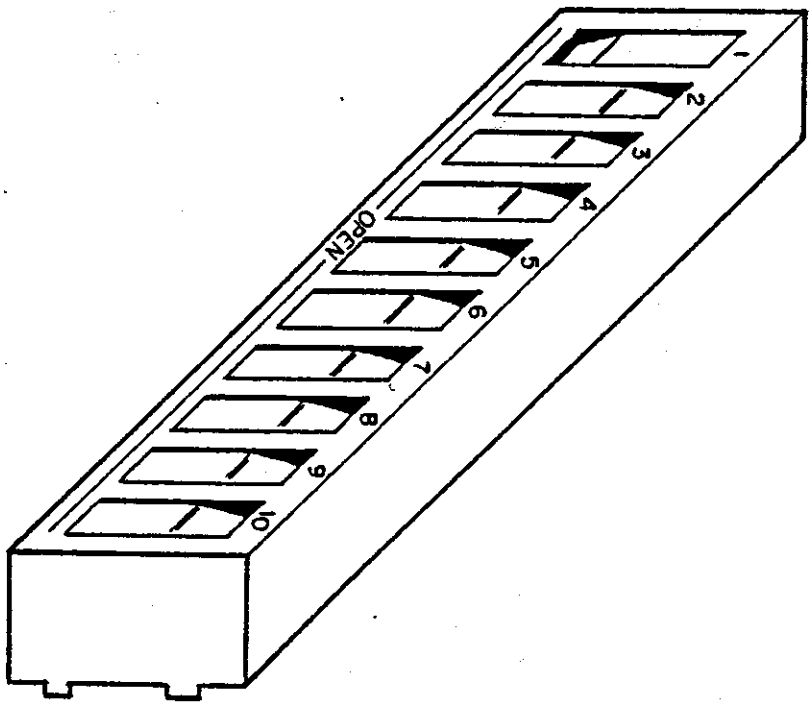
The receiver modules are shown connected to the chamber cards via twisted pair flat cable. Threshold control passes to the chamber cards via these cables. Lower level unprocessed data can be sent to fast

processors from the receiver modules, either latched after the delay or unlatched prior to the delay (See receiver module Technical Specifications for possible configurations).

Each crate can be set up via software commands to readout the wire chambers using unique logical addresses to designate each receiver module. In this way, if two chambers are in the same crate a gap can be left in the addressing between the two chambers. This gap would allow the controller to clusterize hits from the two chambers independently.

Figure P.1.3.3 shows a system with one large chamber where the ECL ports are daisy chained and the MASTER and TERMINAL LED's are lit as shown. Daisy chaining the controllers allows the MASTER controller to clusterize across crate boundaries using contiguous assigned logical addresses. Note that only one ECLport out goes to the trigger processor, this can be done, even if clusterizing is not done, so that the whole chamber can be presented at one ECLport. Only the Master controller will take control the DATABUS for readout. Note that if over 1000 hits are received, data will be lost in the 2738 buffer memory.

Figure P.1.3.4 shows a schematic of the 2738 front panel detailed descriptions of these outputs are given in sections 1.1.2 and 1.1.3. In configuring a system these outputs may be used in various ways starting at the top DATA ACK and DATA RDY go to the trigger processor to control the ECLport. E1 and E2 are connected to the system trigger logic. E2 would be used if two chambers readout from the same crate and one chamber has a larger drift time or jitter than the other chamber requiring a different gate width. The gate that controls a receiver module is set in each receiver module. E3 and E4 are available so that the system can be automatically tested (for timing the system etc.) from the receiver modules upward. Note that only 1023 hits can be readout at one time due to the 2738 buffer memory. If two crates are daisy chained as in figure P.1.3.3 no more than a 1023 hits may be tested at one time. The two test inputs in conjunction with the Pattern Register would have to be used to properly configure a test. INH ENCODE can be used to prevent any new gates from being processed until the users data processor is ready to accept new data. BUSY could be connected to user control logic to indicate that the controller is busy encoding data. This input is set up to allow daisy-chaining from one controller to another producing an OR of all controller BUSY's. CLEAR is used to clear the receiver modules and the encoding section of the 2738. RESET serves the same function as CLEAR and in addition clears the readout section of the 2738. Using CLEAR instead of RESET allows the 2738 to finish reading out an acceptable event while preparing for and then accepting a new event. Neither CLEAR nor RESET are necessary for normal readout of the crates. CLEAR is used if the current Encoding cycle is to be aborted due to a trigger processor decision and RESET is used if the DATABUS readout cycle is to be terminated due to a trigger processor decision.



OPTIONS SWITCH

4, 3, 2, 1		Controller address
M	L	Closed = "0"
S	S	
B	B	Open = "1"

5 LAM Request
Closed = LAM Disabled

6 DATABUS Control
Closed = Auto Transfer to DATABUS Interface

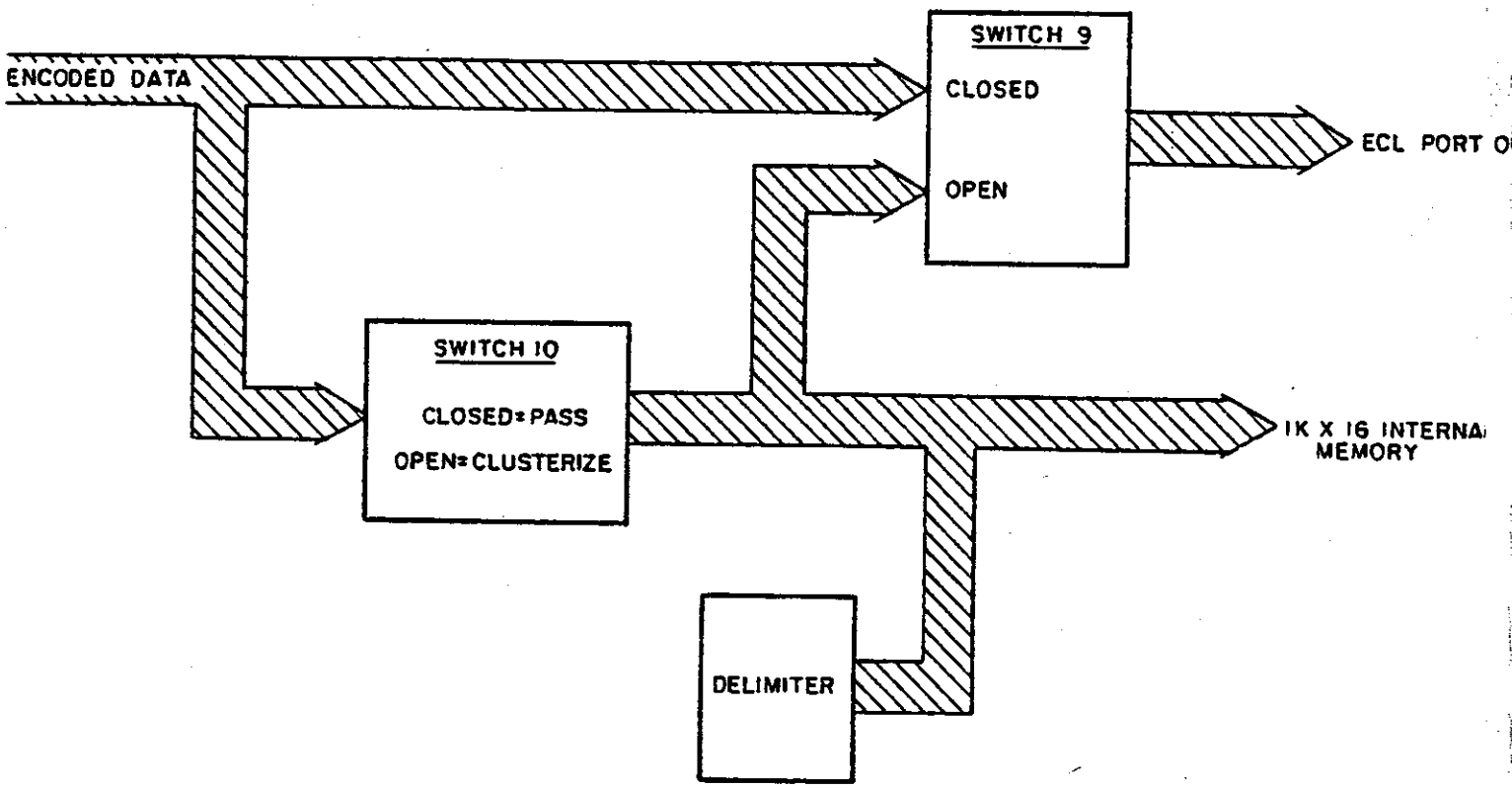
7 Terminal
Closed = Terminal controller

8 Master
Closed = Master controller

9 ECLport source
Closed = before data pipeline
Open = after data pipeline

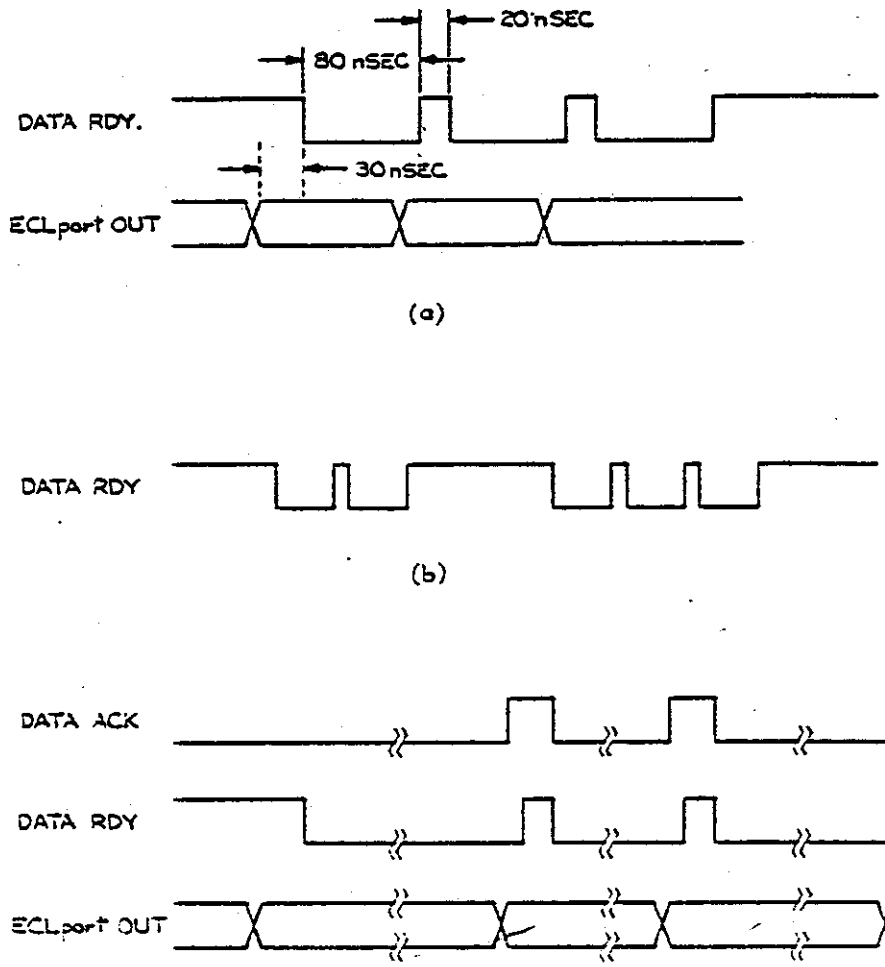
10 Data pipeline Mode
Closed = pass encoded data
Open = clusterize data

Figure P.1.1.1



ECLport DATA PATH CONTROL

Figure P.1.1.2



TIMING DIAGRAM FOR ECL port CONTROL

Figure P.1.1.3

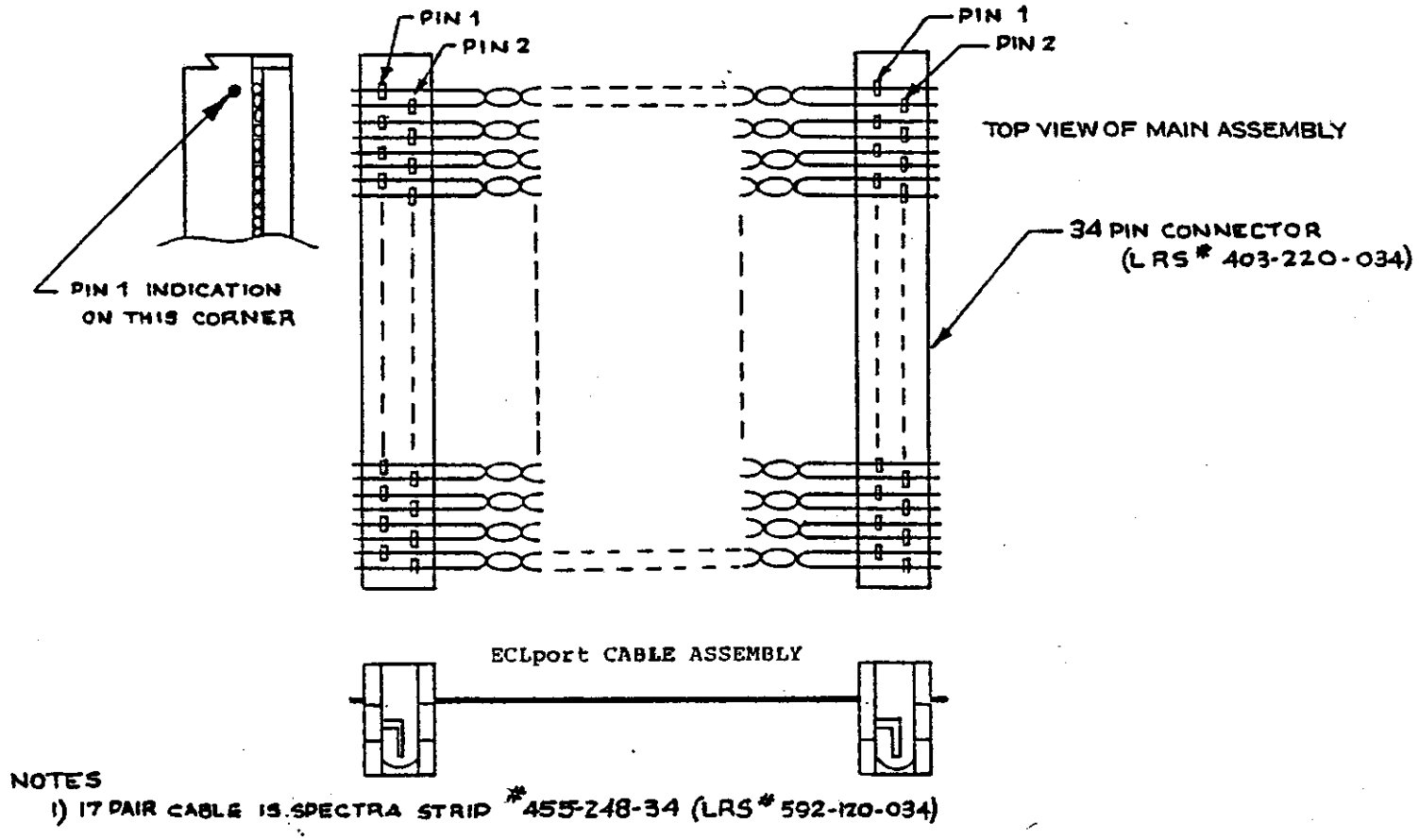
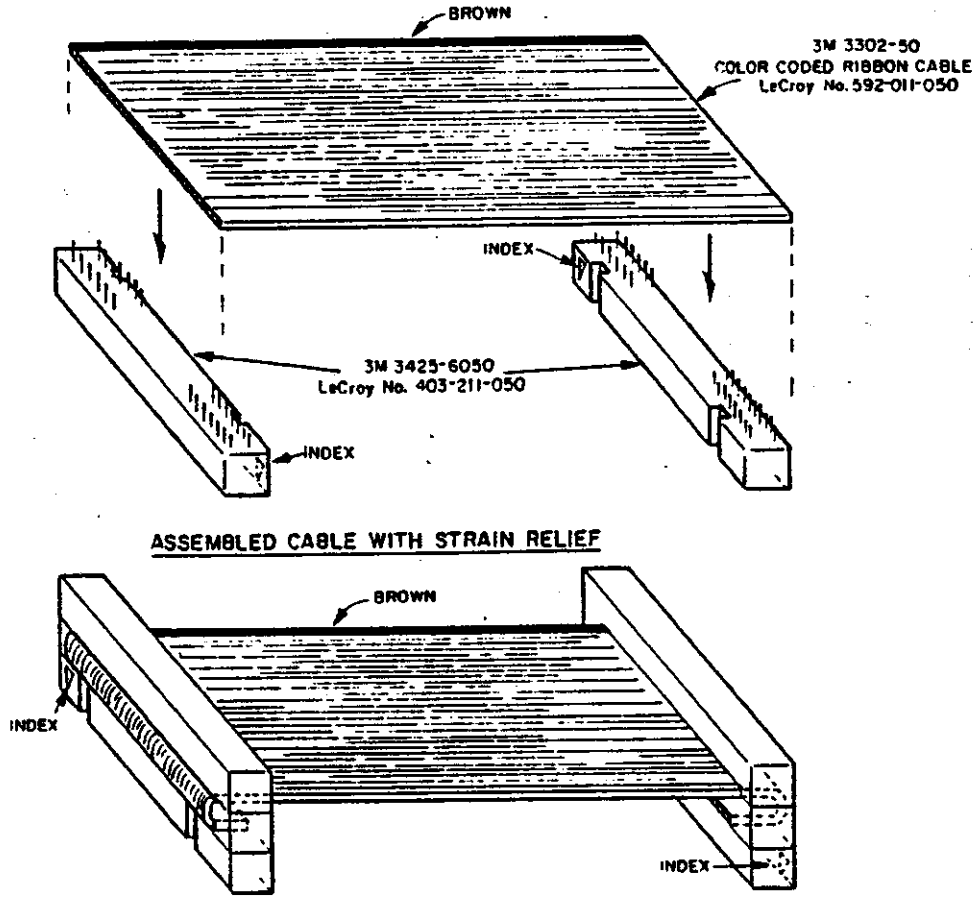

PIN 1
PIN 2
PIN 1
PIN 2
TOP VIEW OF MAIN ASSEMBLY
34 PIN CONNECTOR
(LRS # 403-220-034)
PIN 1 INDICATION
ON THIS CORNER
ECLport CABLE ASSEMBLY
NOTES
1) 17 PAIR CABLE IS SPECTRA STRIP #455-248-34 (LRS # 592-120-034)

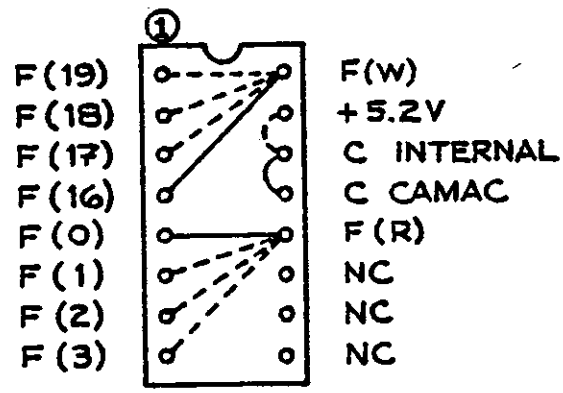
Figure P.1.2.1



DAT-DI/50-LL

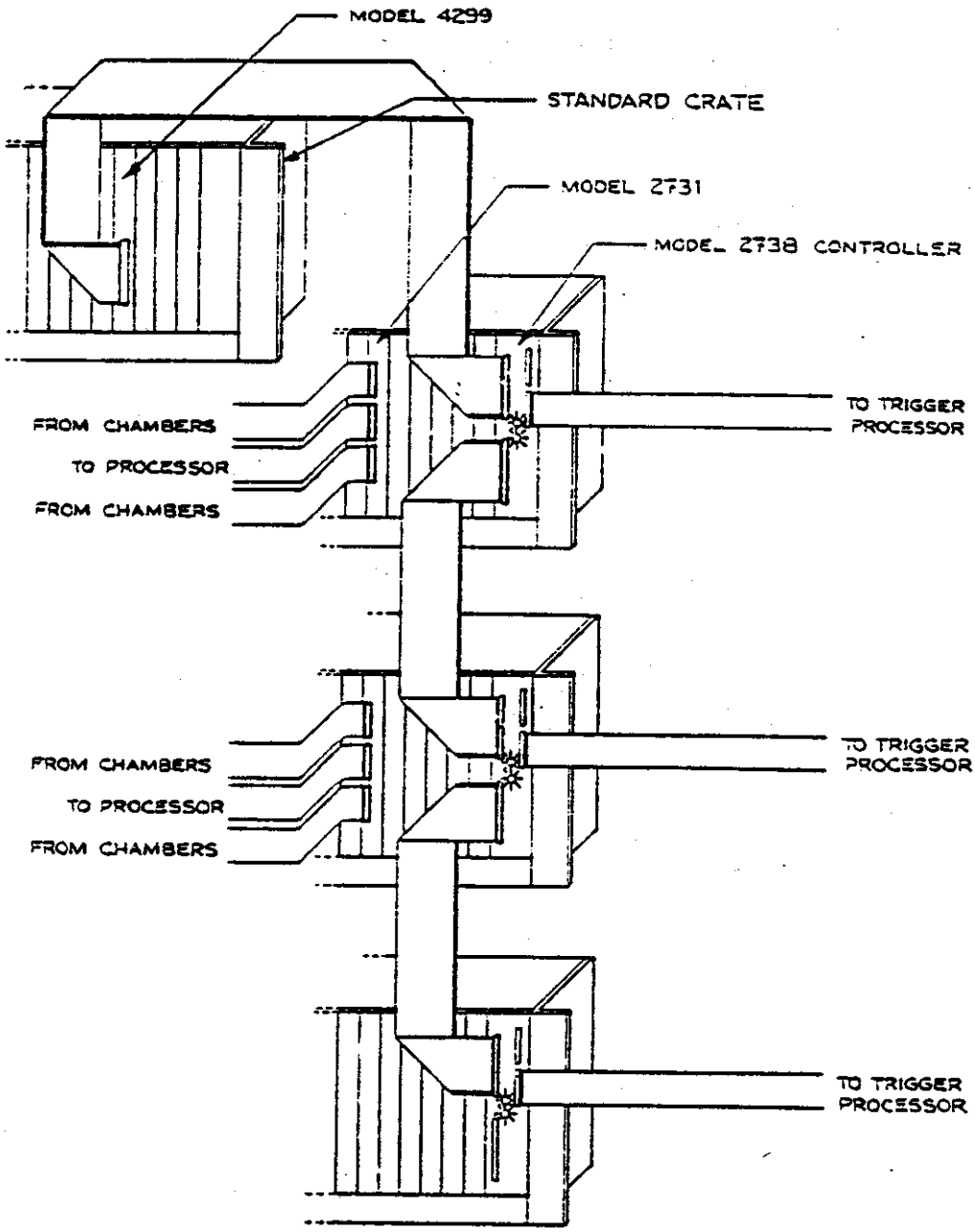
DATABUS CABLE ASSEMBLY

Figure P.1.2.2



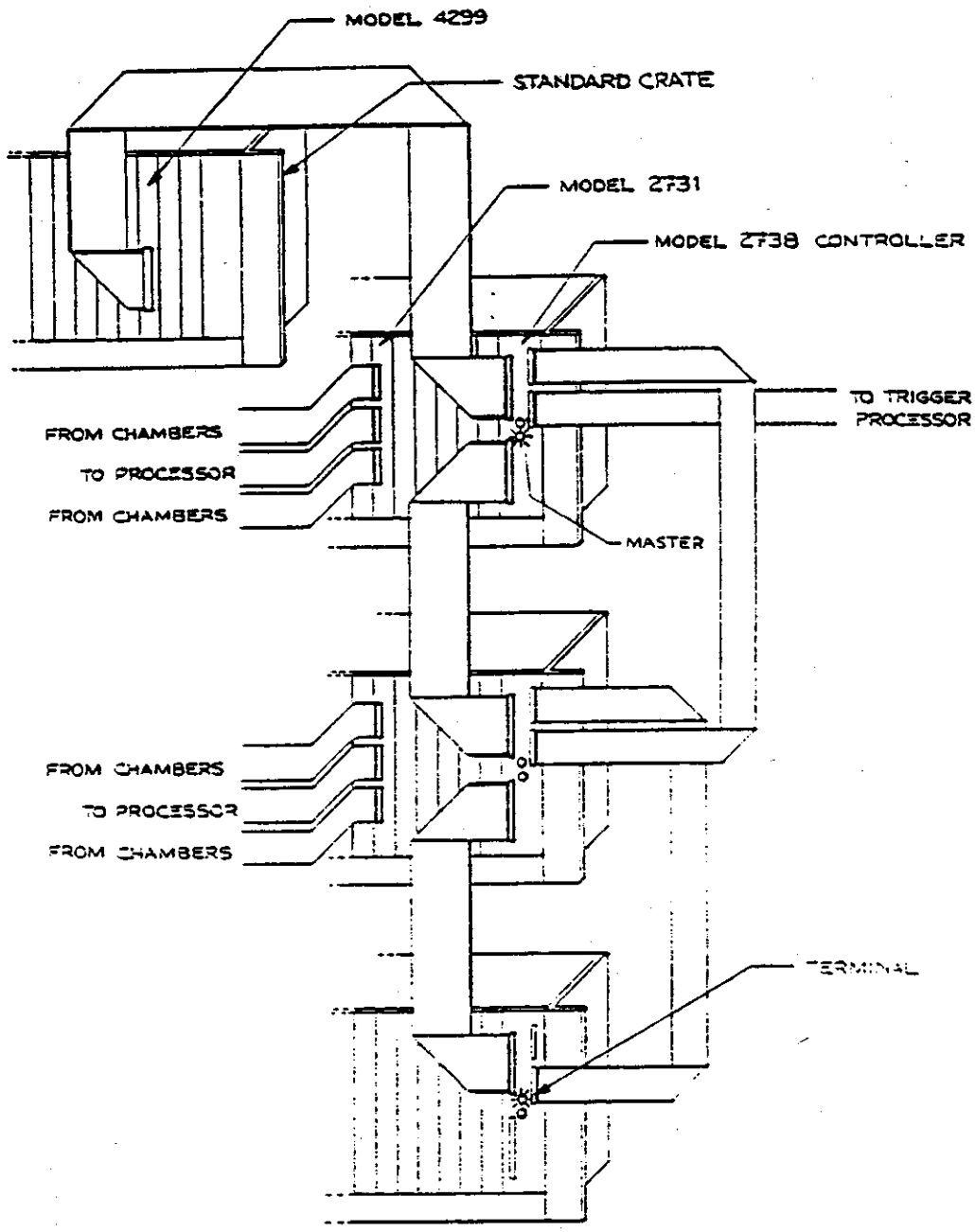
4299 JUMPER PLACEMENT

Figure P.1.3.1



STANDARD SYSTEM CONFIGURATION

Figure P.1.3.2



SYSTEM CONFIGURATION WITH ECLport DAISY CHAIN

Figure P.1.3.3

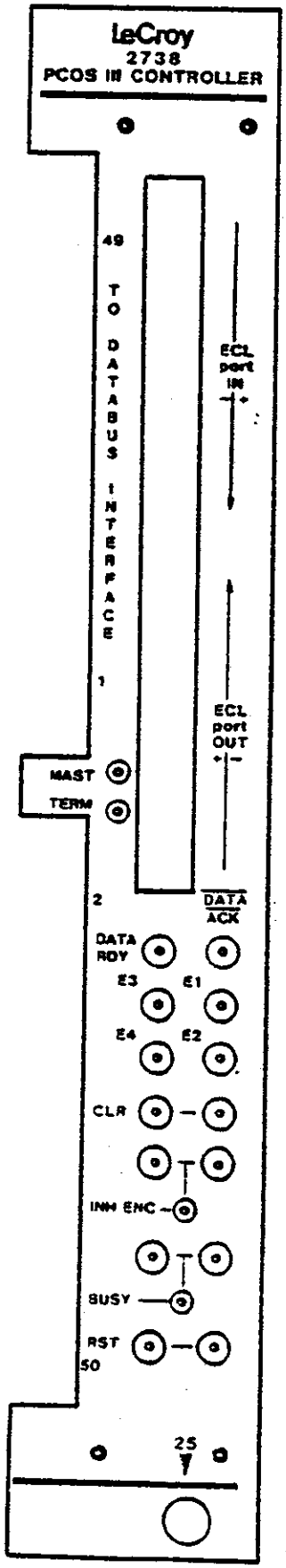


Figure P.1.3.4

FRONT PANEL LAYOUT

SECTION 2

TECHNICAL DESCRIPTION

2.1. DATABUS Control

Figure P.2.1.1 refers to the DATABUS control section of the 2738. The following paragraphs will expand on the blocks in the block diagram.

The LeCroy databus is based on the EIA RS422 standard for a balanced voltage digital interface over 100 Ω lines. Twenty-five wire pairs are defined as shown in Figure P.2.1.2. There are 16-pairs of DATA transceiver lines, 8-pairs of control lines and two ground lines. The destinations of signals on the control lines are also shown in the figure. The DATABUS can be run unterminated; assuming that only short distances (less than 30 meters) will be considered. The GRANT line is terminated in each 2738 and then passed back onto the DATABUS under proper conditions, described below. All other lines are picked off at each controller and daisy-chained to the next controller with no break in continuity.

The COMMAND DECODER is the most straight-forward place to begin describing operation. A command on the DATABUS Address is set in bits 10 to 13. If the READ and INH lines are not asserted, the BUSY $\overline{\text{ENCODE}}$ is not true and the Address bits match those of the controller; the command will be acted upon 100 ns after ISYNC is received. The DATA bits 1 to 4 denote which command occurred. A command is shown in Figure P.2.1.3 using positive logic. (The DATABUS is a tri-state balanced line device and therefore positive logic will be used throughout when showing time to minimize complication). The commands are stored in D-flops which reset appropriately whenever a command is received or a MASTER RESET is asserted on the DATABUS. A MASTER RESET occurs when both READ and INH are asserted simultaneously. The controller sends the MASTER RESET out to the receiver modules on A8 and I in coincidence.

Every command sent by the 4299 is accompanied by an ISYNC as mentioned above. This ISYNC initiates a CSYNC which the 2738 must generate within 25 μsec after the ISYNC was sent. If the full 25 μsec elapses the 4299 will automatically consider the function executed and reset itself. This hand shake must be taken into account in high speed uses of the 4299. Figure 2.1.4 shows the ISYNC-CSYNC timing for all of the various commands.

There are four commands INH WIRE (IW), REREAD (RR), ASSIGN LOGICAL ADDRESS (ALA) and MODULE WRITE (MW). IW and RR are one word commands while MW and ALA require three words. See section 1.1.2 for formats.

IW sets a D-flop which sets the F4 line to +6 volts (minus a diode drop). This changes the bias on the input level translator transistors in the receiver modules; thereby turning the inputs off.

RR sets a D-flop which sets a J-input high on a flip-flop and starts a readout cycle when the trailing edge of the CSYNC (which the control section returns to the 4299 to acknowledge receiving the RR command) clocks the flip-flop.

ALA and MW require the use of the COMMAND DATA ROUTER since more than 16-bits of control information must be sent to the 2738. ALA and MW each send a first word with MSB 0 denoting a command. Then two more words are sent with MSB one. The least significant 8 bits of each of these words are stored in 2 octal D-flops to construct a 16-bit word which determines the MW or ALA operation performed. Figure P.2.1.5 shows what the internal 16-bit words look like. Figure P.2.1.6 shows the timing on the control signals which clock the two data words into the proper D-flop, and it shows the control logic which cues the DATA ROUTER that it should be active. After the ALA or MW is received, the outputs of the octal flip-flops are enabled (FW low, Full Word) and the data is clocked out to the logical address memory or receiver modules respectively.

To check whether MW commands are being sent correctly, the user can check the corresponding lines listed in Figure P.2.1.7. The data is clocked in when N•F1•I is true at the trailing edge of I.

The READOUT CONTROL is intimately intermixed with the DATABUS ARBITRATION section. Figure P.2.1.8 shows the logic levels required on the databus to enable a particular controller to execute a readout cycle, only one controller is on the bus. Once the BUSY is enabled the 4299 cannot take control of the DATABUS. When the GRANT is enabled no 2738 can enable it's REQUEST line. This serves the same function for the 2738's that BUSY performs for the 4299. It is important to note that each 2738 has an INPUT Grant and an OUTPUT GRANT, this is the only DATABUS line which is not continuous. The REQUEST ENABLE (REQ EN) line gates the GRANT OUTPUT. Figure P.2.1.9 shows a more complicated DATABUS arbiration. GRTn where n is 0, 1, 2 etc. is used to designate the source of the output GRANT i.e., 0 is the 4299, 1 is the 1st controller on the DATABUS, 2 is the second etc. Similarly REQN is REQUEST for the nth controller. The Scenario illustrated shows controller's 1 and 2 enabling their REQUEST lines at the same instant. The 4299 only knows that the REQUEST is on and responds with a GRANT. Controller 1, however, doesn't pass the GRANT so controller 2 does not read out till controller 1 disables REQ1. Controller 1 cannot start another external REQUEST until GRT0 is disabled. Shown pictorially in Figure P.2.1.10, REQI is the internal request signal. REQ INH is true whenever BUSY ENCODE is asserted by any Controller connected in the same BUSY ENCODE daisy chain. When REQ INH is true the Controller cannot produce a REQUEST. Therefore the BUSY ENCODE daisy chain can be used to prevent any controller from reading out till all controllers on the chain have encoded their data. When this is done the controllers automatically readout sequentially along the DATABUS daisy chain.

BUSY EN signals the controller to setup readout. The data output line drivers are enabled (RLD EN); the buffer memory Address counter is zeroed and the readout reset MNY is set to the off state. The buffer

memory was enabled on REQ EN so the data is available immediately when BUSY EN occurs. A CSYNC is sent simultaneous with the time that the buffer memory address counter is zeroed.

Each CSYNC causes an ISYNC to be returned. The DISYNC thereby generated clocks the buffer memory address counter (RMC) and sends a CSYNC. When the event has been readout (A=B line true) the DELIMITER word is enabled onto the DATABUS along with a CSYNC. The ISYNC returned resets the readout cycle (MNY true).

The readout cycle is initiated by a signal from the encoder section (MEM RDY) which is gated by MASTER and The DATABUS ENABLE switch. Or by a REREAD command.

2.2 Encoder and Clusterizer

2.2.1 Data Pipeline

Throughput and low power dissipation were the prime design constraints for this section of the 2738. Low power schottky provided the low power dissipation and pipelined operation ensured high throughput.

Pipelined organization of a function requires that the function can be broken into individual subfunctions that require approximately equal time to evaluate. Each subfunction is a combinatorial stage followed by a staging register. A common clock strobes all staging registers simultaneously. At every clock, new data can be input to the pipeline and processed data appears at the output.

The 2738 pipeline block diagram is shown in Figure P.2.2.1. Six staging registers control the flow of data through the pipeline. Three different gated clocks synchronize the data. Many different combinatorial subfunctions are used between the staging registers. Each stage is represented by a T number. The six stages are summarized the in the following table.

Stage T1: Encodes one of 23 LAM lines into a 5 bit address and latches the address.

Stage T2: Decodes the 5 bit address into one of 23 N lines.
Latches the 32 data bits from the selected slot.
Latches the 9 bit logical address of the selected slot.

Stage T3: Encodes one of 32 data bits into a 5 bit wire address and latches the address.
Latches the external address from the ECLport In connector.
Buffers the address to the ECLport Out connector.

Stage T4: Latches and inverts the 14 bit address.

Stage T4: Latches and inverts the 14 bit address.

Stage T5: Calculates the centroid and width if in clusterize mode. Passes the 14 bit address if in pass mode.
Latches the result in both modes.

Stage T6: Latches the address or width for the memory or ECLport out connector.

Encoder blocks B1 and B8 are almost identical. Sheet 4 of the 2738-2 Schematic contains B6 and B8 blocks. B6 is a 32 bit register composed of U96, U97, U98 and U99. The output of each register drives an 8 bit encoder section. Four of these sections comprise encoder block B8 and three similar sections comprise encoder block B1 on sheet 1 of the 2738-1 schematic.

On sheet 1 of 2738-1 U25, a 74LS259, is an addressable register. This register starts in the clear state with all its outputs low enabling all the negative input NANDs U15 and U16. Therefore, LAMs L1 through L7 are presented to the priority encoder U24. U24 encodes the highest priority LAM generating its address at A0, A1, and A2. This address, multiplexed with the addresses from U22 and U28, appears at the input of U33. This is block B2 in the block diagram. The address also appears at the address input of U25. At the clock the output of U25 corresponding to the address, disables the LAM currently being encoded. On the same clock the address is latched in B2. The next highest priority LAM is then digitized and on the next clock it is also disabled, thus, on every clock a new LAM is encoded. The 8 input ORs U31, U30, and U29 enable the next encoder section, finally generating an EMPTY signal when all active LAMs have been encoded and the crate is empty of data.

Encoder block B8 (schematic on sheet 4 of 2738-2) consists of four 8 Bit encoder sections. In addition a set of 32 diodes and 32 resistors form an analog sum of the data bits that are on. When there is one more bit out of the 32 to be encoded, the output of U95 goes high causing the 32 data bits from the next slot to be latched in block B6. The signal from U95 is called LAST WIRE and is used to enable the clock to blocks B1, B2, and B6 called MOD CLK.

The slot address stored in register B2 selects a 9 bit logical address from the memory indicated by Block B4. This logical address is stored in B7 to be appended to every wire address generated from the data latched from the slot. The 9 bit logical address and the 5 bit wire address form a 14 bit address stored in register B10.

A master controller sends the 14 bit address to the cluster calculation section starting at B12 and could also send it to buffer B11 for multiplexing to the ECLport OUT connector. Slave controllers, i.e., controllers without the MAST LED on,

always route the data to the ECLport OUT connector. The controller furthest from the master controller on the ECLport daisy chain must have its TERM LED on.

An empty crate will route the data from B9, the ECLport IN register, instead of B10. Slave controllers will route the data immediately to the ECLport OUT connector thru buffer B11. Master controllers multiplex the data to the cluster section and if selected to the ECLport OUT connector. Register B9 will cause a crate with no LAMs to insers a 100 nsec. cycle with no data into the data stream appearing at the ECLport OUT connector. DATA RDY is not generated for the zero word, nor does a zero word appear in the internal memory. If there is at least one bit of data in the crate no time penalty is incurred.

ECLport IN accepts READY and DATA signals from preceeding controllers and transmits the slave clock to the preceeding controllers. ECLport OUT transmits READY and DATA signals to the following controllers if it is a slave controller. Otherwise the full 16 bits of data, indicating wire addresses or widths, are transmitted. Slave clock is received by the ECLport OUT connector if the controller is a slave controller. Figure P.1.3.3 shows a system where the ECLports are daisy chained for reading out a large chamber.

The pipeline described so far encodes hit wires into addresses and presents them sequentially to register B12 and buffer B11. Every clock latches the address into B12. Adjacent hit wires are considered a cluster and when encoded have addresses differing only by one. If the addresses are An and An-1 An will eventually appear at the input of B12 and An-1 will be at the output of B12. Block B14 is an adder that takes the difference between An and An-1. A difference of one signifies a cluster, generating an increment level to counter B16. B16 is preloaded with a width of one. The next CLK will increment B16 to a width of 2 and latch An in register B12. B13 will subtract w/2 from An or in this case will subtract one from An. the cluster detector B14 checks for additional adjacent hit wire addresses. If none appear the cluster is over and the width is enabled to registers B18 and B19. The next CLK latches the width in B18 and B19 and latches the centroid An-1 in B15. On the next clock the centroid is latched in B18 and B19. The ECLport OUT source select switch selects the clusterized data from B18 or the buffered address from B11 for presentation to the ECLport OUT connector.

2.2.2 Clock and Control Logic.

Figure P.2.2.2 is a simplified Schematic of the clock generator and control pipeline. The first clock pulse appears 20 nsec. after BUSY is set. BUSY is set by the trailing edge of E1. The clock stops when DATA OUT is true and DATA ACK is false. DATA ACK then controls the clock. If DATA ACK is always true, the clock runs at a 100 nsec. cycle time until BUSY

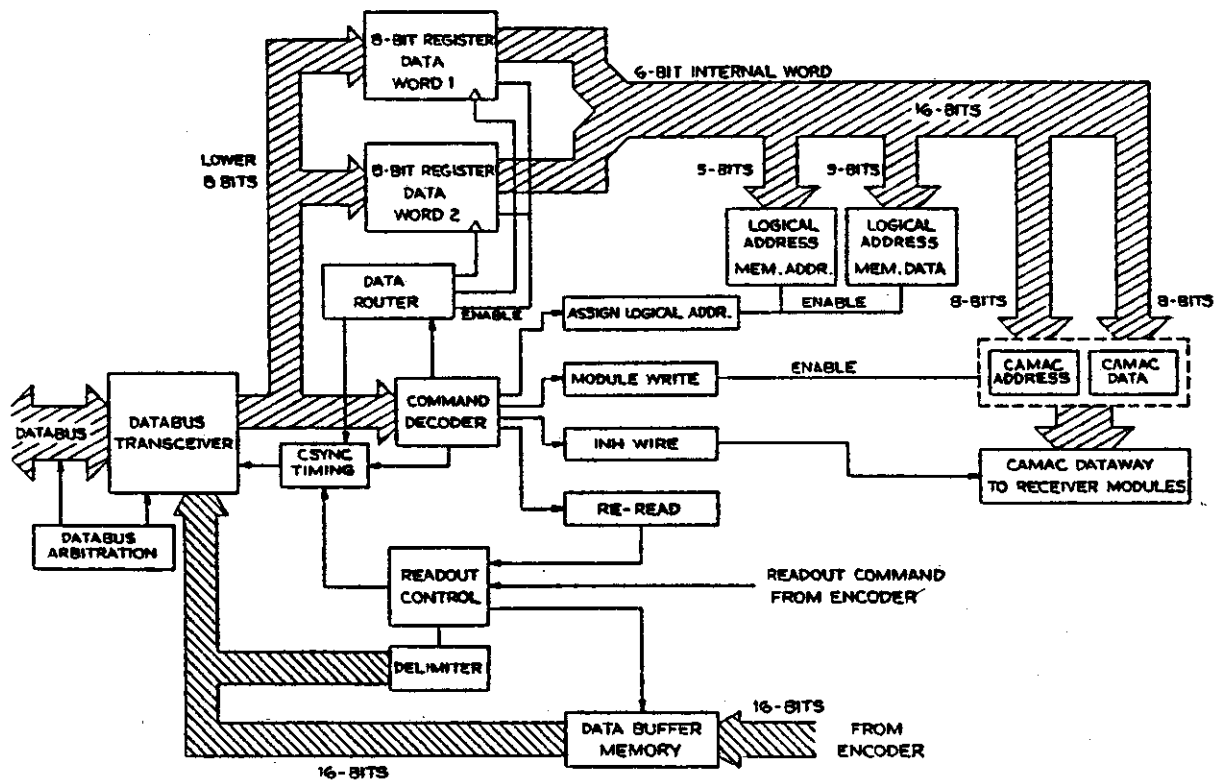
is cleared after all data is encoded.

The control pipeline consist of six registers corresponding to the six staging registers of the data pipeline. Empty and BUSY signals flowing through the control pipeline enable and disable the appropriate logic of the data pipeline. READY and DATA are control signals received from slave controllers signifying their ready status and their data status.

The control pipeline generates DATA RDY for the ECLport and MEM WRITE for the 1K by 16 bit internal memory only when valid data is available. ADD/CLSport selects the data source for the ECLport and the appropriate timing for the DATA RDY.

Figure P.2.2.3 illustrates the relative timing of external NIM and ECL signals and the internal clock. Five wire hits are assumed, 2 nonadjacent and 3 adjacent wires with wire addresses of 10, 15, 23, 24, and 25 respectively. The MSB of the output data is not shown but it would be zero for all addresses and one for the width of 3 wires when the clusterizer is enabled.

Figure P.2.2.3b illustrates the timing when the DATA ACK input is used for handshake timing with the user supplied memory or trigger processor. Note that the internal clock runs at full speed unless data is valid at the ECLport.



DATABUS CONTROL SECTION

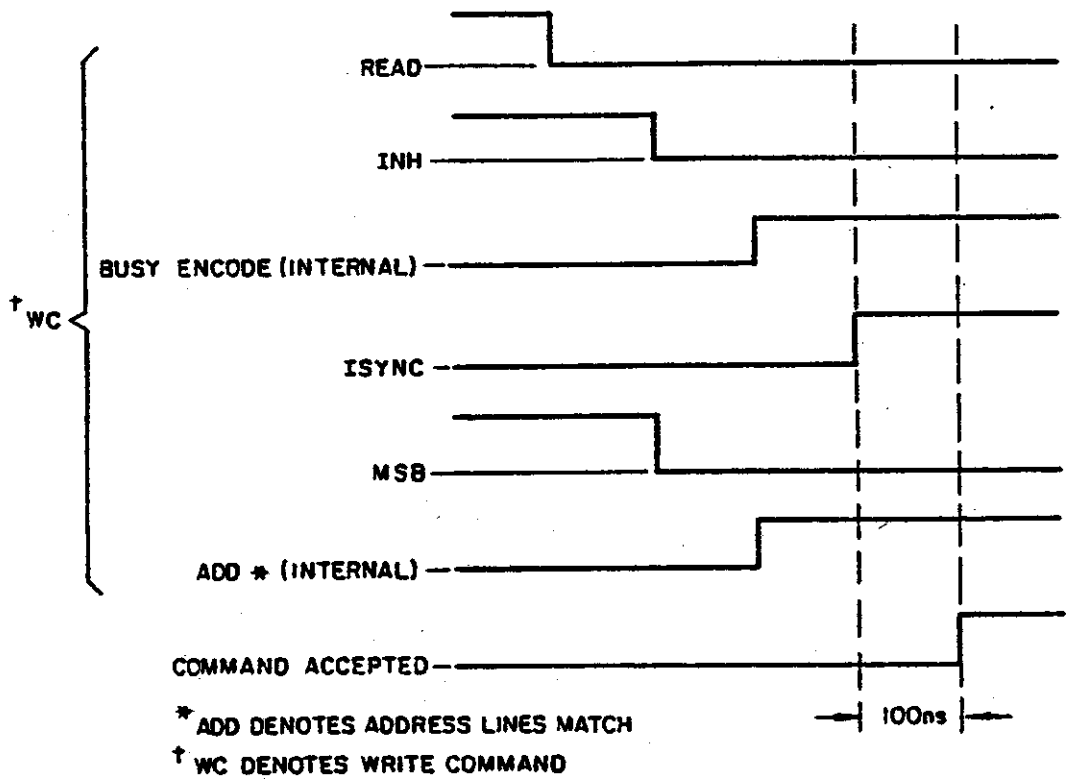
Figure P.2.1.1

LeCROY DATABUS DEFINITION

	PIN #		
BUSY	1	2	/BUSY
LR	3	4	/LR
REQ	5	6	/REQ
CSYN	7	8	/CSYN
GRT	9*	10*	/GRT
ISYN	11	12	/ISYN
INH	13	14	/INH
READ	15	16	/READ
DB16	17	18	/DB16
DB15	19	20	/DB15
DB14	21	22	/DB14
DB13	23	24	/DB13
DB12	25	26	/DB12
DB11	27	28	/DB11
DB10	29	30	/DB10
DB9	31	32	/DB9
DB8	33	34	/DB8
DB7	35	36	/DB7
DB6	37	38	/DB6
DB5	39	40	/DB5
DB4	41	42	/DB4
DB3	43	44	/DB3
DB2	45	46	/DB2
DB1	47	48	/DB1
GND	49	50	GND

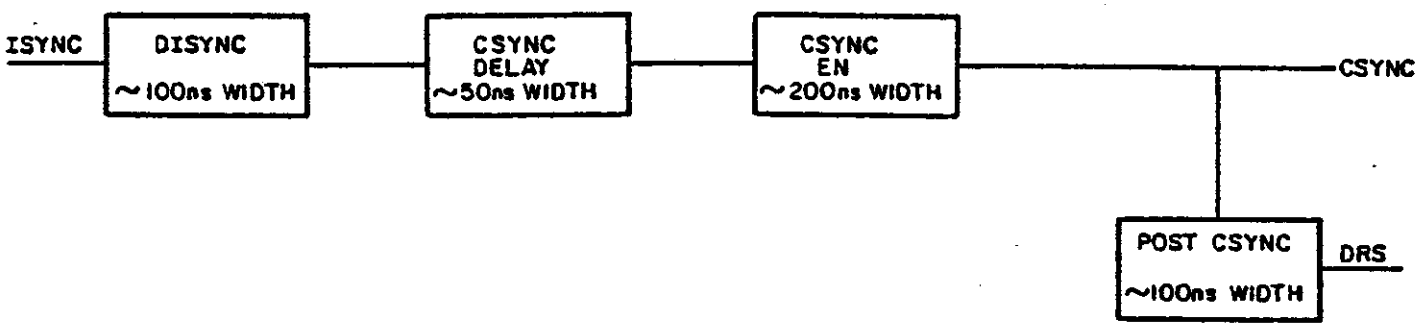
*NOTE THAT THERE IS AN IN CONNECTOR AND AN OUT CONNECTOR SO THERE IS A GRTI AND A GRTO. ALL OTHER PINS ON THE TWO CONNECTORS ARE TIED TOGETHER.

Figure P.2.1.2



DATA BUS WRITE COMMAND

Figure P.2.1.3



ISYNC-CSYNC TIMING

Figure P.2.1.4

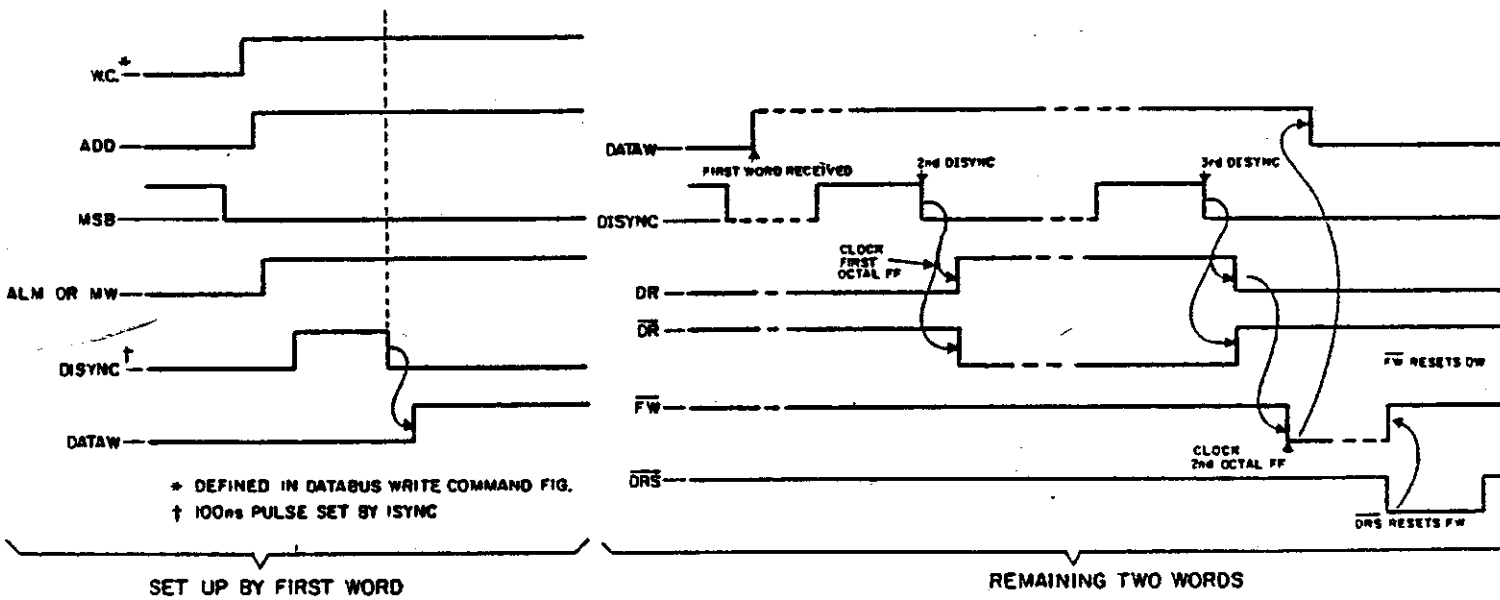
ALA:	A	A	A	A	A	N	N	D	D	D	D	D	D	D	D
MW:	A	A	A	A	A	R	R	R	D	D	D	D	D	D	D

WHERE:

"A" IS ADDRESS
"D" IS DATA
"N" NOT USED
"R" REGISTER

INTERNAL DATA WORD FORMATS

Figure P.2.1.5



COMMAND DATA ROUTER

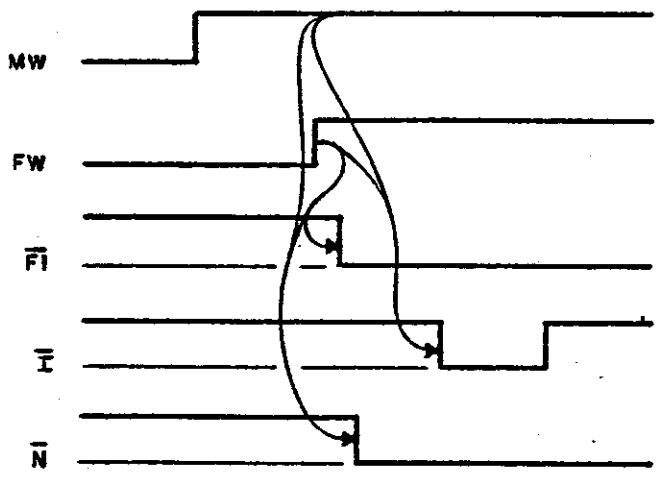
Figure P.2.1.6

MODULE WRITE	DATA LINES
CAMAC LINES	CONTROLLER REDEFINTION
A4	R3
A2	R2
A1	R1
W9	V8
W10	V7
W11	V6
W12	V5
W13	V4
W14	V3
W15	V2
W16	V1

WHERE:
"R" IS A REGISTER ADDRESS
"V" IS DATA
(SEE ALA IN SPEC. SHEET)

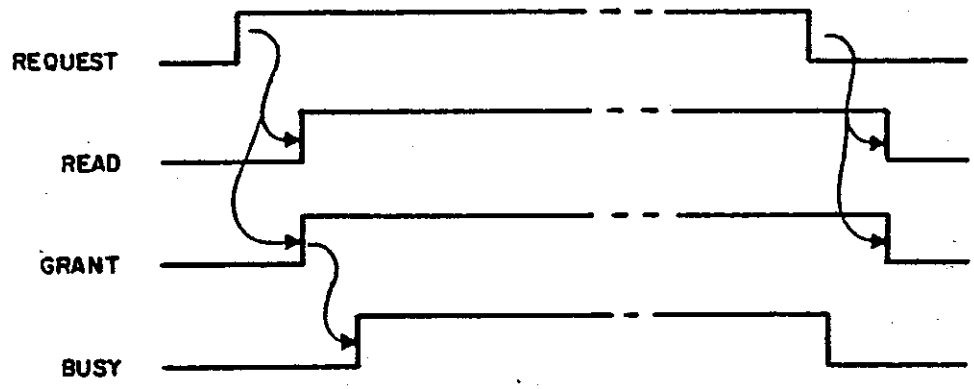
MODULE WRITE DATA LINES

Figure P.2.1.7a



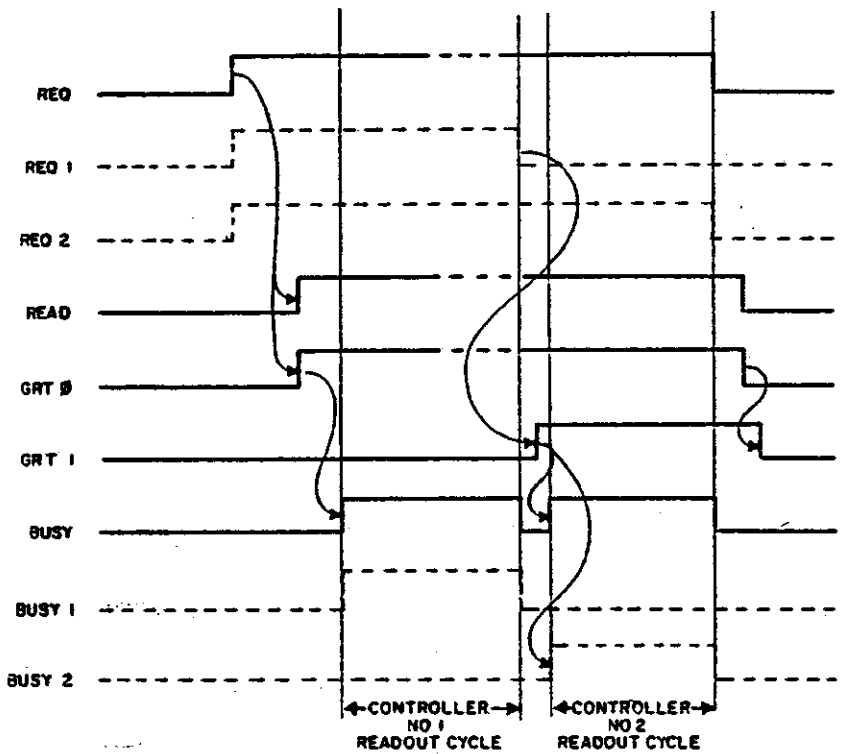
MODULE WRITE CONTROL SIGNAL TIMING

Figure P.2.1.7b



DATABUS ARBITRATION, ONE CONTROLLER ON BUS

Figure P.2.1.8



MULTIPLE CONTROLLER ARBITRATION
(DOTED WAVEFORMS INDICATE WHICH CONTROLLER INITIATES THE WAVEFORM ON THE DATABUS.)

Figure P.2.1.9

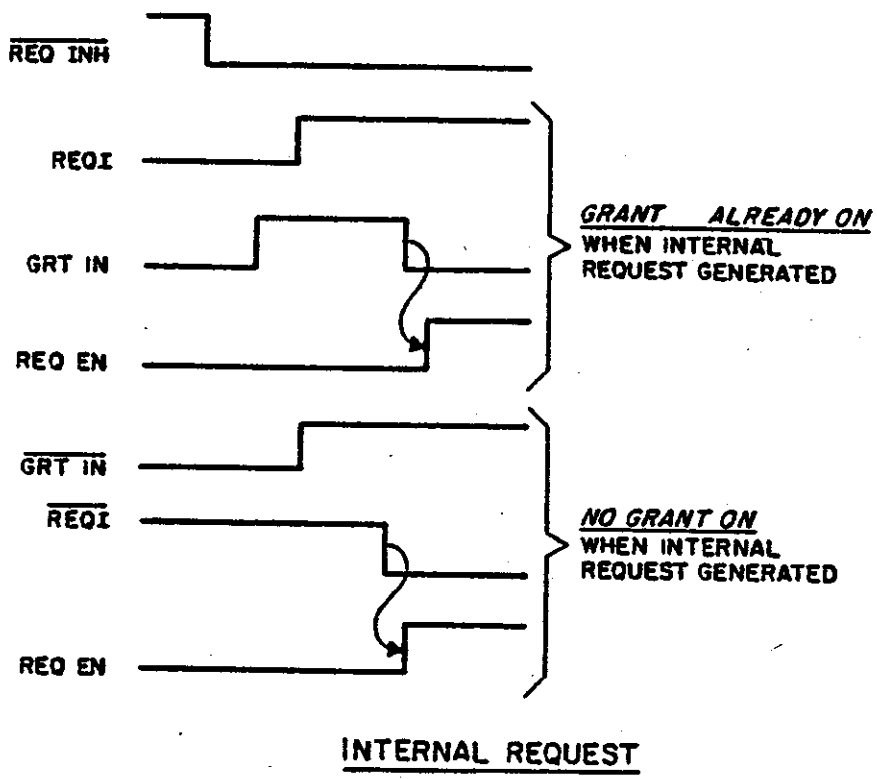
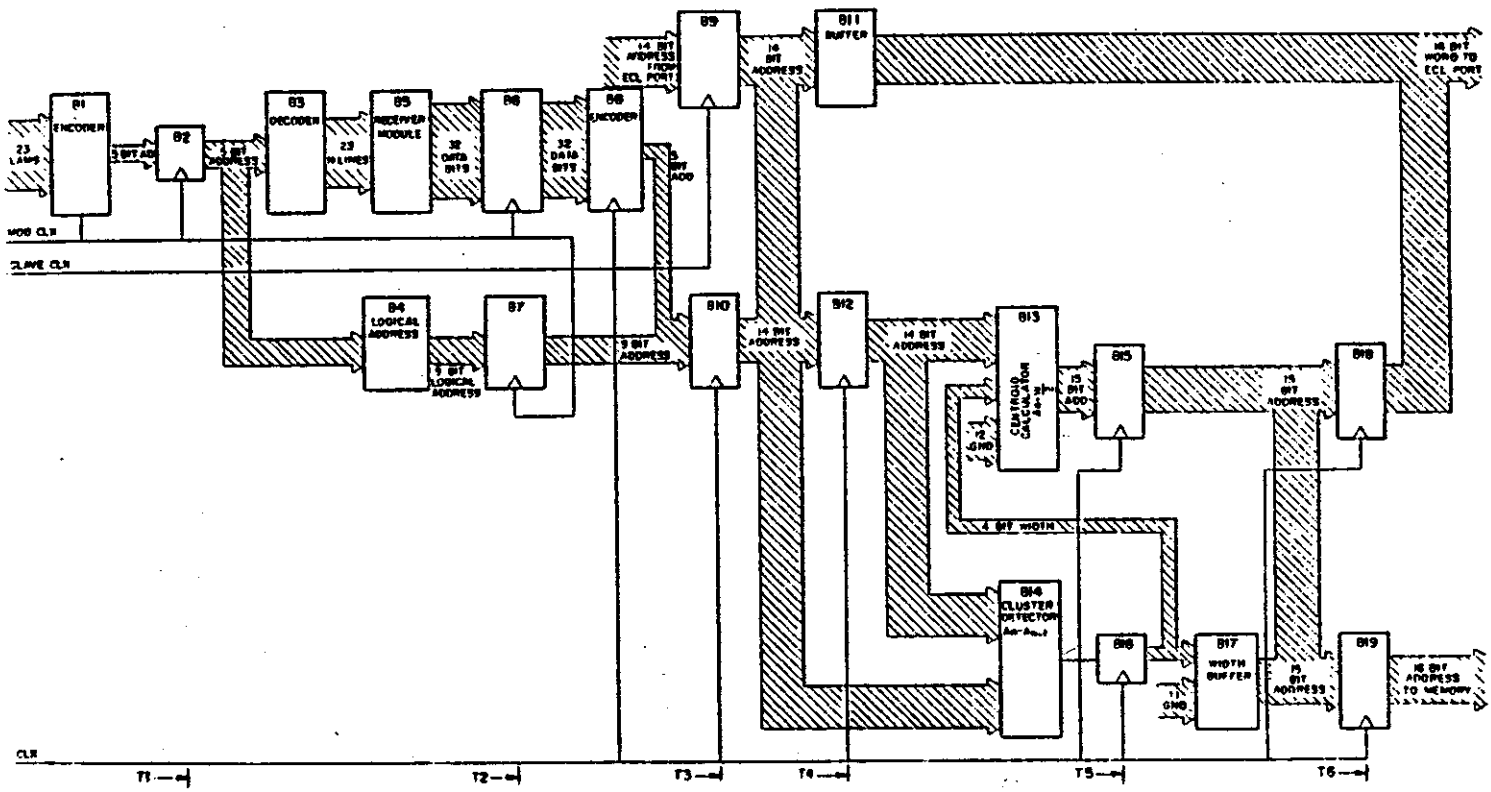
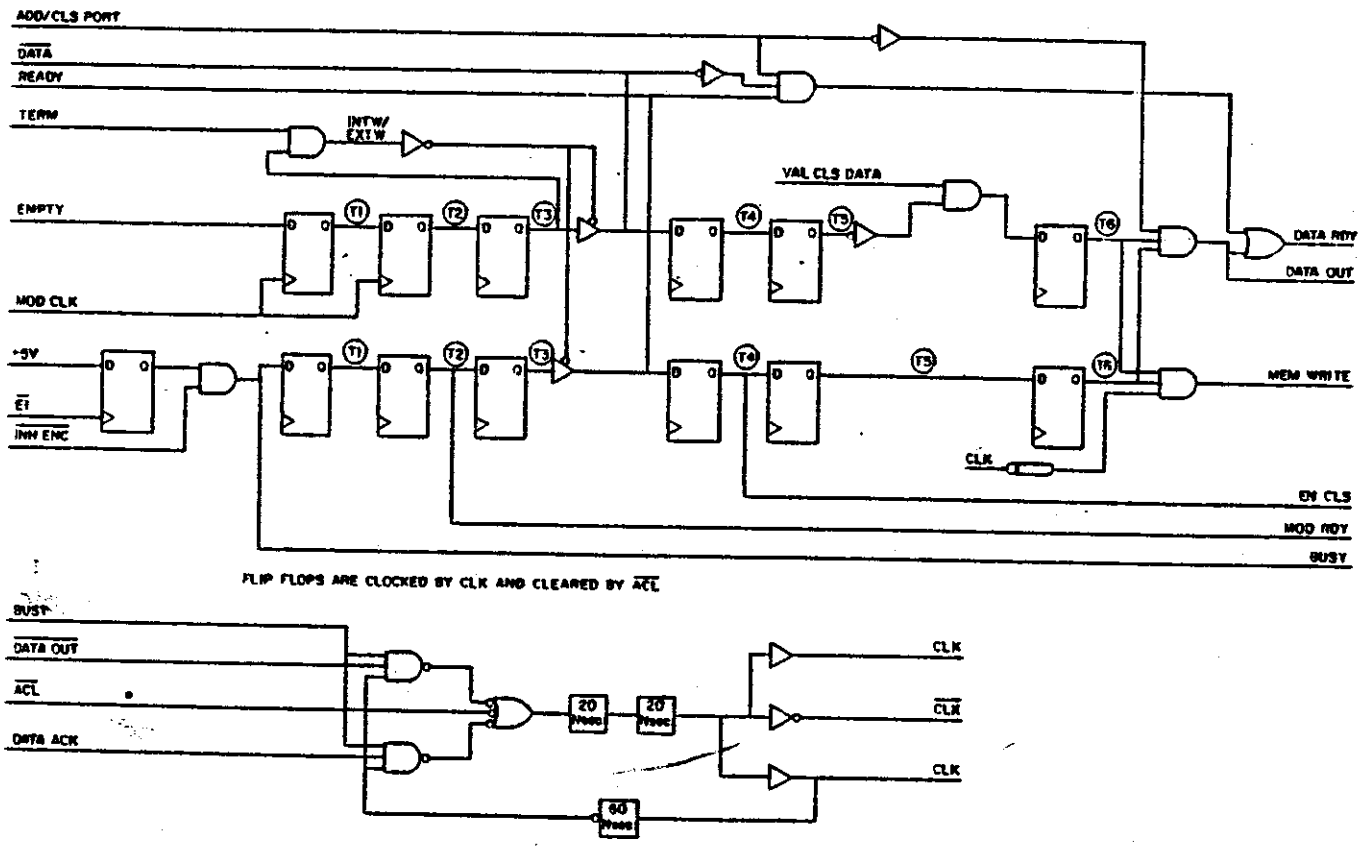


Figure P.2.1.10



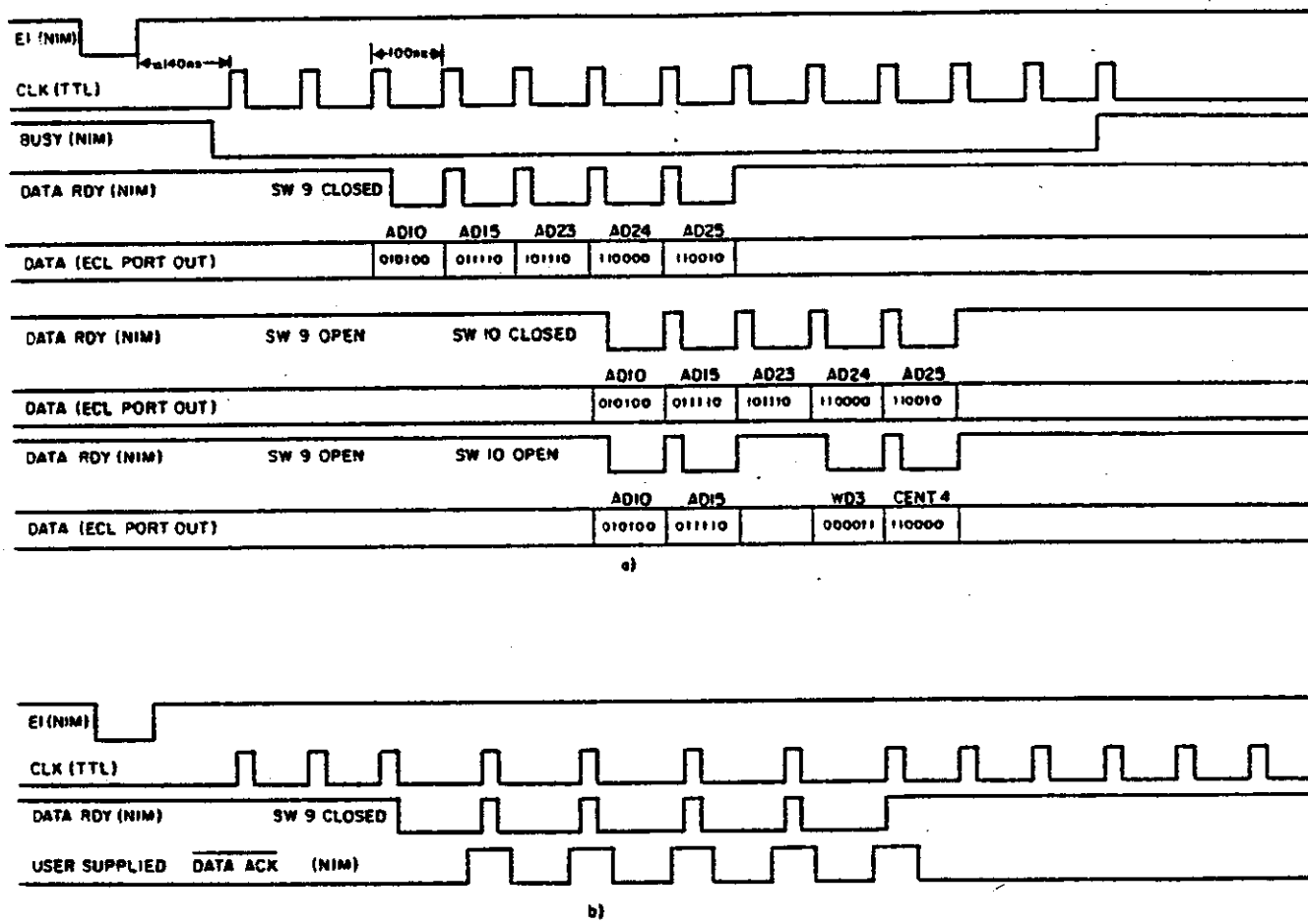
ENCODER AND CLUSTERIZER BLOCK DIAGRAM

Figure P.2.2.1



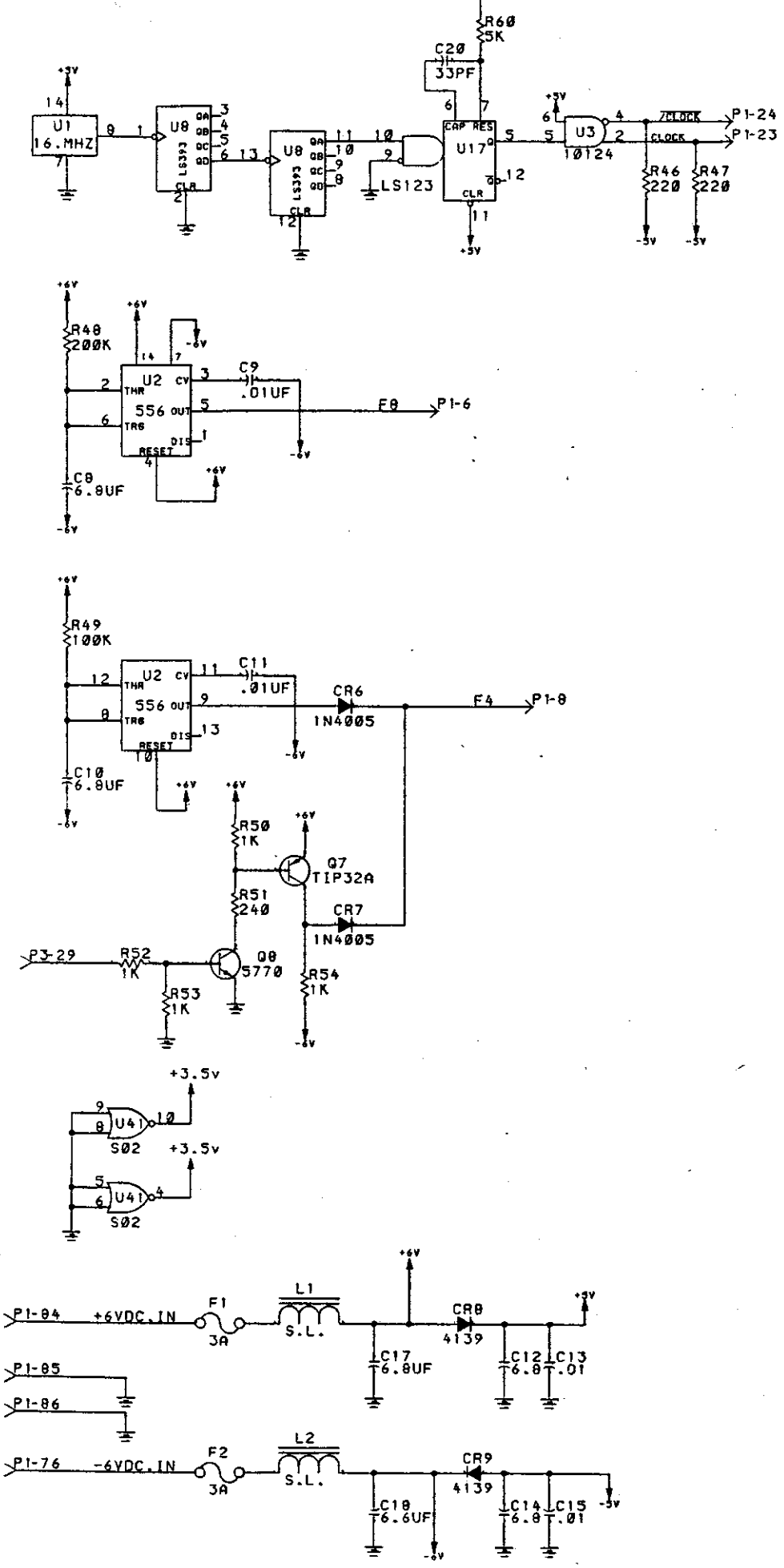
CLOCK AND CONTROL LOGIC BLOCK DIAGRAM

Figure P.2.2.2



ENCODER AND CLUSTERIZER TIMING DIAGRAM

Figure P.2.2.3


R60
5K
C20
33PF
U1
16.MHZ
U8
LS393
U8
LS393
LS123
U17
CAP RES
U3
10124
/CLOCK
CLOCK
P1-24
P1-23
R46
220
R47
220
R48
200K
U2
556
C9
.01UF
F8
P1-6
C8
6.8UF
R49
100K
C11
.01UF
CR6
1N4005
F4
P1-8
C10
6.8UF
R50
1K
Q7
TIP32A
R51
240
CR7
1N4005
P3-29
R52
1K
Q8
S770
R53
1K
R54
1K
+3.5v
U41
S02
U41
S02
P1-84
+6VDC.IN
F1
3A
L1
S.L.
CR8
4139
C17
6.8UF
C12
6.8
C13
.01
P1-85
P1-86
P1-76
-6VDC.IN
F2
3A
L2
S.L.
CR9
4139
C18
6.6UF
C14
6.8
C15
.01