# CAMAC MODEL 4299

# DATABUS INTERFACE BUFFER

March, 1982

# WARRANTY

LeCROY RESEARCH SYSTEMS CORP. warrants each instrument it manufactures to be free from defects in material and workmanship under normal use and service for the period of 1-year from date of purchase. Custom monolithics and hybrids sold separately and all spare or replacement parts are warranted for 90-days. This warranty extends only to the original purchaser. This warranty shall not apply to fuses, disposable batteries or any product or parts which have been subject to misuse, neglect, accident or abnormal conditions of operations.

In the event of failure of a product covered by this warranty, LeCroy will repair and calibrate an instrument returned to the factory or an authorized service facility within 1 year of the original purchase; provided the warrantor's examination discloses to its satisfaction that the product was defective. The warrantor may, at its option, replace the product in lieu of repair. With regard to any instrument returned within one year of the original purchase, said repairs or replacement will be made without charge. If the failure has been caused by misuse, neglect, accident or abnormal conditions or operations, repairs will be billed at a nominal cost. In such case, an estimate will be submitted before work is started, if requested.

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IF ANY FAILURE OCCURS, notify LeCroy Research Systems Corp., or the nearest service facility, giving full details of the difficulty, and include the Model number, serial number, and FAN (Final Assembly Number) or ECO (Engineering Change Order) number. On receipt of this information, service data or shipping instructions will be forwarded to you. On receipt of the shipping instructions, forward the instrument, transportation prepaid. A Return Authorization number will be given as part of shipping instructions. Marking this RA number on the outside of the package will insure that it goes directly to the proper department within LeCroy. Repairs will be made at the service facility and the instrument returned, transportation prepaid.

ALL SHIPMENTS OF LECROY INSTRUMENTS FOR REPAIR OR ADJUSTMENT should be made via Air Freight or "Best Way" prepaid. The instrument should be shipped in the original packing carton; or if it is not available, use any suitable container that is rigid and of adequate size. If a substitute container is used, the instrument should be wrapped in paper and surrounded with at least four inches of excelsior or similar shock-absorbing material.

IN EVENT OF DAMAGE IN SHIPMENT to original purchaser the instrument should be thoroughly inspected immediately upon original delivery to purchaser. All material in the container should be checked against the enclosed packing list. The manufacturer will not be responsible for shortages against the packing sheet unless notified immediately. If the instrument is damaged in any way, a claim should be filed with the carrier immediately. (To obtain a quotation to repair shipment damage, contact the LeCroy factory or the nearest service facility).

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ANY APPLICATION OR USE QUESTIONS, which will enhance your use of this instrument will be happily answered by a member of our Engineering Services Department, telephone 914-425-2000 or your local distributor. You may address any correspondence to:

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TECHNICAL DATA

LeCroy


# CAMAC Model 4299

# Databus Interface

The LeCroy 4299 is a single-width CAMAC interface and data buffer designed for use with LeCroy's expanding family of dedicated CAMAC crate data acquisition systems. These include System 4290, PCOS III, and others. The Model 4299 allows connecting of up to 16 dedicated crates to a single CAMAC station.

The LeCroy DATABUS connects the 4299 with System Controllers (4298, 2738, etc.). This is a bi-directional 16-bit ribbon cable bus. It allows data to be read from LeCroy dedicated crate systems and test or control information to be downloaded to the crates.

The system includes a 4k × 16-bit memory. This allows blocks of data to be transferred to the 4299. Block transfer is ideal for applications which require rapid readout. It may also be operated in the Word Step mode. Data words may be transferred one at a time under CAMAC control.

The Model 4299 has been designed with maximum flexibility for readout of data acquisition systems. The Model 4299 offers destructive or non-destructive readout. It also offers a word count register to facilitate block transfer readout. Side panel accessed switches enable memory overwrite protection from either the Dataway or the DATABUS. Thus, the 4299 may be used as a multiple-event buffer or as a single-event buffer. Front panel Lemo-type connectors allow the user to reset or clear the 4299 with NIM pulses.

A register internal to the Model 4299 can be set by any dedicated controller in the DATABUS chain. This sets the LAM of the Model 4299 and lights a front panel LED labeled LR. The LAM status of the 4299 can be tested or cleared by standard CAMAC commands. It can also be cleared via the front panel Reset or Clear Lemo inputs provided that none of the System Controllers are asserting the LAM.

The operating mode of the LAM circuit can be selected via a side-panel switch, CLEAR LAM. The CLEAR LAM switch has the following four positions:

LMD: The LAM memory circuit is disabled. Reset is possible via dedicated crate controller only.

FWR: LAM is reset at the end of the first readout cycle, FR, or by any of the valid clear functions.

LWR: LAM is reset at the end of the last readout cycle, FR, or by any one of the valid clear functions.

DRC: LAM is not automatically reset by the readout function, FR. All other clear functions remain valid.

May 1982

*Innovators in Instrumentation*

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TWX: 710-577-2832 CABLE: LERESCO TELEPHONE: (914) 425-2000

# SPECIFICATIONS
# CAMAC Model 4299
# DATABUS INTERFACE BUFFER

**INPUTS**

| | |
|---|---|
| General: | Front panel connectors, LEMO type. |
| Impedance: | 50 Ω ± 5%. Direct coupled. Requires NIM-level signal. |
| Reset (RT): | One; resets all registers and memory. Minimum width: 20 nsec. |
| Clear (CL): | One; clears memory only. Minimum width: 50 nsec. |

**OUTPUTS**

| | |
|---|---|
| General: | Front-panel connectors, LEMO type. High impedance current source. Bridge outputs. NIM levels into 25 Ω; 0 level = 0 mA ± 4 mA; 1 level = 32 mA ± 4 mA. Risetimes and falltimes: < 5 nsec, overshoot: 10%. |
| Memory Busy (MB): | Memory Busy signal; indicates that the memory contains data or is being accessed. |
| DATABUS Busy (DB): | DATABUS Busy signal; indicates that the DATABUS BUSY is activated. |

**CAMAC COMMANDS**

| | |
|---|---|
| C•S2: | Memory clear (jumper option). |
| Z•S2 | Clears memory, initializes logic status of the unit and generates initialize cycle on the DATABUS. |
| I: | Activates DATABUS Inhibit line. Front-panel INH LED indicates status. |
| L: | LAM signal is activated by DATABUS LR request. A front-panel LR LED inidicates status. (See LOOK AT ME on previous page.) |
| X: | An X-response is generated when any valid N•A•F command below is recognized even though it may not be executed. |
| Q: | A Q-response is generated only if the request function can be executed. |
| N•F(R)•A(0): | Memory destructive READ function. Can be chosen among CAMAC functions F(0), F(1), F(2) or F(3). Q-response generated if function is executed. |
| N•F(R)•A(1): | Memory non-destructive READ function. Can be chosen among CAMAC functions F(0), F(1), F(2) or F(3). Q-response generated if function is executed. |
| N•F(8)•[A(0) + A(1)]: | Tests LAM. Q-response generated only if LAM is present. |
| N•F(9)•[A(0) + A(1)]: | Clears memory, initializes logic status of the unit, and generates initialize cycle on the DATABUS. Q-response generated. |
| N•F(11)•A(0): | Clears memory. Q-response generated if memory not activated by the DATABUS. |
| N•F(11)•A(1): | Initialize memory address counter for a new readout cycle. Q-response generated if memory not activated by the DATABUS. |
| N•F(W)•A(0): | DATABUS WRITE function. Can be chosen among. CAMAC functions F(16), F(17), F(18) or F(19) to write one word at a time on the DATABUS. Q-response generated if function is executed. |
| N•F(W)•A(1): | Memory WRITE function. Can be chosen among CAMAC functions F(16), F(17), F(18) or F(19). Q-response generated if function is executed. |
| N•F(24)•[A(0) + A(1)]: | Sets DATABUS Inhibit. Q-response generated. |
| N•F(25)•[A(0) + A(1)]: | Triggers the transfer of memory data onto the DATABUS. Q-response generated if data transfer is executed. |
| N•F(26)•[A(0) + A(1)]: | Resets DATABUS Inhibit. Q-response generated. |
| N•F(27)•[A(0) + A(1)]: | Tests DATABUS BUSY signal. Q-response generated if DATABUS BUSY signal is present. |
| R1 to R16: | Data read lines. |
| W1 to W16: | Data write lines. |

**PACKAGING** No. 1 RF-shielded CAMAC module conforming to ESONE Report EUR4100e and IEEE Standard 583.

**CURRENT REQUIREMENTS** + 6 V at 2A; − 6 V at 200 mA.

SPECIFICATIONS SUBJECT TO CHANGE


# CAMAC MODEL 4299

## DATABUS INTERFACE BUFFER

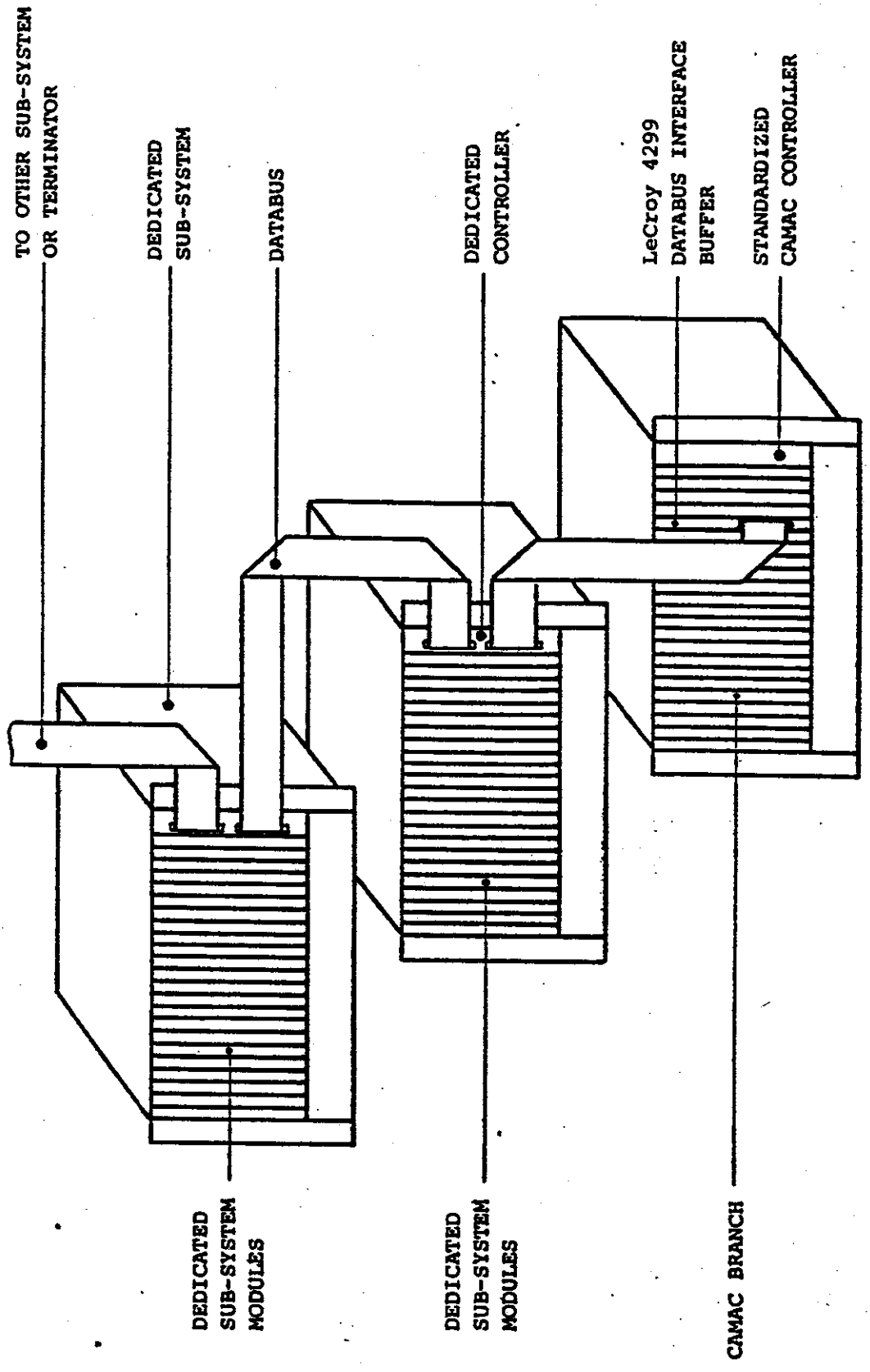
The LeCroy Model 4299 Databus Interface is the interface between a standard CAMAC system and the normalised LeCroy DATABUS. It is housed in a CAMAC module 1 # width and compatible with the EURATOM EUR 4100e norms.

The LeCroy DATABUS fast bus has been designed to transfer 16 bit parallel word from CAMAC to daisy chained data acquisition sub-systems or from these sub-systems to CAMAC.

All DATABUS handshake timing are controlled by the Model 4299 Databus Interface, which has four sections:

- a 4K, 16 bit words Input/Output memory, well suited for data block transfer between CAMAC and DATABUS or DATABUS and CAMAC
- a 16 bit register, well suited for one word transfer from CAMAC to DATABUS
- the control logic, which allows CAMAC control over the DATABUS
- the synchronization logic between CAMAC and DATABUS.

The design of this unit provides maximum flexibility to control and readout dedicated data acquisition systems at high speed. It leaves to the dedicated crate controller freedom of choosing its operating mode, its command, or data word structure as well as its data transfer rate.




DATABUS SYSTEM CONFIGURATION (FIG. 1)

# LeCroy DATABUS FUNCTIONS DESCRIPTION

By definition, the DATABUS is in WRITING MODE when the data are transferred from the 4299 module to the Controller and in READING MODE during the transfer from the Controller to the 4299 module.

READ line: Activated by the 4299 module, it indicates the sense of the data transfer.
In disable state the DATABUS is in WRITING MODE or in stand by.
In enable state the DATABUS is in READING MODE and is maintained throughout data readout.

INH line: INHibit, activated by the 4299 module.
It is set by the I CAMAC line or the 4299's inhibit circuit if the BUSY line is not activated. This circuit is set by F(24) CAMAC function and cleared by F(26) and Z.
On the front panel of the 4299 module, a INH LED indicates if inhibit circuit is set.

REQ line: REQuest, activated by the Controller for a readout demand.
It must be maintained throughout data readout.

GRT line: GRanT, activated by the 4299 module.
It is set in response to a REQ and maintained as long as 4299 module can accept data.

ISYN line: Interface SYNchronization, activated by the 4299 module.
In WRITING MODE transfer, a synchronization ISYN signal is sent from the 4299 module along with the data. ISYN is true until CSYN is returned to the interface. CSYN is the Controller acknowledgement of ISYN. In case where CSYN is not returned, an automatic 25 µs time out will reset ISYN and the 4299 module considers the transfer as executed.
In READING MODE transfer, ISYN is the interface acknowledgement of CSYN. A ISYN pulse is sent after the data present is loaded into the interface memory.

CSYN line: Controller SYNchronization, activated by the controller.
In WRITING MODE transfer, a CSYN pulse must be sent in response to ISYN after the data is loaded.
In READING MODE, and if GRT is present, a CSYN must be sent simultaneously with the data and true until ISYN is returned.

BUSY line: Activated by the Controller. Indicates that the controller is busy. When the BUSY line is true, on the front panel of 4299 module, the DB LED is ON and a DC NIM level is present at the DB output.
A Q response is generated in recognition of F(27).

LR line: Lam Request, activated by the Controller.
CAMAC LAM can be set either by a DC level or a pulse on the LR line. An LR pulse or DC level is memorized by the LAM memory circuit in the 4299 module and a front panel LR LED is turned on.
The LAM circuit status can be tested by F(8) or F(10) functions and it can be cleared by miscellaneous CAMAC functions or via front panel inputs RT and CL, provided that the LR line is no longer activated.
An LR DC level method must be employed if a LAM request with high level of priority is necessary. Because it is not possible to clear the LAM directly in the 4299 module, but only by an action on the controller.

DATA lines: In WRITING MODE, the 16 DATA lines are activated by the 4299 module and the data is valid during all the time of the ISYN.
In READING MODE, the 16 DATA lines can be activated by the Controller, simultaneously with a CSYN, only if the GRT is received. The data must be valid until the ISYN is not received.

An initialization cycle demand is provided by the 4299 module on the DATABUS by a pulse simultaneously on the READ and INH lines.

# LeCroy DATABUS SPECIFICATIONS

**Cable:** 50 conductors ribbon cable or 25 twisted pairs flat cable.
Impedance 110 ohms.
Maximum length > 500 feet.

**Connector:** Cable: 3M type 3425-6050
Receiver: 3M type 3433-1302 with two polarizing key type 3518.

**Levels:** TTL differential.

**Drivers:** Tri-state differential output type 26LS31 or equivalent.

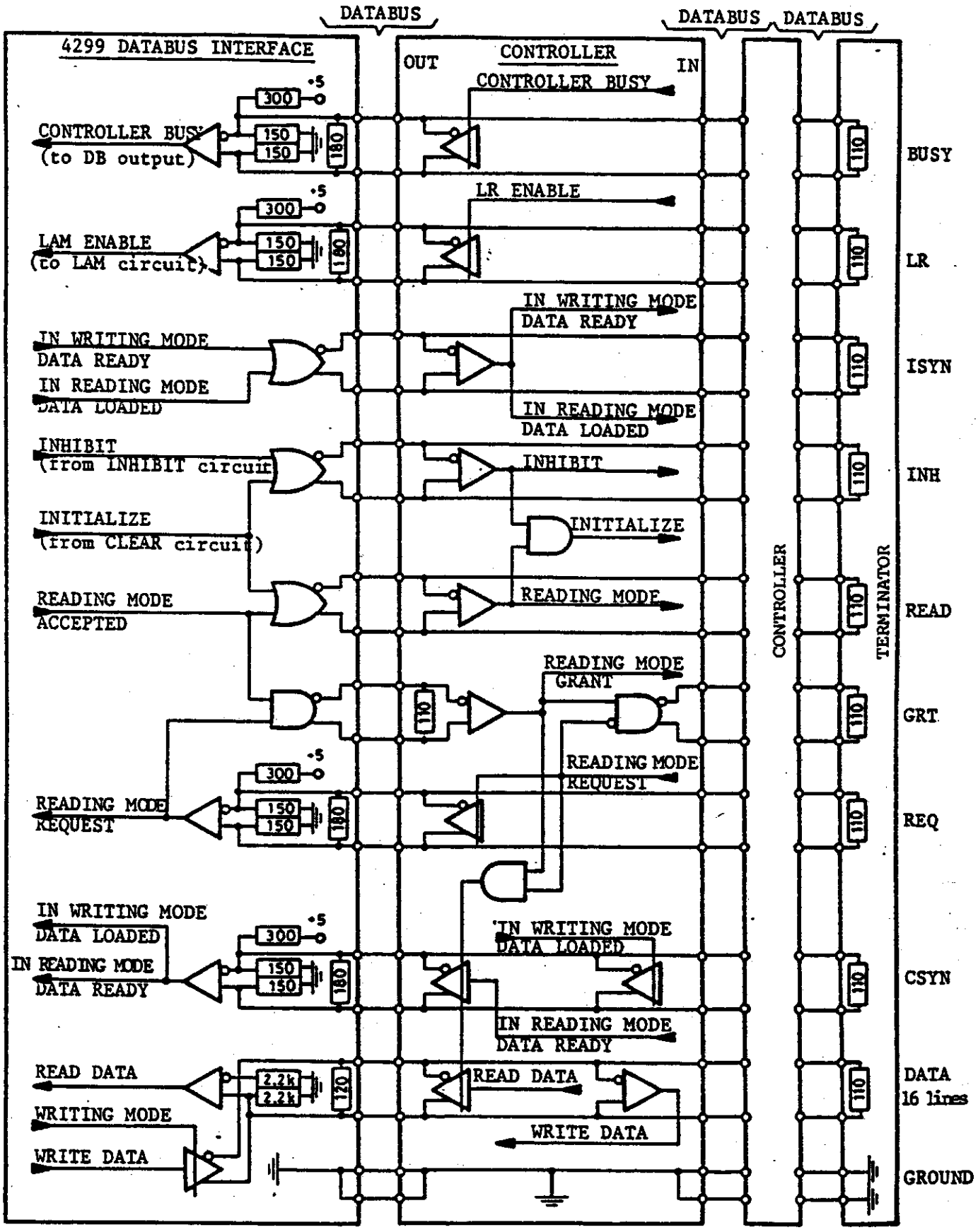
**Receivers:** High impedance differential input type 26LS32 or equivalent.
Hysteresis 200 mV.
The INH, READ, GRANT and ISYN lines must be integrated (approx. 50 ns) in the controller for suppressing the crosstalk and reflection problems.

**Terminator:** For a very long DATABUS cable ( approx. > 300 feet), it is necessary to terminate the DATABUS on the least controller with a LeCroy DAT-TR/50 terminator.

Levels & currents:

| LINES \ STATES | | WAITING | 0 | 1 |
|---|---|---|---|---|
| INH<br>READ<br>GRT<br>ISYN |  | ------- | <0,8V to 25mA | > 2V to -25mA |
| |  | ------- | > 2V to -25mA | <0,8V to 25mA |
| BUSY<br>LR<br>REQ<br>CSYN |  | Output disable<br>±20 µA to 0,6V | on CSYN in READING MODE only<br><0,8V to 36mA | > 2V to -30mA |
| |  | Output disable<br>±20 µA to 1,2V | on CSYN in READING MODE only<br>> 2V to -30mA | <0,8V to 36mA |
| DATA |  | Output disable<br>±20 µA to 0V | <0,8V to 25mA | > 2V to -25mA |
| |  | Output disable<br>±20 µA to 0V | > 2V to -25mA | <0,8V to 25mA |

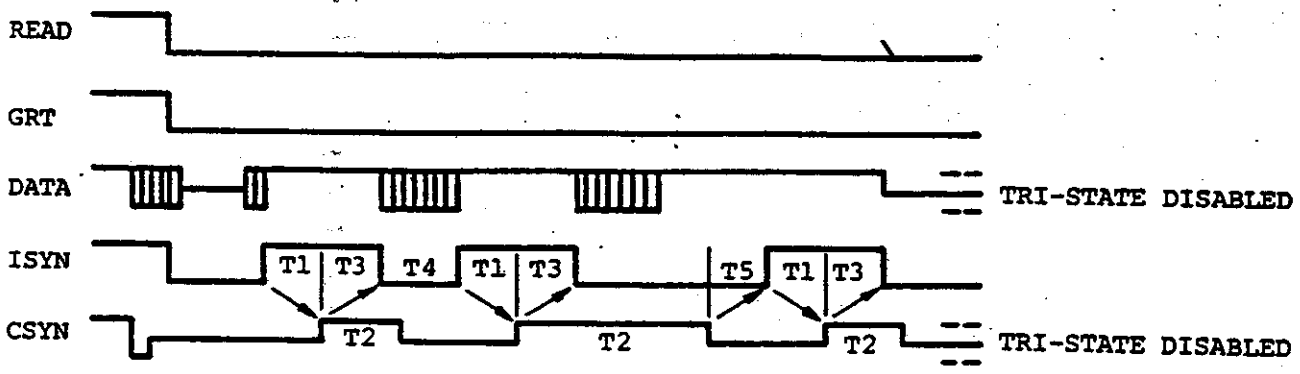
LECROY DATABUS INPUT/OUTPUT STRUCTURE (FIG. 2)



# LeCroy DATABUS TIMING

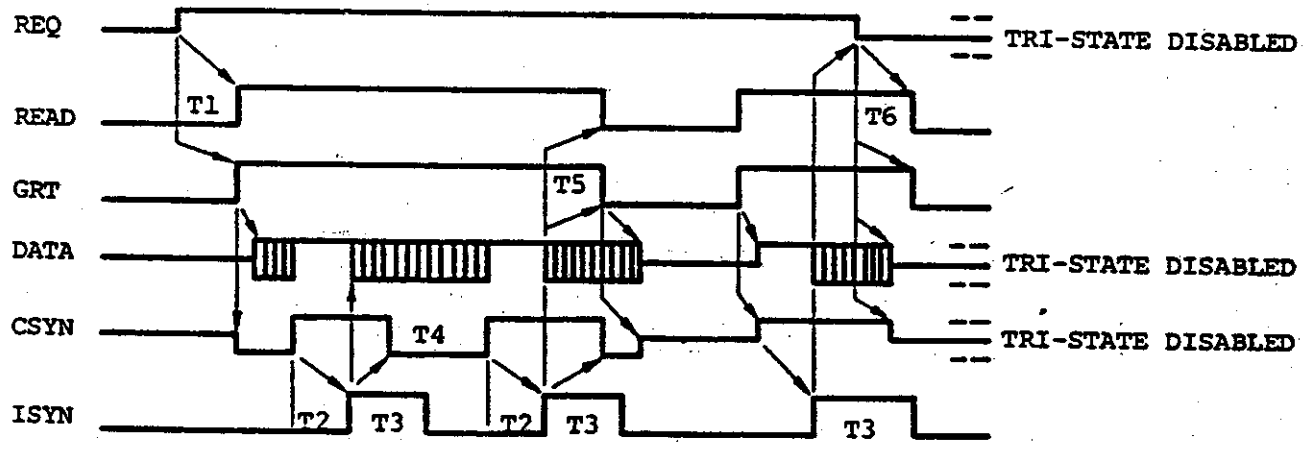
The speed of the transfers depends on the DATABUS cable length.
Maximum frequency: 2 Mc.

WRITING MODE:



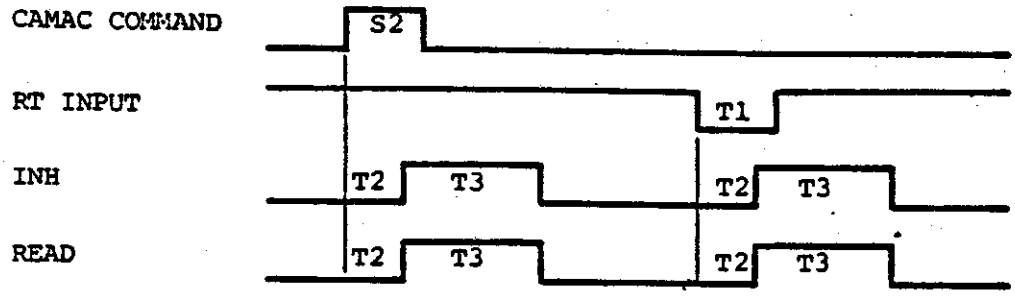

T1: < 25 µs.
T2: > 200 ns . Adjustable in the Controller.
T3: 120 ns.
T4: from 200ns to 600ns. Adjustable by P3 potentiometer in the 4299 module.
T5: 120 ns.

READING MODE:




T1: 120 ns.
T2: from 200ns to 600ns. Adjustable by P3 potentiometer in the 4299 module.
T3: from 200ns to 600ns. Adjustable by P2 potentiometer in the 4299 module.
T4: > 200 ns.
T5: < 150 ns.
T6: 120 ns.

## INITIALISE CYCLE

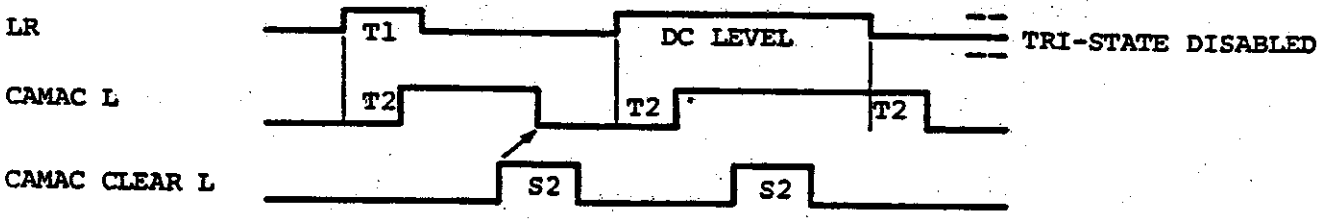



T1 :> 20 ns
T2 : 60 ns
T3 : from 200 ns to 1 µs. Adjustable by P1 potentiometer in the 4299 module

## BUSY CYCLE


T1 : < 80 ns

## LAM REQUEST CYCLE




T1 : from 200 ns to 1 µs. Adjustable in the controller.
T2 : 100 ns

# DATABUS CONNECTOR ASSIGNMENT

| | | | | | |
|---|---|---|---|---|---|
| BUSY | | 1 | 2 | $\overline{\text{BUSY}}$ | |
| LR | | 3 | 4 | $\overline{\text{LR}}$ | |
| REQ | | 5 | 6 | $\overline{\text{REQ}}$ | |
| CSYN | | 7 | 8 | $\overline{\text{CSYN}}$ | |
| GRT | | 9 | 10 | $\overline{\text{GRT}}$ | |
| ISYN | | 11 | 12 | $\overline{\text{ISYN}}$ | |
| INH | | 13 | 14 | $\overline{\text{INH}}$ | |
| READ | | 15 | 16 | $\overline{\text{READ}}$ | |
| DATA | 16 | 17 | 18 | $\overline{\text{DATA}}$ | 16 |
| | 15 | 19 | 20 | | 15 |
| | 14 | 21 | 22 | | 14 |
| | 13 | 23 | 24 | | 13 |
| | 12 | 25 | 26 | | 12 |
| | 11 | 27 | 28 | | 11 |
| | 10 | 29 | 30 | | 10 |
| | 9 | 31 | 32 | | 9 |
| | 8 | 33 | 34 | | 8 |
| | 7 | 35 | 36 | | 7 |
| | 6 | 37 | 38 | | 6 |
| | 5 | 39 | 40 | | 5 |
| | 4 | 41 | 42 | | 4 |
| | 3 | 43 | 44 | | 3 |
| | 2 | 45 | 46 | | 2 |
| DATA | 1 | 47 | 48 | $\overline{\text{DATA}}$ | 1 |
| GROUND | | 49 | 50 | GROUND | |

# 4299 DATABUS INTERFACE GENERAL DESCRIPTION

In the model 4299, the 4K memory can not be accessed simultaneously by CAMAC and DATABUS. Memory data may be protected from being overwritten depending upon the memory access option chosen. These options, which are side panel MEMORY CONTENT PROTECTION switches selectable, are described under MEMORY ACCESS OPTIONS.

The GRANT response to a DATABUS REQUEST as well as the Q response to a CAMAC memory writing function will be suppressed when the memory data is to be protected or if the memory is full.
In DATABUS READING MODE, the end of the data block transfer is recognised at the time the DATABUS REQ line is released.

All valid CAMAC functions will respond to N•A(0) or N•A(1) and generate an X response. A Q response is generated only if the command can be executed or in response to a test status.

The main 4299 DATABUS INTERFACE are the following :

- DATABUS and INTERFACE INITIALISE

  When a CAMAC Z•S2 or F(9)A(0+1)S2 functions or on the front panel RT input pulse is received all registers and memory are cleared and an initialise cycle is setted on the DATABUS (sets a pulse on the DATABUS INH and READ lines). These functions have priority over other functions.

- MEMORY CLEAR

  When a CAMAC C•S2 or F(11)A(0)S2 functions or on the front panel CL input pulse is received the memory and the LAM memory are cleared. These functions have priority over the data transfer.

- DATABUS BUSY : DB

  When the DATABUS BUSY line is true, the front panel LED DB is on and a DC NIM level is present at the two DB output connectors. These two connectors are bridged to permit easy ORing of the BUSY signals. A Q response is generated in recognition of F(27)A(0+1) if DATABUS BUSY line is activated.

- DATABUS INHIBIT : INH

  When the CAMAC I command is present or if the INHIBIT memory is on, the DATABUS INH line and the front panel LED INH are activated. The INHIBIT memory is set by F(24)A(0+1)S1 and cleared by F(26)A(0+1)S1.
  The DATABUS INH command is not possible if the DATABUS BUSY line is activated.

- DATABUS SYNCHRONISATION : ISYN - CSYN

In the DATABUS WRITING MODE, a synchronisation signal ISYN is sent from the INTERFACE to the DATABUS along with the data. ISYN is true until CSYN response is returned to the Interface. In case where CSYN is not returned, an automatic 25 µs time out will reset ISYN and the Interface considers the command as executed.

Quiescently, the DATABUS is in the READING MODE. Upon receipt of a REQUEST, and provided its memory is not full or being accessed, the Interface will switch the DATABUS into the READING MODE and respond with a READ and GRANT signal as long as the REQUEST is maintained. Following CSYN will be accepted and load data present into the 4K memory. Each completed load cycle will return an ISYN response pulse. Memory full will reset READ and GRANT lines, and stop the data transfer.

- DATABUS WRITE FUNCTION : FW

FW is patch selectable among F(16), F(17), F(18) or F(19).

a) WORD STEPPING MODE : FW·A(0).

In this mode, the Interface 4K memory is not used and data 16 bit words are transmitted one at a time from the CAMAC dataway to the DATABUS. The Q response is suppressed when DATABUS is activated.

b) BLOCK TRANSFER MODE : FW·A(1)

In this mode, the interface memory is loaded at S2. The memory write is sequential and the memory writing address is incremented at the end of each FW·A(1) cycle. The first FW·A(1) cycle clears the memory writing and reading address registers at S1 and sets the front panel MB output. The Q response is suppressed each time the memory is full or not accessible.

Data block transfer from the memory to the DATABUS is triggered by F(25)A(0+1). The Q response to this function is suppressed if data transfer cannot be executed and during the block transfer. The DATABUS block transfer is sequential and the memory reading address is incremented at the end of each word transfer by the DATABUS CSYN response. At the end of the block transfer the front panel MB output is released.

- CAMAC MEMORY READOUT : FR

FR is patch selectable among F(0), F(1), F(2) or F(3)

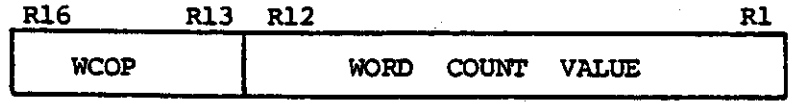
a) DESTRUCTIVE READOUT : FR·A(0)

In this mode the CAMAC data readout proceeds sequentially and the memory reading address is incremented at the end of each FR·A(0) cycle. The Q response is maintained until the last word in the data block has been readout. Q is suppressed each time the memory is empty or not accessible. At the end of the block transfer readout the front panel MB output is released.

b) NON DESTRUCTIVE READOUT : FR·A(1)

Identical as aboye. In addition, a new data block readout can be reinitiated by F(11)A(1)S2. This function clears the memory reading address register. The memory data is protected and access to the memory is prevented until a F(11)A(0)S2 or any other valid memory clear function is applied to the Interface. The Q response is maintained until the last word in the data block has been readout and reinitialised by F(11)A(0)S2. When the memory clear function is received the front panel MB output is released.

The number of data word stored in the memory is registered in the memory writing address register which can be readout to determine the number of word to be transferred in the data block readout. The readout of the WORD COUNT can be enabled with the side panel RWC switch. The WORD COUNT is always readout first and has the following format:




The four most significant bits can be hard wire programmed via the side panel WORD COUNT OPTIONAL PATTERN switches.

- MEMORY ACCESS OPTIONS

The three MEMORY CONTENT PROTECTION switches are accessible on the side panel.

a) SINGLE BLOCK READ : SBR switch

Prevent memory access from the DATABUS as long as the precedent DATABUS data block contents in the memory has not been readout by CAMAC, or cleared.

b) DATABUS OVERWRITE PROTECTION : DOP switch

Prevent memory access from the DATABUS as long as the data written from CAMAC into the memory has not been transferred to the DATABUS, or cleared.

c) CAMAC OVERWRITE PROTECTION : COP switch

Prevent memory access from the CAMAC as long as the data written from the DATABUS into the memory has not been readout by CAMAC, or cleared.

- MEMORY BUSY : front panel MB output

When the memory is being accessed or contents data the front panel LED MB is on and a DC NIM level is present at the two MB output connectors. These two connectors are bridged to permit easy ORing of the MEMORY BUSY signals. The MEMORY BUSY is set by the first CAMAC memory writing cycle or each time a DATABUS GRANT is actived in response to a REQuest. It is clear when the memory is empty or cleared.

- LOOK AT ME : CAMAC LAM

CAMAC LAM can be set either by a DC level or a pulse on the DATABUS LR line. An LR pulse is memorised by the LAM memory. If the CAMAC L line is activated a front panel LED LR is turned on. An Q response is generated in recognition of F(8)A(0+1) or F(10)A(0+1) if CAMAC L line is activated. The LAM memory is cleared by F(10)A(0+1)S2 or the memory clear functions.

The operating mode of the LAM circuit can be selected with the side panel CLEAR LAM switch.

a) LMD position (LAM Memory Disable)

In this position the LAM memory is disabled. Reset is possible with an action on the dedicated crate controller only.

b) FWR position (First Word Reset)

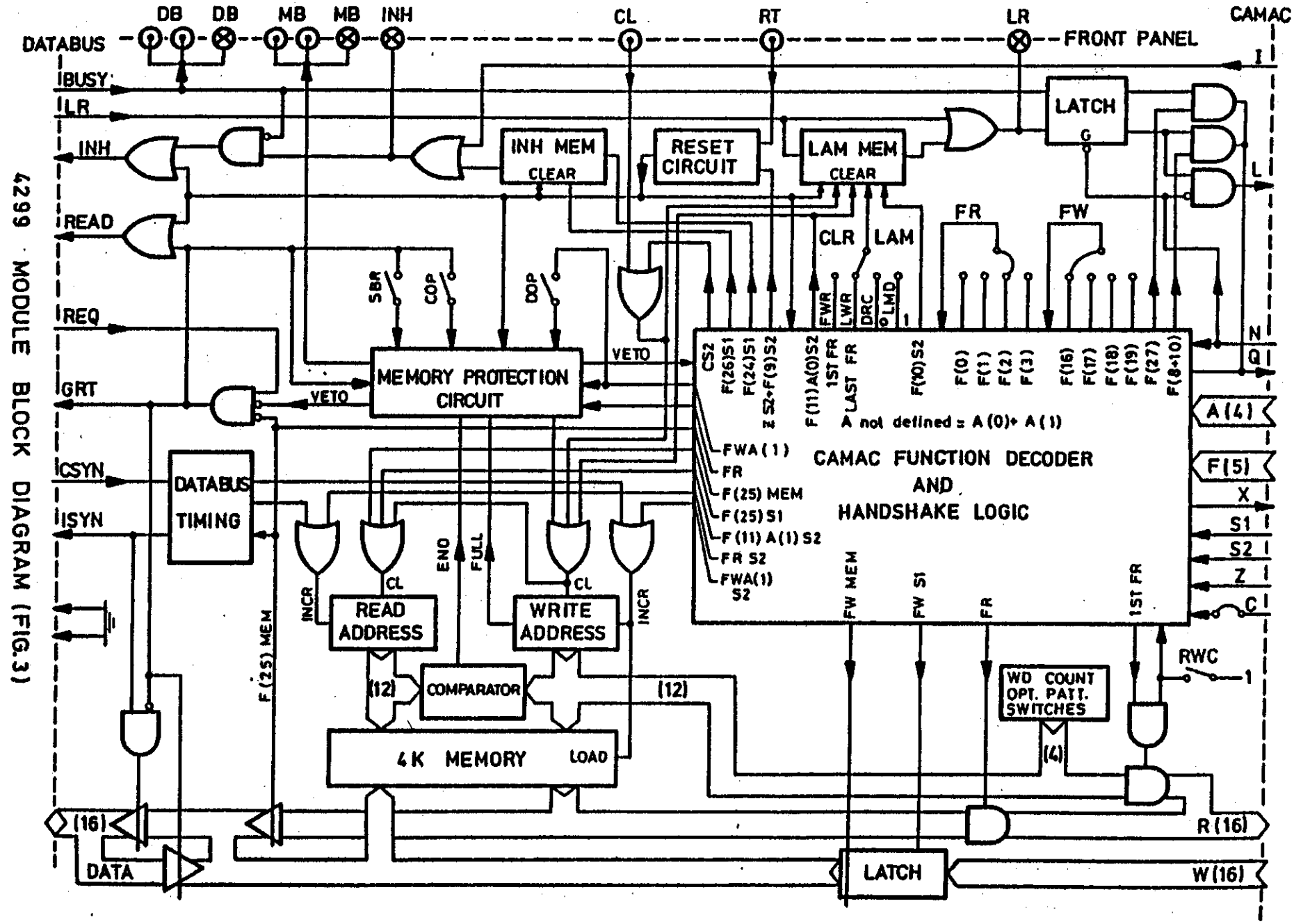
The LAM memory is reset at the end of the first FR·A(0+1) memory readout cycle or by a valid clear function.

c) LWR position (Last Word Reset)

The LAM memory is reset at the end of the last FR·A(0+1) memory readout cycle or by a valid clear function.

d) DRC position (Disable Readout Clear)

The LAM memory is not automatically reset by the memory readout function but by a valid clear function.


DATABUS
DB
DB
MB
MB
INH
CL
RT
LR
CAMAC
FRONT PANEL
IBUSY
LR
INH
READ
REQ
GRT
CSYN
ISYN
LATCH
INH MEM
CLEAR
RESET
CIRCUIT
LAM MEM
CLEAR
CLR
LAM
FR
FW
SBR
COP
DOP
VETO
MEMORY PROTECTION
CIRCUIT
CAMAC FUNCTION DECODER
AND
HANDSHAKE LOGIC
FWA(1)
FR
F(25) MEM
F(25) S1
F(11) A(1) S2
FR S2
FWA(1)
S2
A not defined = A(0)+ A(1)
DATABUS
TIMING
INCR
CL
READ
ADDRESS
WRITE
ADDRESS
END
FULL
F(25) MEM
(12)
COMPARATOR
4K MEMORY
LOAD
WD COUNT
OPT. PATT.
SWITCHES
RWC
(4)
(16)
DATA
R(16)
W(16)
4299 MODULE BLOCK DIAGRAM (FIG.3)

# SPECIFICATIONS

## INPUTS

General :

Front panel connectors Fischer type DLP101A004
Requires NIM - level signal
0 level : 0 mA ± 2 mA
1 level : 16 mA ± 2 mA
Impedance : 50 ohms ± 5%
Direct coupled
Not protected, max. ± 3V
Reflection : <10% for input pulse of 2 ns risetime

RT :

Reset, one, resets all registers and memory, sets an initialised cycle on the DATABUS.
This function has priority over other functions.
Minimum width 20 ns.

CL :

Clear, one, clears the memory and the LAM memory.
This function has priority over the data transfers.
Minimum width 50 ns.

## OUTPUTS

General :

Front panel connectors Fischer type DLP101A004
High impedance current source. Bridge outputs.
NIM levels into 25 ohms.
0 level : 0 mA
1 level : 32 mA ± 2 mA
Maximum amplitude : - 1 V
Rise and fall times : 2.5 ns
Maximum overshoot : 10%
Not protected

MB :

Memory Busy signal. Indicates that the memory contains data or is being accessed.
MB is setted by N·FW·A1·S1 or REQ DATABUS signal and resetted when the memory is empty or cleared.
A front panel MB LED indicates that the MB output is activated.

DB :

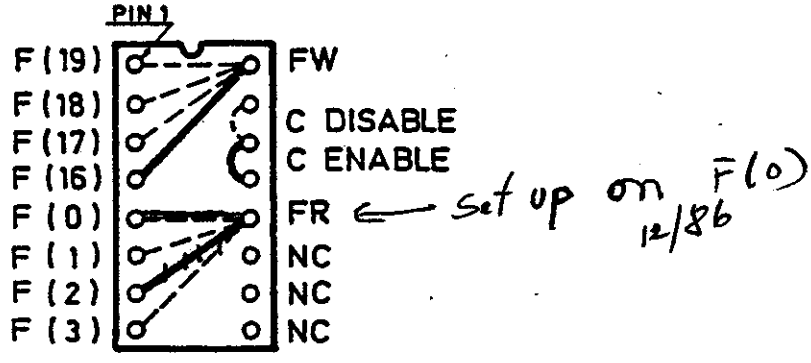
Databus Busy signal. Indicates that the DATABUS BUSY line is activated.
A front panel DB LED indicates that the DB output is activated.

## CAMAC COMMANDS

The FR memory reading function is patch selectable among F(0), F(1), F(2) or F(3). The X and Q responses are generated for the selected read function only.
The FW writing function is patch selectable among F(16), F(17), F(18) or F(19). The X and Q response are generated for the selected write function only.
The CAMAC C line must be disconnected by a bridge.
This module is normally supplied with FR connected on F(2), FW on F(16) and C connected.

- CAMAC FR, FW and C bridges :

Potting base located on printed circuit board at C2 station.




| | |
|---|---|
| Z·S2 | Clears memory, initialises logic status of the unit and generates initialised cycle on the DATABUS. Same function of the front panel RT input. It has priority over other functions. |
| C·S2 | Bridge option, clears memory and LAM memory. Same function of the front panel CL input. It has priority over the data transfers. |
| I | Activates DATABUS INH line and front panel INH LED. The DATABUS INH line command is closed during the DATABUS BUSY. |
| L | LAM signal, is activated by a DC level on the DATABUS LR line or by the LAM memory. The front panel LR LED is activated. If N address is received the L request is suppressed. |
| X | An X-response is always generated when a valid N·A·F command is recognised. |

| | |
|---|---|
| Q | A Q-response is generated only for test status functions or if the requested function can be executed. To prevent a Q-response reading status error, it cannot be changed during the function or if the N address is not released. |
| N·FR·A(0) | Memory destructive reading function. The memory address is incremented at the end of S2.<br>The Q-response is maintained until the last word in the data block has been readout and suppressed each time the memory is empty or being accessed.<br>The LAM memory is cleared at S2 by the first reading cycle if the CLEAR LAM switch is in FWR position or by the last cycle if in LWR position. |
| N·FR·A(1) | Memory non destructive reading function. The memory address is incremented at the end of S2.<br>The Q-response is maintained until the last word in the data block has been readout and suppressed each time the memory is empty or being accessed.<br>A new data block readout can be reinitiated by N·F(11)·A(1).<br>The memory data is protected and access to the memory is prevented until a N·F(11)A(0) or any other valid clear function is applied.<br>The LAM memory is cleared at S2 by the first reading cycle if the CLEAR LAM switch is in FWR position or by the last cycle if in LWR position. |
| N·F(8)·A(0+1) | Tests LAM. A Q-response is generated only if LAM is present. |
| N·F(9)·A(0+1) | Clears memory, initialises logic status of the unit and generates initialised cycle on the DATABUS and a Q-response.<br>Same function of the front panel RT input.<br>It has priority over other functions. |
| N·F(10)·A(0+1) | Tests LAM. A Q-response is generated only if LAM is present.<br>Clears the LAM memory at S2 if the CLEAR LAM switch is not in LMD position. |
| N·F(11)·A(0) | Clears memory if any DATABUS transfer cycle is activated.<br>A Q-response is generated if the clear memory may be executed. |
| N·F(11)·A(1) | Initialise memory address counter for a new datablock readout if any DATABUS transfer cycle is activated.<br>A Q-response is generated if this initialisation may be executed. |
| N·FW·A(0) | DATABUS writing function. With this function the memory is not used and data word are memorised at S1 and transmitted one at a time from CAMAC to the DATABUS.<br>A Q-response is generated if the DATABUS is free. |

| | |
|---|---|
| N·FW·A(1) | Memory writing function. The data are memorised at S1 and loaded in the memory at S2 and the memory address is incremented at the end of S2.<br>The first memory writing cycle clears at S1 the memory address and sets the front panel MB output.<br>The Q-response is suppressed each time the memory is full or being accessed from the DATABUS. |
| N·F(24)·A(0+1) | Sets DATABUS INH line if the DATABUS BUSY line is not activated.<br>A Q-response is always generated. |
| N·F(25)·A(0+1) | Triggers the data block transfer from the memory to the DATABUS.<br>The Q-response is generated only if the data transfer can be executed and suppressed if the memory is being accessed from the DATABUS. |
| N·F(26)·A(0+1) | Resets DATABUS INH line.<br>A Q-response is always generated. |
| N·F(27)·A(0+1) | Tests DATABUS BUSY line.<br>A Q-response is generated only if the DATABUS BUSY signal is present. |
| R1 to R16 | 16 data read lines. |
| W1 to W16 | 16 data write lines. |

POWER REQUIREMENT

+ 6V : < 2A
- 6V : 200 mA

Power : 13 W

PACKAGING RF shielded # 1 CAMAC module.

## OPTIONAL ACCESSORIES

DATABUS cable for connection between 4299 and controller :

LeCroy type DAT - DO / 50 - LL

LL : length of cable in feet (max. 100 feet).

(Cable mounted with two 3M 3425-6050 connectors and 3M 3302-50 color coded ribbon cable).

DATABUS extension cable for length ≥100 feet :

LeCroy type DAE - DO / 50 - LL

LL : length of cable in feet / 10.

(Cable mounted with two 3M 3433-1302 connectors and 25 twisted pairs round cable).

Two DAT-DO/50-LL cable must be used to connect this extension cable.

DATABUS cable for connection between controllers or between controller and terminator :

LeCroy type DAT - DI / 50 - LL

LL : length of cable in feet (max. 100 feet).

(Cable mounted with two 3M 3425-6050 connectors and 3M 3302-50 color coded ribbon cable).

DATABUS terminator :

LeCroy type DAT - TR / 50

(Terminator equipped with a 3M 3433-1302 connector).

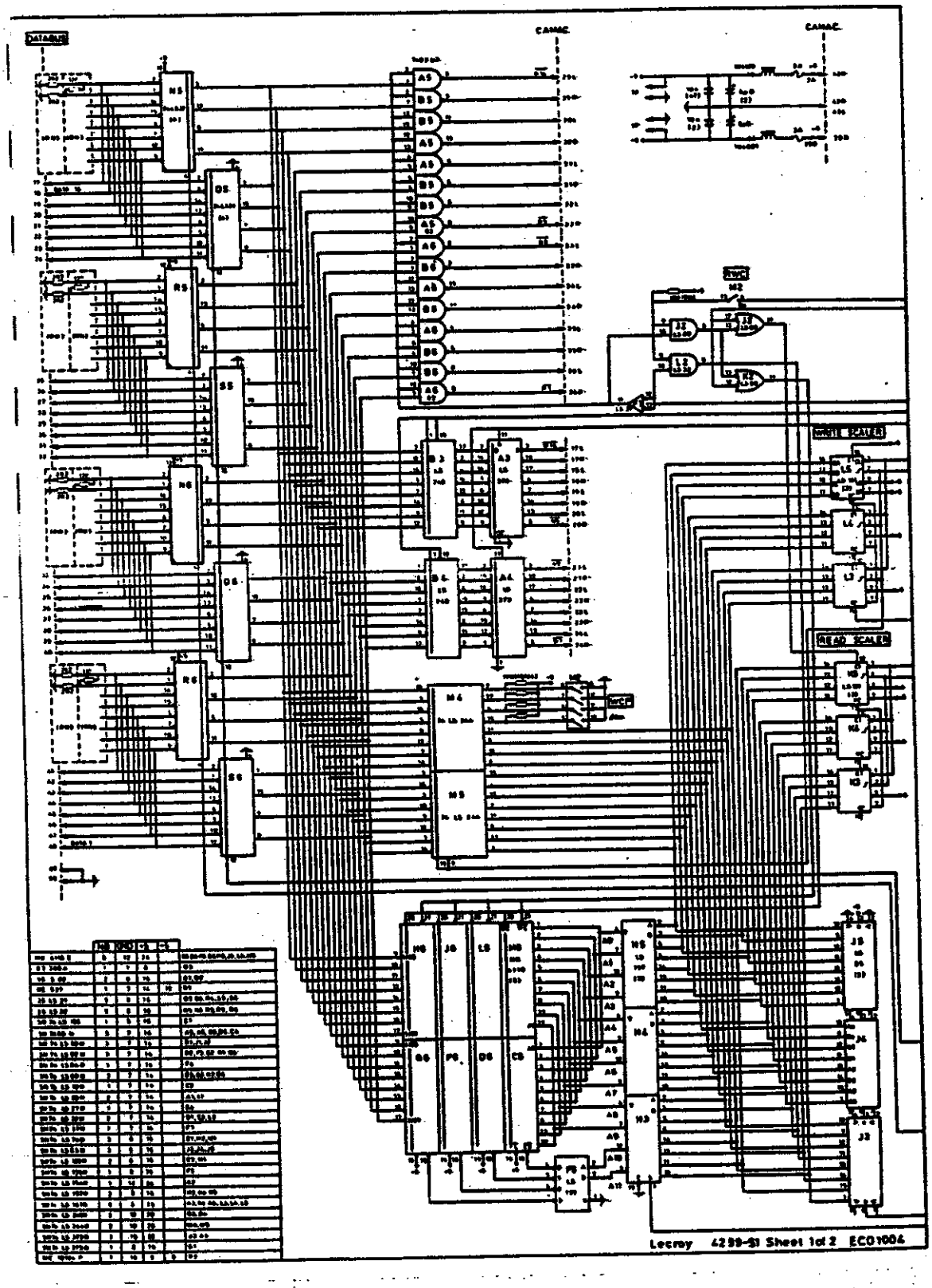
A DAT-DI/50-LL cable must be used for connecting this terminator.

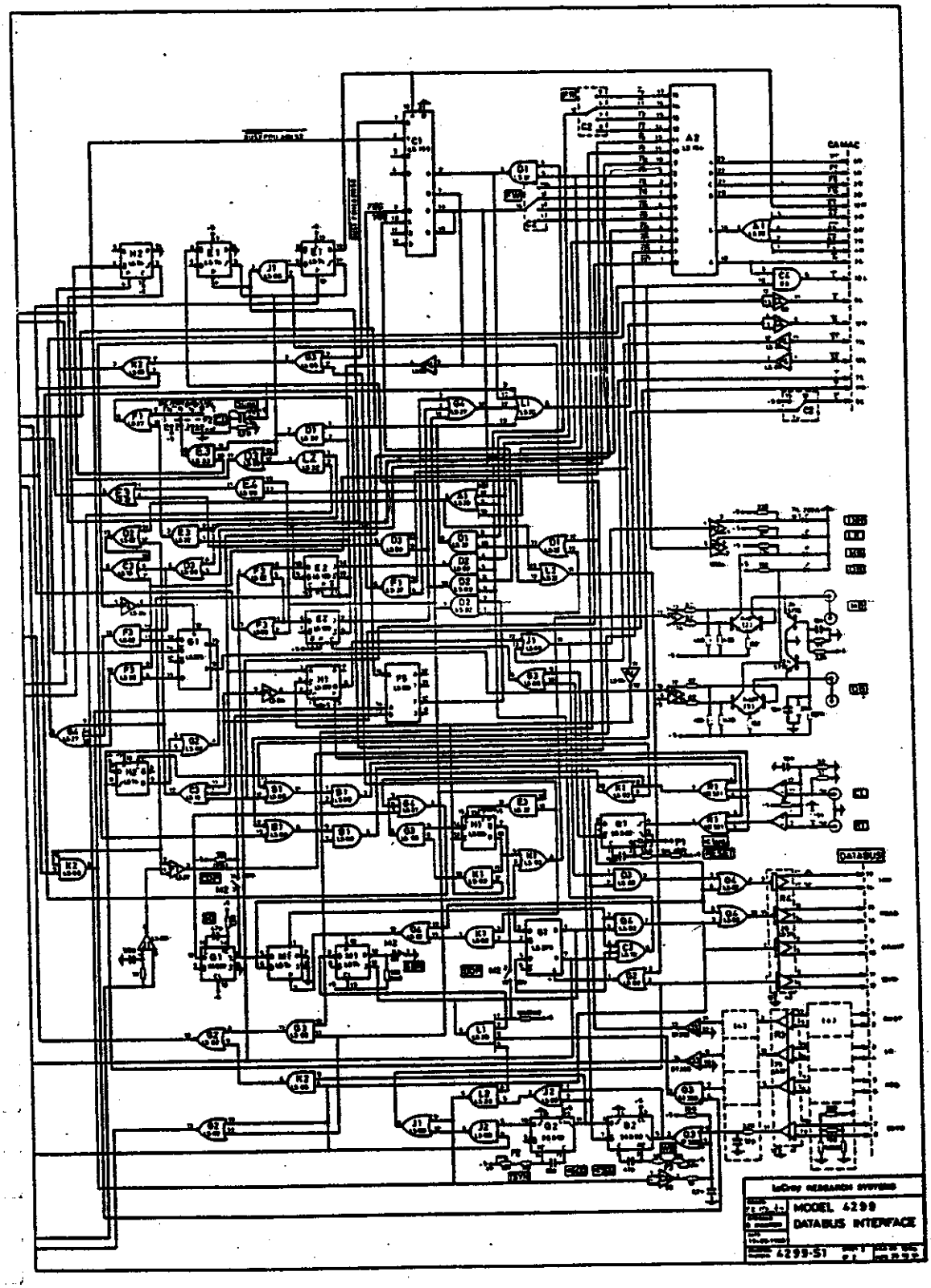
Necessary only for DATABUS cable > 300 feet.

MODEL NO 4299 DATA BUS INTERFACE
LAST REVISION NO 1003 REVISION DATE 14-Apr-01

| | | | | |
|---|---|---|---|---|
| 102 | 412 | 120 | CAP CERA DISC 100V 12 PF | 4 |
| 102 | 412 | 121 | CAP CERA DISC 100V 120 PF | 1 |
| 102 | 412 | 151 | CAP CERA DISC 100V 150 PF | 1 |
| 102 | 412 | 470 | CAP CERA DISC 100V 47 PF | 3 |
| 102 | 412 | 680 | CAP CERA DISC 100V 68 PF | 1 |
| 103 | 317 | 222 | CAP CERA MONO 50V 2200 PF | 1 |
| 103 | 327 | 103 | CAP CERA MONO 50V .01 UF | 52 |
| 142 | 824 | 685 | CAP TANT DIP CASE 6.8 UF | 3 |
| 161 | 335 | 102 | RES COMP 1/4W 5% 1 K | 3 |
| 161 | 335 | 151 | RES COMP 1/4W 5% 150 OHMS | 10 |
| 161 | 335 | 152 | RES COMP 1/4W 5% 1.5 K | 3 |
| 161 | 335 | 181 | RES COMP 1/4W 5% 180 OHMS | 4 |
| 161 | 335 | 222 | RES COMP 1/4W 5% 2.2 K | 9 |
| 161 | 335 | 301 | RES COMP 1/4W 5% 300 OHMS | 4 |
| 161 | 335 | 331 | RES COMP 1/4W 5% 330 OHMS | 2 |
| 161 | 335 | 393 | RES COMP 1/4W 5% 39 K | 1 |
| 161 | 335 | 431 | RES COMP 1/4W 5% 430 OHMS | 4 |
| 161 | 335 | 510 | RES COMP 1/4W 5% 51 OHMS | 4 |
| 161 | 335 | 820 | RES COMP 1/4W 5% 82 OHMS | 7 |
| 181 | 457 | 103 | RES VARI CERMET 10 K | 3 |
| 190 | *42 | 103 | RESISTOR NETWORK 10 K | 1 |
| 190 | *42 | 222 | RESISTOR NETWORK 2.2 K | 2 |
| 190 | 832 | 121 | RESISTOR NETWORK 120 OHMS | 4 |
| 190 | 842 | 222 | RESISTOR NETWORK 2.2 K | 2 |
| 200 | *31 | *28 | IC 2-IN NAND GT SN74LS00N | 3 |
| 200 | *31 | *33 | IC 2-IN NAND GATE SN7403N | 5 |
| 200 | *31 | *46 | IC HEX INVERTER SN74LS04N | 1 |
| 200 | *31 | *47 | IC 3-IN NAND GT SN74LS10N | 1 |
| 200 | *31 | *48 | IC 4-IN NAND GT SN74LS20N | 2 |
| 200 | *31 | *49 | IC FLIP-FLOP SN74LS74N | 3 |
| 200 | *31 | *51 | IC 2-IN NOR GT SN74LS02N | 5 |
| 200 | *31 | *57 | IC 3-IN POS NOR SN74LS27N | 1 |
| 200 | *31 | *73 | IC 2-IN POS OR SN74LS32N | 3 |
| 200 | *31 | *74 | IC POS-NAND BUF SN74LS37N | 1 |
| 200 | *31 | *86 | IC 2-IN AND GAT SN74LS08N | 4 |
| 200 | *31 | 380 | IC QUAD BUS RECVR DS8836N | 1 |
| 200 | *41 | *26 | IC 4-BIT CTR SN74LS161N | 6 |
| 200 | *41 | *27 | IC QUAD SEL/MP SN74LS157N | 3 |
| 200 | *41 | *43 | IC 4-BIT MAGNIT SN74LS85N | 3 |
| 200 | *41 | *66 | IC FLIP-FLOP SN74LS109N | 2 |
| 200 | *41 | 139 | IC DEC/MULTIPL SN74LS139N | 1 |
| 200 | *41 | 155 | IC DEC/DEMULTIPL 74LS155N | 1 |
| 200 | *41 | 375 | IC 4-BIT LATCH SN74LS375N | 1 |
| 200 | *42 | **5 | IC MULTIVIBRATOR 96S02PC | 2 |
| 200 | *71 | **1 | IC OCTL BUFFER AM25LS240A | 2 |
| 200 | *71 | **7 | IC OCTAL BUFF SN74LS244N | 2 |
| 200 | *71 | 373 | IC OCTAL LATCH SN74LS373N | 2 |
| 200 | *81 | **4 | IC DECODER/DEM DM74LS154N | 1 |
| 200 | 141 | *31 | IC DIFF LINE DRV AM26LS31 | 5 |
| 200 | 141 | *32 | IC DIFF LINE REC AM26LS32 | 5 |

| | | | | | |
|---|---|---|---|---|---|
| 204 | *42 | **7 | IC QUAD TRANSL | MC10124P | 1 |
| 206 | *52 | 182 | IC 1024X8 RAM | MK4118-2 | 8 |
| 208 | *31 | **3 | IC VOLT COMPARATOR | NE521A | 1 |
| 235 | *10 | **5 | DIODE RECTIFIER | 1N4005 | 1 |
| 235 | *50 | **1 | DIODE RECTIFIER | 1N4139 | 1 |
| 256 | 233 | 209 | DIODE LED (RED) | TIL209A | 4 |
| 270 | 130 | 401 | TRANSISTOR NPN | A401 | 4 |
| 270 | 170 | **1 | TRANSISTOR NPN | 2N5770 | 2 |
| 300 | *50 | **1 | CHOKE FERRITE SINGLE LEAD | | 2 |
| 400 | *20 | *14 | SOCKET IC ST | DIP-14 | 31 |
| 400 | *30 | *16 | SOCKET IC ST | DIP-16 | 31 |
| 400 | *40 | *24 | SOCKET IC ST | DIP-24 | 9 |
| 400 | 170 | *20 | SOCKET IC ST | DIP-20 | 6 |
| 402 | 130 | **1 | CONN LEMO RT ANGLE PC MTG | | 6 |
| 403 | 170 | *50 | HEADER RT ANGLE ST | 50-PIN | 1 |
| 403 | 211 | *50 | CONN FLAT CABLE | 50-POS | 2 |
| 403 | 950 | **2 | POLARIZING KEY | | 2 |
| 411 | 851 | **1 | SWICH ROCKER PC MTG | SPST | 1 |
| 419 | 244 | **1 | SWITCH SLIDE | DIP-16 | 1 |
| 433 | 220 | **2 | FUSE SUB-MINI | 3 AMP | 2 |
| 454 | 310 | **2 | HDR DIP SOLD TO PC BD | 2 | 2 |
| 521 | 440 | **9 | SPACER HEX | 4-40X9/32 | 4 |
| 528 | *55 | *16 | PLUG(POTTING BASE) DIP- | 16 | 1 |
| 540 | 203 | **1 | SIDE COVER CAMAC STD(LIP) | | 1 |
| 540 | 206 | **1 | RAIL | CAMAC STANDARD | 2 |
| 540 | 209 | **1 | REAR PANEL CAMAC SIZE | #1 | 1 |
| 555 | 430 | **3 | CAPTIVE SCREW ASSEMBLY | | 1 |
| 560 | 440 | **2 | SCREW PHILIPS | 4-40X1/8 | 4 |
| 560 | 440 | **3 | SCREW PHILIPS | 4-40X3/16 | 4 |
| 560 | 440 | **5 | SCREW PHILIPS | 4-40X5/16 | 6 |
| 560 | 440 | **6 | SCREW PHILIPS | 4-40X3/8 | 2 |
| 564 | 440 | **4 | SCREW ROUND PHIL | 4-40X1/4 | 2 |
| 592 | *30 | *50 | CABLE FLAT AWG 28 | 50-COND | 15 |
| 714 | 299 | **3 | PC BD PREASS'Y | 4299 | 1 |
| 724 | 299 | **3 | FRONT PNL PREASS'Y | 4299 | 1 |
| 734 | 299 | **3 | SIDE CAMAC LEFT | 4299 | 1 |


DATABUS
CAMAC
CAMAC
WRITE SCALER
READ SCALER
Lecroy 4299-91 Sheet 1of 2 ECO1004


MODEL 4299
DATABUS INTERFACE
4299-S1