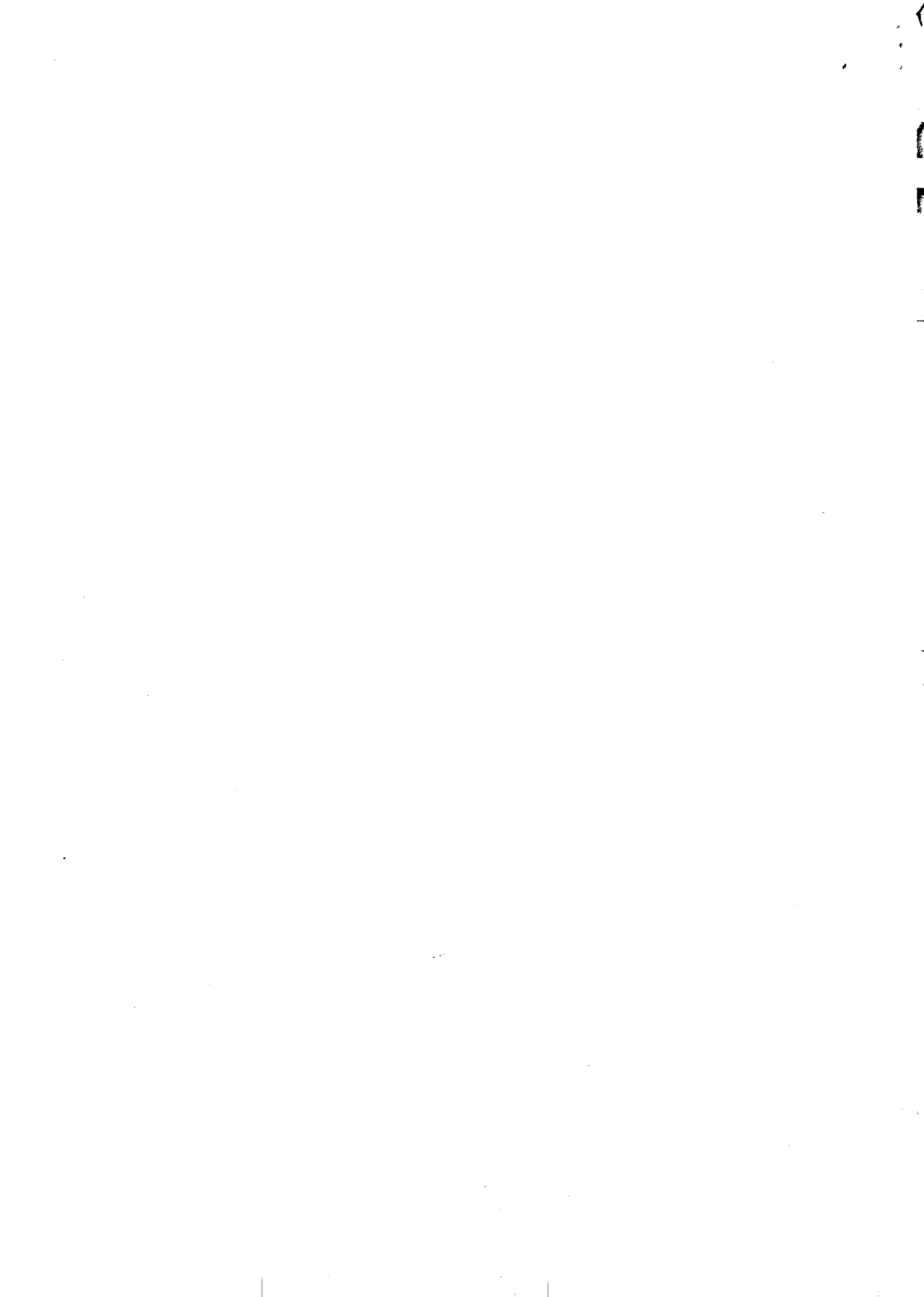


CAMAC MODEL 4434
32-CHANNEL, 24-BIT SCALER
USER'S MANUAL

November 1982



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ATTENTION

CRATE POWER SHOULD BE TURNED OFF DURING INSERTION AND REMOVAL OF THE UNIT TO
AVOID POSSIBLE DAMAGE CAUSED BY MOMENTARY MISALIGNMENT OF CONTACTS.

SEE POCKET IN BACK IF MANUAL FOR SCHEMATICS, PARTS LISTS AND ADDITIONAL ADDENDA
WITH ANY CHANGES TO MANUAL.

ATTENTION



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CAMAC ECLine Model 4434 32 Channel 24-Bit Latching Scaler

- **High Density:** 32 Scalers, 24 bit each, in a single width CAMAC Module
- **Auxiliary Bus Output:** for interconnection with external raster scan display
- **Medium Counting Rate:** 20 MHz
- **Input Levels:** complementary ECL or single ended TTL
- **Common Load, Common Clear, Common Veto:** on the Front Panel or via CAMAC Command
- **LAM Generation**
- **Sequential or addressed readout**

The new generation of high energy physics experiments, involving extremely high counting rates and/or large detector arrays, requires a "total system" approach to instrumentation. LeCroy's new CAMAC 4000 Series of ultra-fast, high-density programmable instrumentation modules provides the solution to this requirement by allowing the experimenter to achieve full computer control of the data acquisition system within a single instrumentation standard.

The LeCroy Model 4434 contains 32 channels of 24-bit scalers. Through the extensive use of LeCroy custom built hybrid circuits, the Model 4434 achieves a dramatic increase in channel density with a very low overall cost per channel.

Each channel is identical and is followed by an internal buffer which may be used to store and readout accumulated data independent of data acquisition.

Inputs to the 4434 are complementary ECL levels compatible with all ECLine modules. Single ended TTL levels are available as a factory option. Each scaler counts signals which have a duration > 10 nsec and a maximum frequency of 20 MHz, assuming the module is not disabled by either the front panel veto or CAMAC Inhibit. However, a local double pulse resolution of 30 nsec is permitted. Receipt of a CAMAC or front panel Load command temporarily halts the scalers and transfers the contents to the internal buffer memory. The scalers may then be optionally cleared before counting is resumed.

Memory readout may take place at any time, independent of data acquisition, under standard CAMAC or Auxiliary Data Bus control. In either case, readout can be performed both sequentially or randomly.

The Auxiliary Bus organization is designed to permit connection of up to 16 modules to the same bus.

October 1982

Innovators in Instrumentation



SPECIFICATIONS

CAMAC ECLine Model 4434

32 CHANNEL 24-BIT LATCHING SCALER

INPUT CHARACTERISTICS

Signal Inputs:	32, in two 2 × 17-pin front panel connectors, BERG 7578D-101-34.
Input Levels:	Differential ECL (Factory option is available to accept TTL single-ended inputs with the scaler incrementing on the negative going transition).
Input Impedance:	110 Ω pin-to-pin with differential ECL, 560 Ω to +5 V for TTL single-ended inputs.
Input Pulse Width:	10 nsec minimum.
Double Pulse Resolution:	Less than 30 nsec.
Maximum Frequency:	> 20 MHz.
Maximum Instantaneous Rate:	> 30 MHz.

COMMAND INPUTS

General:	The LOAD, CLEAR and VETO inputs each have a single front panel Lemo-type connector; a common side-switch selects either negative going NIM or TTL levels, input impedance 50 Ω for NIM pulses; 50 Ω AC and 100 Ω DC to +5 V for TTL pulses.
Load Input:	A LOAD pulse with > 10 nsec width will disable inputs for 220 nsec and shift the scaler contents into a 32-word × 24-bit buffer; the LOAD command can optionally generate a LAM on the CAMAC dataway and also prepare the memory for readout by loading the starting subaddress (FA) and readout number (RN) previously defined by a CAMAC F(16) or Z; a front panel LED (RDE, Readout Enabled) is lit in recognition of a Load command.
Clear Input:	A CLEAR pulse with > 20 nsec width will disable inputs for a duration of approximately 100 nsec and clear the 32 scalers.
Veto Input:	Disables inputs for the duration of the VETO (action identical to CAMAC INHIBIT).

CAMAC COMMANDS AND FUNCTIONS

Note:	The following notation is used in this section: CR: Command Register; loaded by F(16) FA: First Address to be read RN: Readout Number; defines how many channels (minus one) have to be read in the module.
Z:	Initialize the unit at S2, i.e. all scalers, buffer and LAM are cleared as well as register CR.
C:	Clear all scalers at S2.
I:	All scaler inputs are inhibited during CAMAC INHIBIT command; the action is identical to that of the front panel VETO input.
X:	A X = 1 response is generated in recognition of any valid function.
Q:	A Q = 1 response is generated in recognition of any executable function.
L:	A Look-At-Me signal can be generated according to several possible options described in the "Option Switches" section below.
N•F(0)•A(0):	Generates readout of the selected channel; F(0) can be executed and a Q = 1 response will be provided under the following conditions: a) Side switch LAD (Latching Disable) = ON: always if the LED RDE (Readout Enabled) is ON. b) Side switch LAD = OFF: only after a LOAD has been performed and as long as the readout of the given number of channels had not been completed.
N•F(2)•A(0):	Sequential data readout with auto-increment of the address; F(2) can be executed and a Q = 1 response will be provided independent of the Latching Disable switch position, if a LOAD has been previously performed, and as long as the readout of the given number of channels has not yet been completed. Note: if the number of scalers to be read is RN + 1 > 32-FA then the readout, after address 31, will continue with addresses 0, 1, 2, etc. until RN + 1 channels have been read.

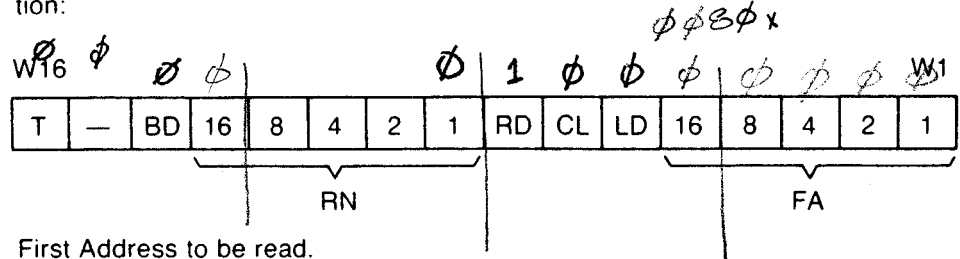
N•F(8)•(0):
N•F(10)•A(0):

Test LAM: Q = 1 response is generated when LAM is ON.
Test and clear LAM; a Q = 1 response is generated when LAM is ON. LAM is cleared at S2.
Note: LAM goes on again after F(10) in the following cases:
a) Switch LOF (LAM at Overflow) = ON and scaler not cleared.
b) Switch LDR (LAM Data Ready) = ON and data readout not finished.
Load register CR (Command Register); F(16) can always be executed and a Q = 1 response is generated.

N•F(16)•A(0):

The Command Register is a 16 bit word with the following format and explanation:

*Read ch 1
no clear*



FA: First Address to be read.
RN: Readout Number; defines how many channels (minus one) have to be read starting from the address FA; after a Z command, RN is set to 31 and FA to 0.
T: Test; when T = 1 permanently inhibits signal inputs; increments at S2 all scalers by one count; after a Z command T = 0.
LD: Load; LD = 1 performs a load if switch LAD (Latching Disable) = OFF; after 0.8 μ sec the module will be ready for readout; enables functions F(0) and F(2).
CL: Clear; CL = 1 clears all the 32 scalers.
RD: Readout enable; RD = 1 prepares the module for readout, does not require a LOAD; readout can be started after 0.8 μ sec.
BD: Bus Disable; BD = 1 disables the Auxiliary Bus readout; after a Z command BD = 0.

OPTION SWITCHES

A set of side accessible switches allows the user to select different options as follows:
LAD: Latching Disable; when ON the module works as a normal non-latching scaler.
OVF: Overflow decides whether an overflow condition occurs when bit 16 of any scaler is ON or when bit 24 is ON.
LCO: Load and Clear at Overflow when ON.
LOF: LAM at Overflow; a LAM is generated when at least one channel reaches the overflow set value.
LRE: LAM at Readout Enable; a LAM is generated after a readout request.
LDR: LAM Data Ready; a LAM is generated after a readout request and as long as there are data to be read.
BAD: 4-bit Bus Address; defines module address in the auxiliary bus.
VBR: Veto by Bus Readout; enables a veto of all scaler inputs during the loading of the auxiliary bus output registers (< 200 nsec).
NIM/TTL: Decides pulse standard accepted by inputs LOAD, CLEAR and VETO:
NIM: 0 = 0 mA 1 = - 12mA
TTL: 0 = + 2.5 V 1 = + 0.5 V

AUXILIARY BUS

A total of 16 LeCroy Model 4434 Modules may be interfaced to an auxiliary bus via a front panel 34-pin connector. The auxiliary bus must end in an independent dedicated controller. Use of the auxiliary bus permits addressed readout of the scaler contents independent of CAMAC operations for applications such as raster scan display.

GENERAL

Packaging: Single width CAMAC standard module.
Power Consumption: TTL-Version ECL-Version
+ 6 V 2.8 A 3.1 A
- 6 V 40 mA 400 mA

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SECTION 1

OPERATING INSTRUCTIONS

1.2 General

Packaging

Single width CAMAC standard module.

Power Consumption

	<u>TTL Version</u>	<u>ECL Version</u>
+ 6 V	2.8 A	3.1 A
- 6 V	40 m A	400 m A

1.3 Input Characteristics

Signal Inputs: 32, in two 2 x 17-pin front panel connectors, BERG 7578D-101-34.

Input Levels: Differential ECL (factory option is available to accept TTL single-ended inputs with the scaler incrementing on the negative going transition).

Input Impedance: 110 Ω pin-to-pin with differential ECL, 560 Ω to + 5 V for TTL single-ended inputs.

Input Pulse Width: 15 nsec minimum.

Double Pulse Resolution: < 30 nsec.

Maximum Frequency: > 20 MHz.

Maximum Instantaneous Rate: > 30 MHz.

1.4 Command Inputs

General: The LOAD, CLEAR and VETO inputs each have a single front panel Lemo-type connector; a common side-switch selects either negative going NIM or TTL levels, input impedance 50 Ω for NIM pulses; 50 Ω AC and 100 Ω DC to + 5 V for TTL pulses.

- Load Input: A LOAD pulse with > 10 nsec width will disable inputs for 220 nsec and shift the scaler contents into a 32-word x 24-bit buffer; the LOAD command can optionally generate a LAM on the CAMAC dataway and also prepare the memory for readout by loading the starting subaddress (FA) and readout number (RN) previously defined by a CAMAC F(16) or Z; a front panel LED (RDE, Readout Enabled) is lit in recognition of a Load command.
- Clear Input: A CLEAR pulse with > 20 nsec width will disable inputs for a duration of approximately 100 nsec and clear the 32 scalers.
- Veto Input: Disables inputs for the duration of the VETO; see Figure 1.1 (action identical to CAMAC INHIBIT).

1.5 CAMAC Commands and Functions

Note: The following notation is used in this section:

- CR: Command Register; loaded by F(16).
 FA: First Address to be read.
 RN: Readout Number; defines how many channels (minus one) have to be read in the module.
- Z: Initialize the unit at S2, i.e. all scalers, buffer and LAM are cleared as well as register CR; FA is set to 0 and RN is set to 31.
- C: Clear all scalers at S2.
- I: All scaler inputs are inhibited during CAMAC INHIBIT command; the action is identical to that of the front panel VETO input.
- X: An X = 1 response is generated in recognition of any valid function.
- Q: A Q = 1 response is generated in recognition of any executable function.
- L: A Look-At-Me signal can be generated according to several possible options described in the "Option Switches" section below.
- F(0)*A(0): Generates readout of the selected channel; F(0) can be executed and a Q = 1 response will be provided under the following conditions:
- a. Side switch LAD (Latching Disable) = ON: always if RDE (Readout Enabled) is ON.
 - b. Side switch LAD = OFF: only after a LOAD has been performed and as long as the readout of the given number of channels has not been completed.

F(2)*A(0): Sequential data readout with auto-increment of the address; F(2) can be executed and a Q = 1 response will be provided independent of the Latching Disable switch position, if a LOAD has been previously performed, and as long as the readout of the given number of channels has not yet been completed.

Note: if the number of scalars to be read is $RN + 1 > 32 - FA$ then the readout, after address 31, will continue with addresses 0, 1, 2, etc. until $RN + 1$ channels have been read.

F(8)*A(0): Test LAM; Q = 1 response is generated when LAM is ON.

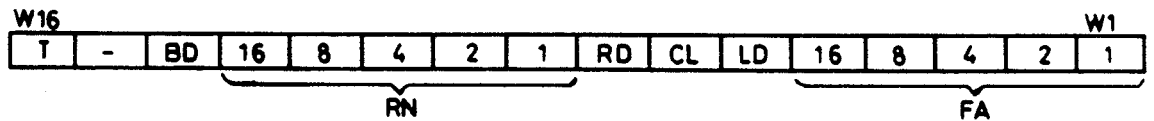
F(10)*A(0): Test and clear LAM; a Q = 1 response is generated when LAM is ON. LAM is cleared at S2.

Note: LAM goes on again after F(10) in the following cases:

- a. Switch LOF (LAM at Overflow) = ON and scaler not cleared.
- b. Switch LDR (LAM Data Ready) = ON and data readout not finished.

F(16)*A(0): Load register CR (Command Register); F(16) can always be executed and a Q = 1 response is generated.

The Command Register is a 16-bit word with the following format and explanation:



All these data, except for the bits LD, CL, RD, are stored in an internal memory at S1 where they will be kept until a new F(16) or a Z command is received.

FA = First Address; gives the address of first channel to be read and can assume values from 0 to 31; the FA value is loaded in an internal Address Counter (AC) automatically incremented by one every time a new channel has been read and therefore defines which channel will be read next; after 31, the AC will continue counting 0, 1, 2, etc. until the given number of channels, RN + 1, has been read; after a Z command, FA is set to 0.

RN = Readout Number, defines how many channels have to be read starting from the first address FA; RN may assume values ranging from 0 to 31, the number of channels read will be RN + 1; this value is automatically loaded in a decrementing counter Read Counter (RC) at the start of a readout sequence; after a Z command RN is set to 31.

LD = Load; LD = 1 performs a Load if switch LAD = OFF; also loads counters AC and RC; after 0.8 μ sec, the module will be ready for readout; enables functions F(0) and F(2).

CL = Clear; CL = 1 clears all the 32 scalers.

RD = Readout enable; RD = 1 prepares the module for readout and does not require a LOAD; readout can be started after 0.8 μ sec; this bit can be used to read data again.

BD = Bus Disable; BD = 1 disables the Auxiliary Bus readout; after a Z command BD = 0.

T = Test; T = 1 inhibits signal inputs; performs increment test on all the 32 channels. For this test the 24 bits of each scaler are considered as three words of eight bits. The three words are all incremented by one (this permits the complete test of the module in only 256 cycles in total).

The bit T is memorized and it will keep a permanent inhibit on the 32 scaler inputs until T is overwritten or a Z command applied; after a Z command T = 0.

To summarize, F(16) can generate the following operation sequences (X = no care):

T	RD	CL	LD	Sequence Generated:
0	0	0	0	Load Command Register (CR) only.
0	X	0	1	Load scaler contents into the internal buffer and start readout.
0	0	1	0	Clear all the 32 scalers.
0	X	1	1	Load scalers into buffer; clear scalers; start a readout.
0	1	0	0	Start a readout without pre-loading.
0	1	1	0	Clear all scalers and start a readout.
1	0	0	0	Inhibit all signal inputs and increment all channels.
1	0	1	0	Inhibit all signal inputs, clear all scalers, and increment all channels.
1	X	0	1	Inhibit all signal inputs, increment all channels by one, load scalers into buffer and start a readout.
1	1	0	0	Inhibit all signal inputs, increment all channels by one and start a readout.
1	X	1	1	Inhibit all signal inputs, increment all channels by one, load buffer, clear scalers and start readout.

1.6 Side Switch Options

A set of switches, accessible on the side of the module, permits the user to select different options as follows:

LAD:	Latching Disable; when LAD = ON the internal buffer becomes transparent so that the Load function is no longer effective and can be used only to start a readout.
OVF:	Overflow; in position 16 (24) an overflow condition occurs when bit 16 (24) scaler is ON (16 or 24 bit half full scale).
LCO:	Load and Clear at Overflow; a Load is automatically generated, followed by a Clear and a start readout, when an overflow occurs.

LOF: LAM at Overflow; a LAM is generated as soon as at least one of the scalers arrives at half full scale; a LAM can be cleared by a Z command or, if the scalers are cleared, by an F(10).

LRE: LAM at Readout Enable; a LAM is generated after a readout request. A LAM can be cleared by a Z command or an F(10).

LDR: LAM Data Ready; a LAM is generated after a readout request and as long as there is data to be read.

BAD: Bus Address; 4 bit, defines the module address on the Auxiliary BUS.

VBR: Veto by Bus Readout; enable a VETO of all scaler inputs during the loading of the BUS output register (< 200 nsec).

NIM/TTL: Sets the standard for pulses accepted by inputs LOAD, CLEAR and VETO:

NIM : 0 = 0 mA; 1 = -12 mA.

TTL : 0 = 2.5 V; 1 = 0.5 V.

1.7 Auxiliary Bus Specifications

General: All BUS lines are in TTL low power Shottky technology, negative logic.

Level 0: > 2 V

Level 1: < 0.8 V

DA 1 to 24: Data and Address lines:

DA 1 to 9

(Address Inputs)

Level 0: < 100 μ A at 5 V

Level 1: < -400 μ A at 0.4 V

DA 1 to 24

(Data Output), Tri-state Output

Level 0: > 3.1 V at -1 mA

Level 1: < 0.4 V at 12 mA

ARY: Address Ready Input: Impedance 6.8 K ohm
(Integration 80 nsec)

DRY: Data Ready Output: Open Collector

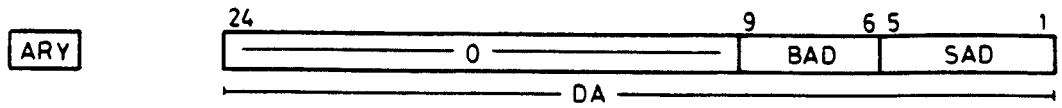
Level 0: < 50 μ A at 5 V

Level 1: < 0.4 V at 16 mA

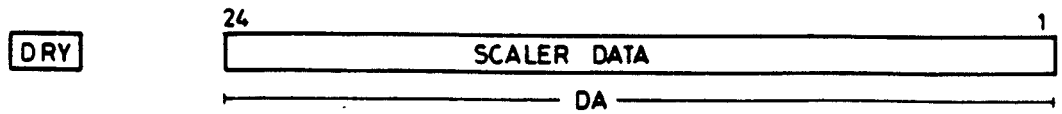
EGD: Enable Ground: Impedance 10 K ohm at +5 V

This line must be grounded by the BUS controller.

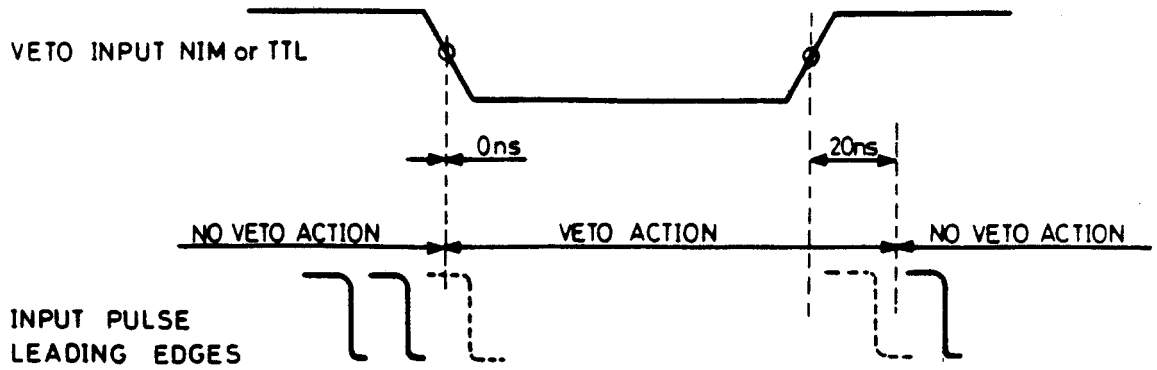
1.8 Address Transfer Structure:



1.9 Data Transfer Structure:



VETO TIMING DIAGRAM



Time measurements made on front panel connectors.

Figure 1.1

AUXILIARY BUS ALLOCATION PINS

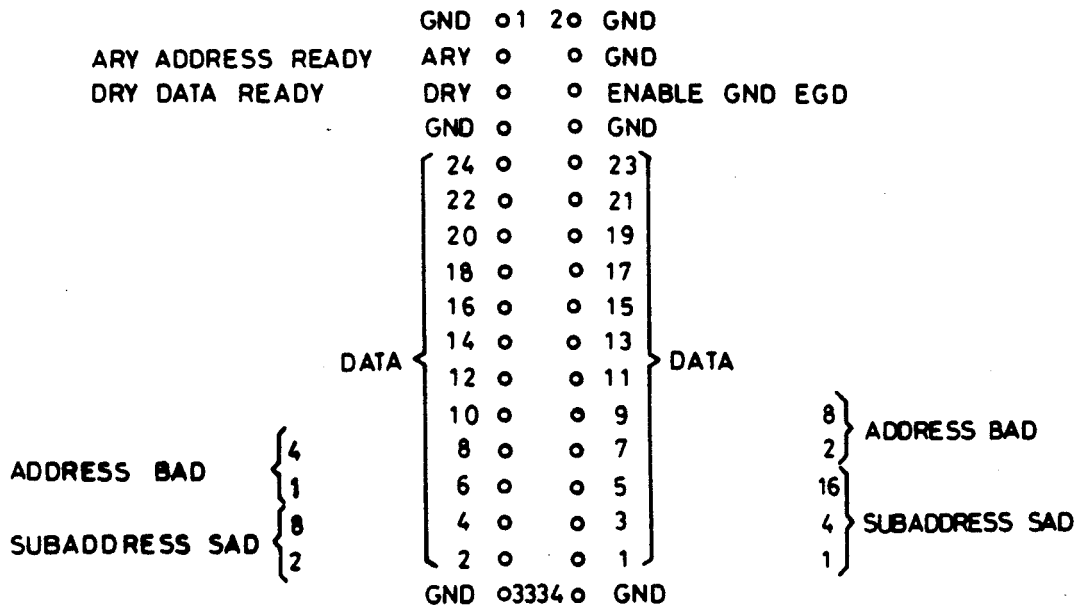
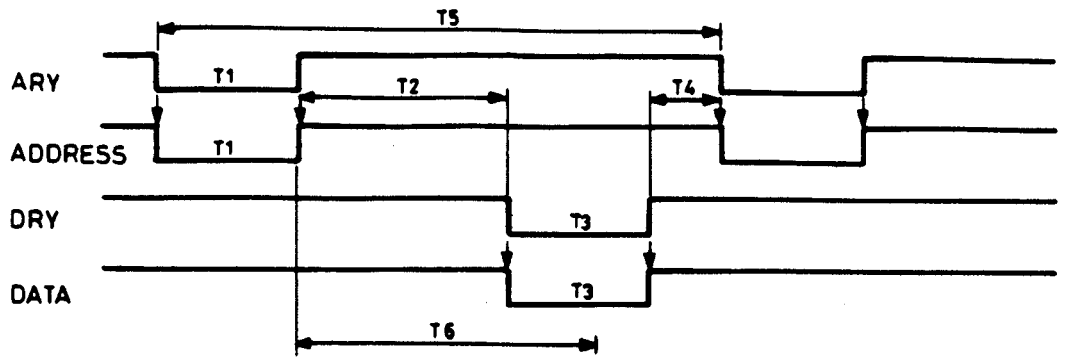


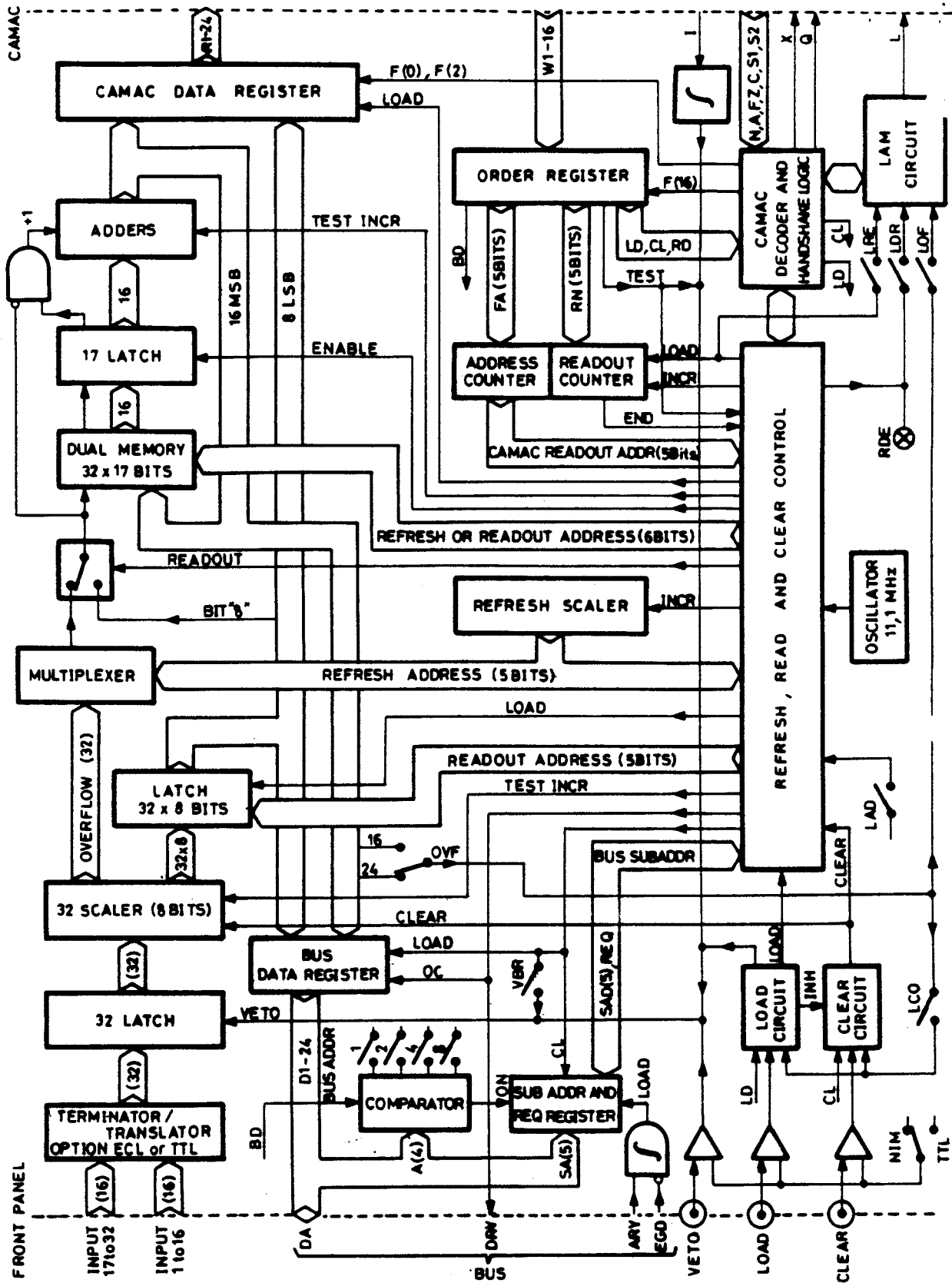
Figure 1.2

AUXILIARY BUS TIMING



- T1: ARY is in phase with ADDRESS; width ≥ 300 nsec
- T2: $500 \text{ nsec} < T2 < 1050 \text{ nsec}$
- T3: DRY is in phase with DATA; width $500 \text{ nsec} \pm 50 \text{ nsec}$
- T4: WAIT TIME $> 0 \text{ nsec}$
- T5: PERIOD $1.3 \mu\text{sec} < T5 < 1.85 \mu\text{sec}$ (frequency $\leq 750 \text{ KHz}$)
- T6: TIME OUT $\geq 1.2 \mu\text{sec}$

Figure 1.3



MODEL 4434 BLOCK DIAGRAM

FIG 1.4

SECTION 2

TECHNICAL DESCRIPTION

In this chapter, information concerning the Model 4434 scaler and simple data acquisition program concepts are presented.

Figure 2.1 shows a functional block diagram for the 4434 user that will be referred to in the following paragraphs (2.1 to 2.4).

2.1 LOAD Scaler Function

This function is performed either by sending an external LOAD signal (NIM or TTL, width greater than 10 nsec) or by F(16)*A(0) with bit W6 = 1.

At the time this function is executed, the following actions occur:

- a. All scaler inputs are inhibited for less than 220 nsec; the inhibit action, with respect to inputs on front panel connectors, starts 30 nsec (typical) to 45 nsec (maximum) after leading edge of input LOAD pulse.
- b. All scaler contents are loaded into a temporary register with 32 words of 24 bits each.
- c. If CAMAC load is given (F(16)*A(0)), the 10 bits W1/W5 and W9/W13 are loaded into the first address and readout number registers at S1, thus defining the first address to be read and the number of channels to be read.
- d. The address and readout counters are set to the value of the address and readout registers; readout is initialized.
- e. The content of the first scaler to be read is loaded into the output register; this operation occurs (maximum) 500 nsec after LOAD time (or < 900 nsec if the BUS readout is simultaneously initialized).

2.2 CLEAR Scaler Function

This function is performed either by sending an external CLEAR signal (NIM or TTL, width greater than 20 nsec) or by F(16)*A(0) with bit W7 = 1; CAMAC Z OR C also perform this function.

Following this operation, all scaler contents are set to zero. Figure 2.2 shows the CLEAR timing diagram.

2.3 VETO Action

For all 32 scalers, counting can be inhibited by setting the CAMAC INHIBIT line on or by input VETO action; counting is inhibited either when input veto level is below -0.4 V (NIM veto) or +2 V (TTL veto).

If VBR switch (Veto by BUS Readout) is ON, a Veto is applied for each readout demand from the BUS (duration < 200 nsec).

Please note that inhibit (or VETO) pulses are not counted, whatever the state of the scaler inputs.

2.4 READ Scaler Sequences (Read Out)

Preliminary remark: any READ sequence will permit the user to read the scaler states (counts) at the time the last LOAD function has been performed, except when the Model 4434 scaler is set to "latching disable mode" (see: Side Switch Options - Section 1.6).

There are basically two ways of reading the scaler contents by CAMAC:

a. Sequential read out: $F(2) \cdot A(0)$

When using $F(2) \cdot A(0)$, consecutive channels are read sequentially, starting from the channel addressed by the address register content.

The $Q = 1$ response is generated for each $F(2) \cdot A(0)$ function, until the last channel has been read ($Q = 0$ is given when the readout number is $= RN + 1$).

b. Random read out: $F(0) \cdot A(0)$

If the user wants to read one specific channel, he has to first write that channel address by sending $F(16) \cdot A(0)$ with $W8$ set to one and $W1$ to $W5$ containing the specific channel address and then to read the scaler contents by using $F(0) \cdot A(0)$. Please note that $F(0)$ does not increment the address counter and thus an $F(2)$ sequence may always follow a single $F(0)$ read out. The first $F(2)$ would then give the same result as the preceding $F(0)$ read out.

Final remarks : (see also Figure 2.4)

1. Any read out sequence must be preceded by a LOAD function or by an $F(16) \cdot A(0)$ with $W8$ set to one; in the latter case, the read out will enable the user to re-read the scaler register contents (which remain unchanged until the next LOAD function execution).
2. $Q = 1$ for $F(0)$ is given if read out has been correctly initialized (see above).
3. $Q = 1$ for $F(2)$ is given if read out has been correctly initialized and if last channel has not been read.

2.5 TEST Function

Figure 2.3 shows a 24-bit scaler block diagram that represents the scaler operation for the TEST function.

When $F(16) \cdot A(0)$ with $W16 = 1$ is performed, each byte (8 bits/byte) of each scaler is incremented by one, and if the content of the preceding (left side) byte counter was 255 decimals, the counter is incremented by two; this operation needs 12 μ sec to be performed; the VETO is set.

The user can choose between the two following sequences to control the Model 4434 operations with the TEST function:

a. Test and verify each step

CLEAR SCALERS

S { TEST + LOAD ($F(16) \cdot A(0)$ WITH BIT $W6 = W16 = 1$)
 { READ OUT and VERIFY ($32 \times F(2) \cdot A(0)$)

repeat S n times

b. Test and verify the final value

CLEAR SCALERS

S { TEST ($F(16) \cdot A(0)$ WITH BIT $W16 = 1$)
 Repeat S n-1 TIMES (CYCLE TIME > 12 μ sec)
 TEST + LOAD ($F(16) \cdot A(0)$ with bit $W6 = W16 = 1$)

READ OUT and verify results (n TESTS)

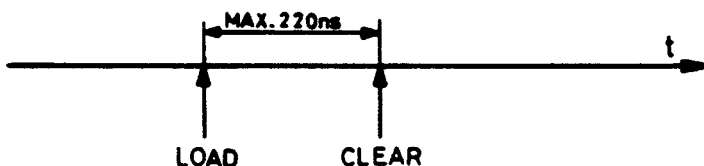
WHEN COMPLETE TEST HAS BEEN PERFORMED, $F(16) \cdot A(0)$ WITH BIT $W16 = 0$ OR Z MUST BE SENT TO REMOVE VETO!

2.6 Multiple Functions

As can be seen from Section 2.5, some functions can be executed "simultaneously" by the Model 4434 scaler. The purpose of this section is to define all multiple functions that can be executed and the order in which they are performed.

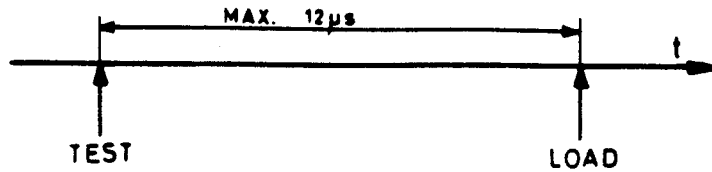
a. LOAD + CLEAR

When simultaneously initialized, these functions are executed according to the following timing diagram:



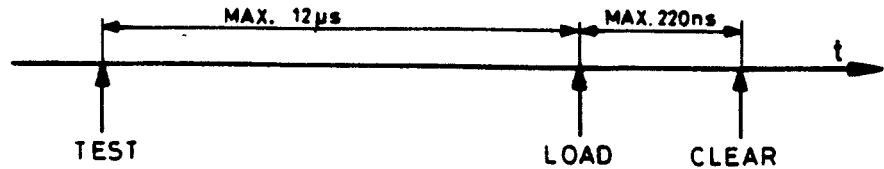
b. TEST + LOAD

When simultaneously initialized, these functions are executed according to the following timing diagram:



c. TEST + LOAD + CLEAR

When simultaneously initialized, these functions are executed according to the following timing diagram:



2.7 LAM and Switch Settings

a. Switch LAD (Latching Disable)

When set, the Model 4434 is set to latching disable mode, all data acquired during read out process are now relative to the time the read out is in progress. Therefore, if the scalers are counting, the data read may be "erroneous".

Note : it is still necessary to initialize the read out process by using $F(16) \cdot A(0)$ with $W8 = 1$.

b. Switch OVF (Overflow)

By default (switch overflow on 16) an "overflow" condition occurs when bit 16 of any scaler is ON (set to 1); when setting switch overflow to 24 an "overflow" condition occurs when bit 24 of any scaler is ON.

c. Switch LCO (Load and Clear at Overflow)

When ON, switch LCO will enable the automatic load and clear function (see Section 2.6) as soon as an "overflow" condition occurs.

This switch must be set to OFF if the user wants to test the scaler operation (see Section 2.5).

d. Switch LOF (LAM Request at Overflow)

When ON, switch LOF will enable automatic LAM generation as soon as an "overflow" condition occurs and is maintained as long as overflow condition is present.

e. Switch LDR (LAM Request when Data Ready)

When ON, switch LDR will enable automatic LAM generation as soon as the 24-bit output register (see Figure 2.1) contains the data to be read.

In this case, LAM is set each time the read out has been initialized.

L is cleared by F(0)*S2 or F(2)*S2 and is set approximately 500 nsec late until the last channel has been read.

f. Switch LRE (LAM Request at Readout Enable)

When ON, switch LRE will enable automatic LAM generation after a readout request.

Final Remark:

LAM and Q response to F(8) and F(10) operations conform to the EUR 4100 e (1972) CAMAC specifications.

2.8 Addressable Read Only Auxiliary BUS

This BUS allows, at any time, the readout of any of the 32 scalers independent of the CAMAC dataway.

The BUS requires an independent controller which is the BUS Master.

A data transfer on the auxiliary BUS is initiated by the BUS Master by sending a 9 parallel bit word, defining the address of the desired scaler, together with a synchronization pulse ARY (Address Ready).

The 9-bit address word includes 4 bits for the address BAD of the modules connected to the BUS (BAD = Bus Address). The BAD may range from 0 to 15. Up to 16 4434 modules can be connected to the same Auxiliary BUS. The address BAD is set for each module by a binary switch, accessible on the side of the module. The other 5 bits in the address word define the subaddress SAD inside the given module (SAD ranges from 0 to 31).

Responding to a readout request, the addressed 4434 will send on the Auxiliary BUS, after the end of the ARY signal, the content of the addressed scaler, as a 24 parallel bit word, together with a synchronization signal DRY (Data Ready). Readouts by CAMAC and by Auxiliary BUS, when acting together, proceed by time sharing, CAMAC having priority. The response time on the Auxiliary BUS will be affected. (Response time from 500 nsec to 900 nsec.)

In addition, when a 4434 is in test mode, the readout by Auxiliary BUS will be halted during a complete test cycle (12.8 μ sec).

The Bit BD (BUS Disable) of the Command Register CR, allows the suspension of the readout by the Auxiliary BUS. The bit BD is reset to zero by a Z command.

Depending on the type of CAMAC readout chosen for a particular 4434, two types of readout by Auxiliary BUS are possible:

a. Spying Readout

In this case, a CAMAC readout has not been initialized (LED RDE OFF) or the switch LAD (Latching Disable) is on.

The content of a scaler is loaded on the Auxiliary BUS output register even when the scaler is counting. The data can eventually be wrong. The possibility of wrong data can be avoided by setting the switch VBR (Veto by BUS Readout). The switch has the effect of halting counting over all the 32 channels during 200 nsec, that is, the time needed to load the output register.

b. Latched Readout

In this case, a CAMAC readout has been initialized (LED RDE ON).

The data loaded in the Auxiliary BUS output register will be taken out of the latches associated with each scaler. The above is valid as long as readout via CAMAC is not finished. This readout mode allows the readout of the same data both by CAMAC and by Auxiliary BUS.

2.9 Input Options

Scaler Counting Inputs

The 32 scaler inputs can be set to operate either in ECL differential input mode or in TTL single ended input mode.

This is done by inserting the appropriate set of termination resistor networks into the input termination single-in-line sockets and eight jumpers.

a. Differential (ECL) Input Mode

Figures 2.5 and 2.7 show the input termination arrangement.

b. Single Ended TTL Input Mode (MOD 100)

Figures 2.6 and 2.8 show the input termination arrangement.

2.10 Cables

Interconnections between different ECLine modules, for transmission of different ECL pulse pairs, can be made either by multiwire cables or by single twisted pair cables for one to one connections.

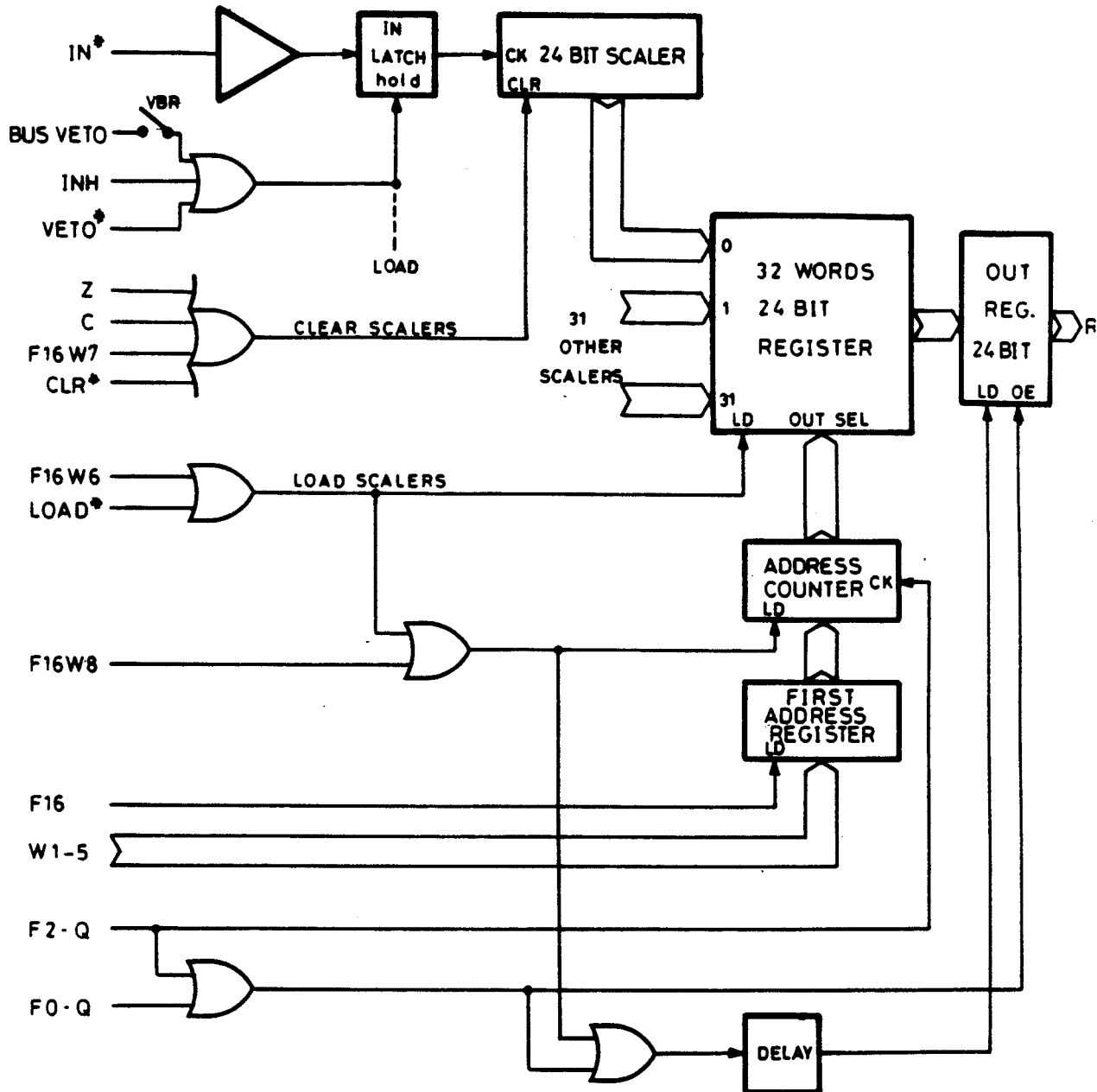
Such interconnecting cables may be purchased from LeCroy and in particular, as multiwire cables, two types are available; one for short interconnections using just flat cable, the second for long interconnections using twisted and flat ribbon cable.

The notation used in ordering these cables is as follows:

- STC-DC/34-LL Multiwire cable for short interconnections
- LTD-DC/34-LL Multiwire cable for long interconnections
- STP-DC/02-LL Single twisted pair cable.

Where LL is the cable length in feet which should be specified by the customer.

FUNCTIONAL BLOCK DIAGRAM



Remarks :

- a) SYMBOL * means front panel input SIGNAL.
- b) The following functional block diagram should not be used for timing calculations.

Figure 2.1

CLEAR TIMING DIAGRAM

ALL TIMES REFERED TO FRONT PANEL INPUT CONNECTORS

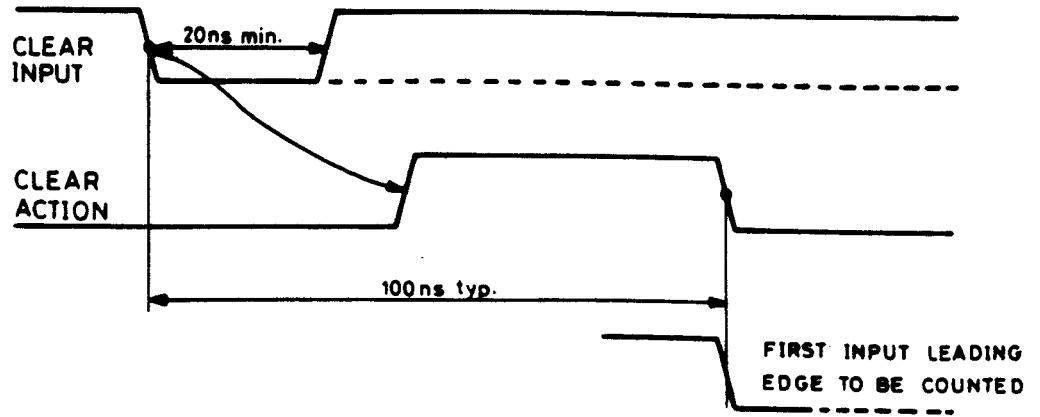


Figure 2.2

TEST INCREMENTATION BLOCK DIAGRAM

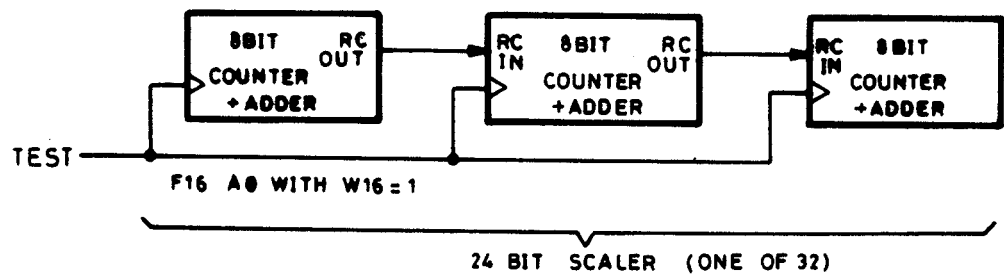


Figure 2.3

FUNCTIONAL BLOCK DIAGRAM LAM & ANSWER LOGIC

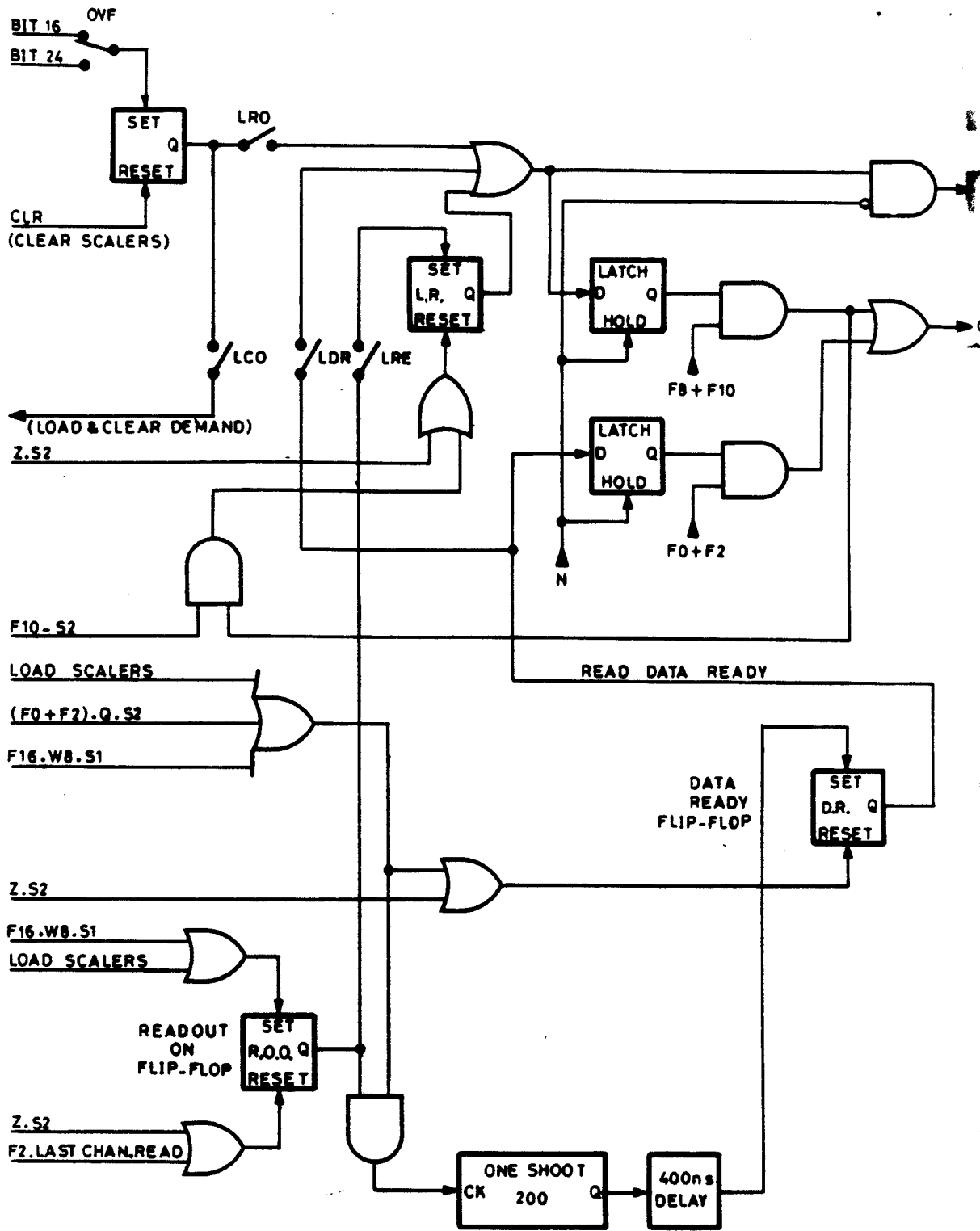
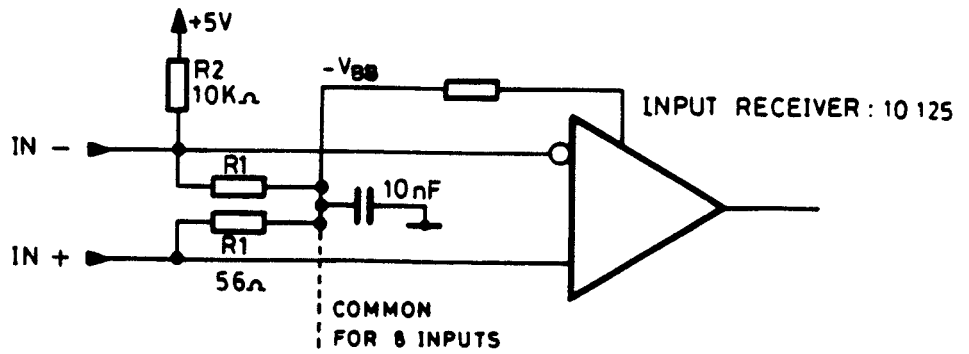


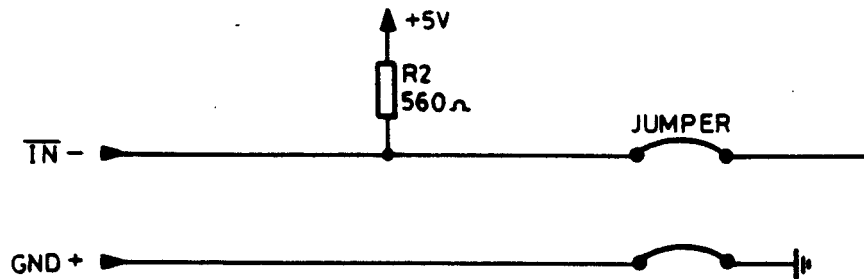
Figure 2.4



ECL DIFFERENTIAL INPUT MODE

Common mode input range: $-1.3\text{ V} \pm 0.2\text{ V}$
 Differential mode input range: $\pm 0.6\text{ V}$

Figure 2.5



TTL SINGLE ENDED MODE

Note: + inputs are connected to ground in this mode; negative TTL input pulses enter the scaler via the - input; the last pair of each 34-pin input connector is connected to ground to give a return path for the input currents (last pair of each input cable).

Figure 2.6

ECL DIFFERENTIAL MODE

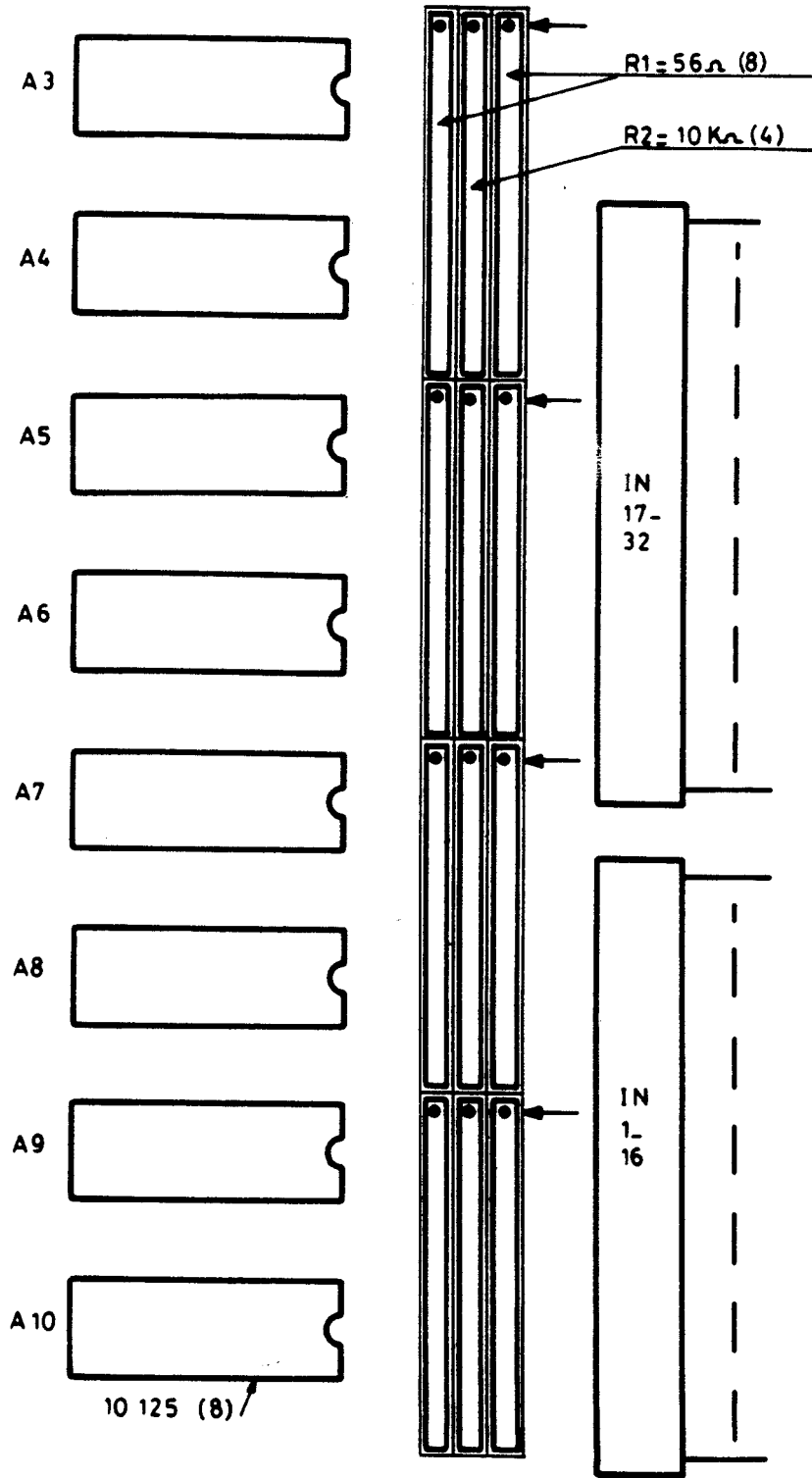


Figure 2.7

TTL SINGLE ENDED MODE

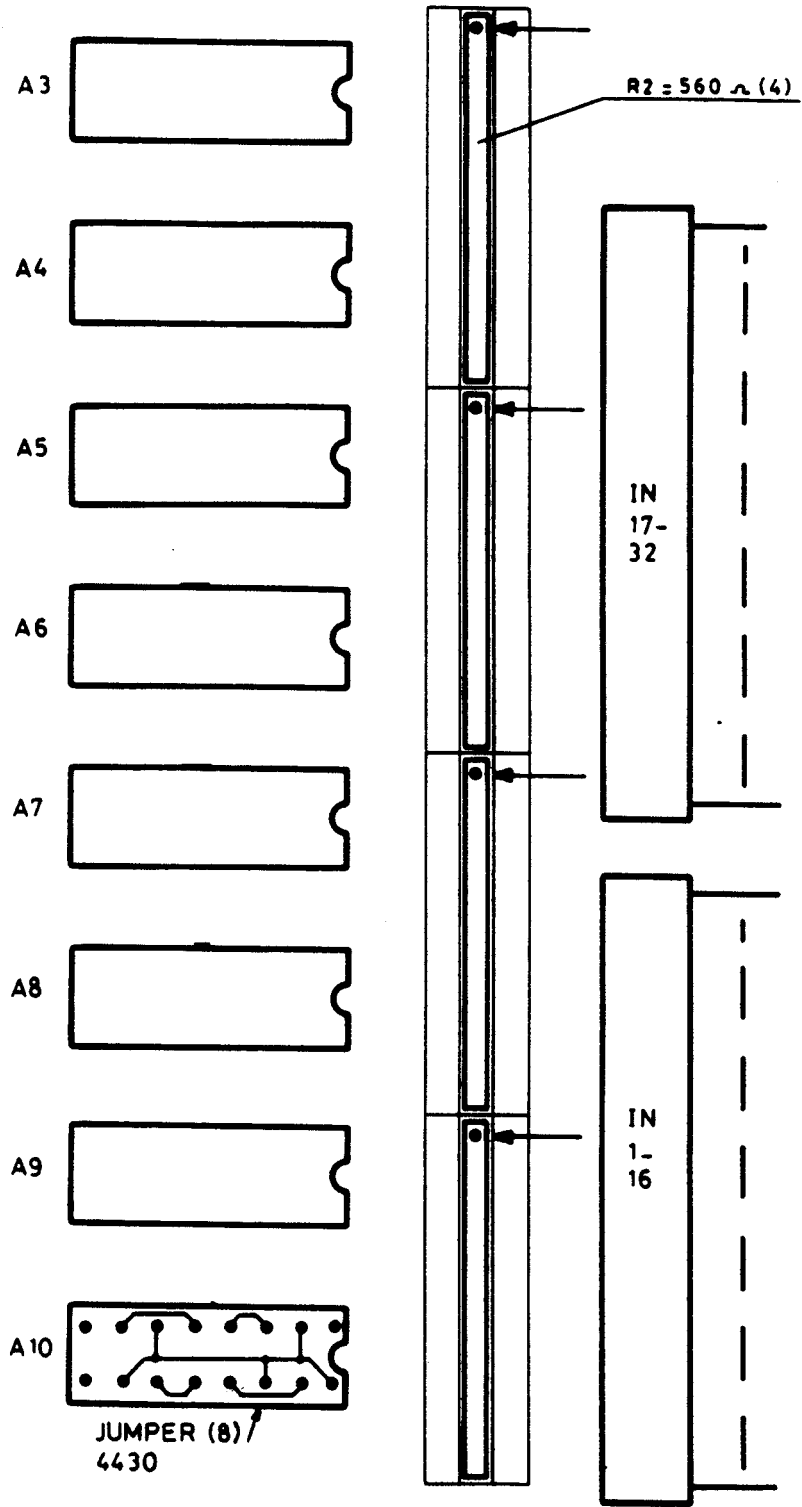


Figure 2.8

