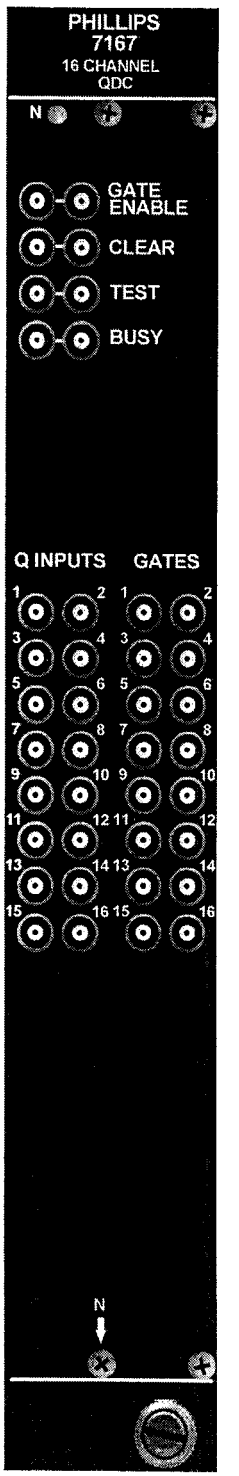
Phillips Scientific

16 Channel Individual Gate Charge ADC

CAMAC MODEL 7167 7167H

FEATURES

* *The Model 7167 Features LEMO Inputs*
* *The Model 7167H has Differential Header Inputs*
* *Individual GATE and CHARGE Inputs for Each Channel*
* *Less Than 7.2 µSec Conversion and Processing Time*
* *12-Bit Dynamic Range, Resolution to 125 fC/Count*
* *Programmable Pedestal Correction*
* *Sparse Data Scan with Lower and Upper Threshold Cuts*
* *Fast CLEAR and COMMON ENABLE Window*
* *Built-in Test Features Check QDC and Digitization*



DESCRIPTION

The Model 7167/H QDC implements 16 channels of Charge to Digital Conversion (QDC), each with its own GATE, followed by a digital processing section and CAMAC interface in a double width CAMAC module. To minimize data readout time, the QDC performs a sparse data function. Channels can be individually programmed with pedestal correction and both lower and upper level thresholds. Digitization starts following release of the COMMON ENABLE input. It may be delayed by a user-programmable amount to allow time for derivation of fast CLEAR signals.

Channels that meet the sparsification requirements will have corresponding bits set in the Hit Register. Subsequent events will be ignored until the Hit Register is cleared either by completing a sparse read of the module or via front panel FAST CLEAR or CAMAC Clear commands.

CHARGE INPUTS

Input Impedance

Single Ended : *51 ohm, ±2%, direct coupled. (AC coupling optional).*

Differential : *102 ohm, ±2%, direct coupled. (AC coupling optional).*

Voltage Compliance : *0 to -2.5 Volts;* ***Common Mode:*** *±2.5 Volts DC.*

Input Offset

Single Ended : *0 to 2mVolt, (40µAmp) maximum.*

Differential : *0 to 2mVolt, (20µAmp) maximum.*

Dynamic Range : *-512pC full scale, -125fC/Count ±2%, 12-bit Range. (Other ranges available).*

Charge Feedthrough : *Less than ±0.1% of input.*

Internal Signal Coupling : *Front-end is AC coupled to the current integration stage with a 3.3 mSec time constant. Other time constants or DC coupling is available.* ***Note:*** *When direct-coupled, small input offset voltages can cause large pedestals.*

Stability : *Better than 5fC/ °C between 0 °C to 60 °C.*

Pedestal vs. Gate Width : *Less than 40fC/nSec.*

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CLEAR, GATE and TEST INPUTS

LEMO Inputs (7167) : NIM logic levels; Two LEMO connectors per input to facilitate daisy chaining. Input impedance 5.1K ohm; 50 ohm terminate at last module in chain.

ECL Inputs (7167H) : Differential ECL logic levels; 2 pairs per input to facilitate daisy chaining; Terminate at end of chain with 110 ohms.

GATE ENABLE Input : Common to all channels, enables the individual gate inputs. Processing of events begins at end of enable pulse. Usable from 50nSec to 10µSec. Must extend at least 10nSec before and after all individual gates.

Individual Gates : 20nSec to 10µSec; should precede the charge input by 20nSec minimum; no charge dependence on position of analog event within gate, other than pedestal vs. gate effect. **Note:** When operating with GATE durations greater than several microseconds, large pedestals can be present due to the integration of small input signals or levels; Q (Charge) = I (Current) x T (Time)

GATE Feedthrough : Less than ±0.5 pC.

CLEAR Input : Common to all channels, accepts 10nSec or greater input width.

CLEAR Settling Time : Less than 750nSec to within one count.

CLEAR Function : Halts conversion, locks out any new gate, clears analog data, most recent digital data and hit register.

TEST Input : Leading edge causes a GATE and analog input to be applied to all channels. Digitizes to approximately 1/4 full scale calibration. NOT intended for precise calibration of the module.

BUSY Output

LEMO (7167) : Two paralleled LEMO connectors, bridged negative NIM logic 32mA.

ECL (7167H) : Two double row connector pins; Differential ECL logic output.

Active from the trailing edge of GATE ENABLE until the event has been aborted by CLEAR or has been fully digitized and read out through the sparse data port. BUSY follows the Hit Register and thus may also be released by clearing the Hit Register. Useful for minimizing QDC dead time when folded into the fast trigger logic.

FRONT END PERFORMANCE

A dithered mode may be selected by the user for improved performance in spectroscopy analysis. It should be disabled when working within the bottom or top 1.5% of the module's range or for those measurements not creating histograms of data

Linearity : Integral : Less than 3 counts over 10% to 90% of range.
Differential : Less than 0.025% of full scale maximum.
Non-Dithered : ±0.5 bins typically.
Dithered : ±0.1 bins typically.

Crosstalk : 1 LSB maximum between adjacent channels operated within range.

Conversion Time : 7.2µSec maximum, includes 750nSec for settling and for accepting fast CLEAR signals. Timing is measured from the trailing edge of the COMMON ENABLE signal. Digitization may be delayed by 0 to 16µSec in 62.5nSec increments with external jumpers. The increased delay may be used to allow a greater acceptance window for CLEAR signals.

Power Supply Requirements : + 6V @ 2.6 Amps typically
– 6V @ 2.0 Amps typically
+24V @ 400 mA typically
Forced air cooling is recommended.

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ADDITIONAL TEST FEATURES

Calibration Check : Simulates a Charge/Gate sequence under CAMAC control to verify operation of the module. CAMAC selectable nominal 1/3 or 2/3 full scale calibration. Not intended for precise calibration of the module.

CAMAC Check : Loads a predetermined pattern to simulate the outputs of the A/D converters. Useful for verifying the operation of the processing sections of the module.

SPARSIFICATION and LAM OPERATION

Separate pedestals and upper and lower thresholds may be set for each channel. They are enabled using bits in the Control Register. Pedestals in signed 2's complement format are added to the data before threshold comparison. Bits in the Hit Register are set during digitization for those channels whose pedestal corrected data falls within their upper and lower thresholds. If enabled, LAM is set whenever a bit in the Hit Register is set. Sparse data reads present only those channels with bits set in the Hit Register, starting with the highest numbered channel. As channels are read, their Hit Register bits are reset; when the final channel has been read LAM is reset. LAM is also reset when the Hit Register is reset.

DATA WORD FORMAT

16 13	12 1
Channel ID	Channel Data

CONTROL REGISTER FORMAT

16 9	8 4	3	2	1
Conversion Delay (Read Only)	0	UT Enable	LT Enable	PED Enable

CAMAC DATAWAY OPERATIONS

F(0)·A(X) : Read event data memory for Channel (X+1). Data word as described above.

F(1)·A(X) : Read the parameter memory pointed to by the most recent F17 operation for channel (X+1).

F(4)·A(0) : Read Sparse Data. Only those channels with data that falls between their upper and lower thresholds are read, starting with the highest numbered channel. Reading an empty buffer returns Q false. Data word as described above.

F(6)·A(0) : Read the Control Register. Format described above.

F(6)·A(1) : Read the Hit Register. Shows which channels' pedestal corrected data falls within their upper and lower thresholds.

F(8) : Test LAM. A Q=1 response is generated if LAM is present and enabled. The address lines have no effect on this command.

F(9) : Clear the Module. Resets front end, clears and disables LAM, disables pedestals and thresholds. The address lines have no effect on this command.

CAMAC DATAWAY OPERATIONS (continued)

F(10) : *Clear LAM. Occurs on S2 strobe. The address lines have no effect on this command.*

F(11)·A(0) : *Reset the Control Register. Occurs on S2 strobe.*

F(11)·A(1) : *Reset the Hit Register and LAM. No effect on data memory. Occurs on S2 strobe.*

F(11)·A(2) : *Reset the Test Register. Occurs on S2 strobe.*

F(11)·A(3) : *Reset the Hit Register, LAM and data memory. Occurs on S2 strobe.*

F(16)·A(X) : *Write to data memory for channel (X+1).*

F(17)·A(0) : *Select the Pedestal Memory for the next F1 or F20 operation.*

F(17)·A(1) : *Select the Lower Threshold Memory for the next F1 or F20 operation.*

F(17)·A(2) : *Select the Upper Threshold Memory for the next F1 or F20 operation.*

F(17)·A(4) : *Select the Test Register for the next F20 operation.*

F(19)·A(0) : *Set the Control Register bits. Format described above.*

F(20)·A(X) : *Write the pedestal, upper or lower threshold for Channel (X+1) as selected by the most recent F17 operation. Pedestal range is ±4095; threshold ranges are 0 to 4095. Program the test register if it was selected by the most recent F17 operation.*

A0 : Test pattern = 001001001001
A1 : Test pattern = 010010010010
A2 : Test pattern = 100100100100
A3 : Test pattern = 111111111111

F(23)·A(0) : *Reset the Control Register bits. Format described above.*

F(24) : *Disable LAM. Occurs on the S2 strobe. The address lines have no effect on this command.*

F(25)·A0 : *Digital test. Initiates a data acquisition cycle using the value stored in the Test Register by the most recent F20 command.*

F(25)·A1 : *Test. Initiates a data acquisition cycle using a simulated event of approximately 1/3 full scale applied to the front end.*

F(25)·A2 : *Test. Runs a data acquisition cycle using a simulated event of approximately 2/3 full scale applied to the front end.*

F(26) : *Enable LAM. Enables LAM on the S1 strobe. The address lines have no effect on this command.*

C, Z : *Reset the front end, clear and disable the LAM, disable pedestal and thresholds and clear the Hit Register. Occurs on the S2 strobe.*

I : *Inhibits QDC Front End.*

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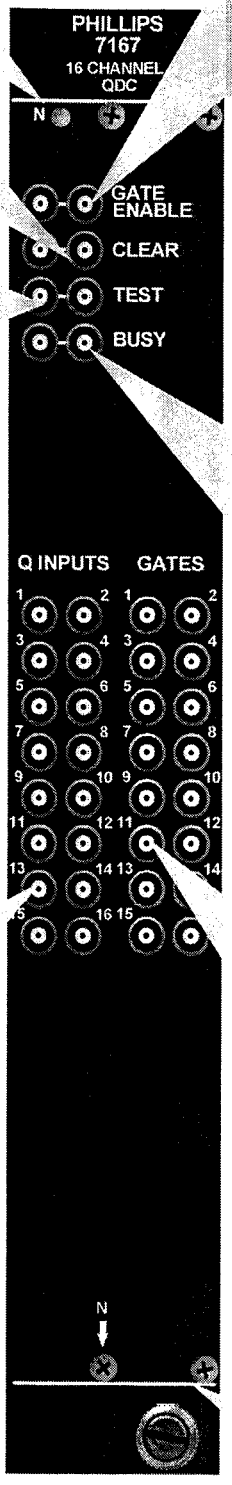
MODEL 7167 SIXTEEN CHANNEL INDIVIDUAL GATE CHARGE ADC

(Front Panel Description)

An LED Indicates the Module is Being Addressed via CAMAC.

Clear Input; NIM Logic (-500mV); Bridged Inputs Allow Easy Daisy Chaining; Clears All QDC Front Ends in 750nSec.

Test Input; NIM Logic (-500mV); Bridged Inputs Allow Easy Daisy Chaining; Generates a Gate and a Test Event.



Gate Enable Input; NIM Logic (-500mV); Bridged Inputs Allow Easy Daisy Chaining; Enables Individual Gates; Width 50nS to 10μS.

Busy Output Active After Gate until Clear or Event Read; Bridged NIM Out; -32mA (-1.6V @ 50 ohm, -.8V @ 25 ohm Load).

Sixteen Analog Charge QDC Inputs; -512pC, 50 ohm Input is Standard; (Optional Inputs +512pC)

Sixteen Individual Gates; NIM Logic (-500mV), 50 ohm Input; Samples Charge; Width 20nS to 10μSec.

Standard #2 CAMAC Packaging in accordance with EUR 4100.

Note:

1). Rear Panel Jumper Provides a Programmable Conversion Delay of 16μSec in 62.5nS Increments. The Delay allows an Unwanted Event to be Cleared Before it is Digitized and Stored.

PROGRAMMING MANUAL FOR

THE MODELS

7164 / 7164H

7166 / 7166H

7167 / 7167H

7186 / 7186H

7187 / 7187H

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PROGRAMMING MANUAL FOR MODELS

7164/7164H,

7166/7166H, 7167/7167H,

7186/7186H, AND 7187/7187H

1. CAMAC DATAWAY OPERATIONS

1.1 Writing Data

F(16)•A(X): Write to data memory for channel (X+1).

1.2 Reading Data

F(0)•A(X): Read event data memory for Channel (X+1). Data word contains pedestal corrected data and the channel number. Data is present regardless of sparsification and is read non-destructively.

F(4)•A(0): Read Sparse Data. Only those channels with data that falls between the Upper and Lower Thresholds are read, starting with the highest numbered channel. Each read presents the next channel on the hit list. As each channel is read, its bit in the Hit Register is reset. Reading an empty buffer returns Q false, X true.

16 13	12 1
Channel #	Channel Data

Channel Data Format

1.3 Set the Control Register

F(19)•A(0)•D(X): Selectively enable the Pedestal, Upper and Lower Thresholds for all channels.

D1=1 Enable the Pedestals
D2=1 Enable the Lower Thresholds
D3=1 Enable the Upper Thresholds
D4 to D15 = 1 No Action

1.4 Reset the Control Register

F(23)•A(0)•D(X): Selectively disable the Pedestal, Upper and Lower Thresholds for all channels.

D1=1 Disable the Pedestals
D2=1 Disable the Lower Thresholds
D3=1 Disable the Upper Thresholds
D4 to D15 = 1 No Action

1.5 Read the Control Register

F(6)•A(0): Read the control register. This tells which of the Pedestal, Upper Threshold or Lower Threshold are enabled, as well as the programming of the Conversion Delay.

16 9	8 4	3	2	1
MSB Delay Time LSB	0	UT Enabled	LT Enabled	PED Enabled

Control Register Data Format

1.6 Read the Hit Register

F(6)•A(1): Read the Hit Register. Shows which channels' pedestal corrected data fall within their Upper and Lower Thresholds. A 1 in any position indicates the channel has passed sparsification. For example, 0100 0010 0000 1001 shows that data on channels 1, 4, 10, and 15 have passed sparsification. These are the channels which will be read using the sparse data read function (F4).

16	1
Channel 16	Channel 1

Hit Register Data Format

1.7 Read and Write the Parameter Memory

Signed two's complement arithmetic is used. Pedestals occupy 13 bits giving a range of -4096 ($1000) to +4095 ($0FFF). Thresholds are 12 bits, ranging from 0 to 4095.

1.7.1 Select the Parameter

F(17)•A(0): Select the Pedestal Memory for the next F1 or F20 operation.

F(17)•A(1): Select the Lower Threshold Memory for the next F1 or F20 operation.

F(17)•A(2): Select the Upper Threshold Memory for the next F1 or F20 operation.

1.7.2 Write the Data

F(20)•A(X): Write the Pedestal, Upper or Lower Threshold for Channel (X+1) as selected by the most recent F17 operation.

1.7.3 Read the Data

F(1)•A(X): Read the Parameter Memory pointed to by the most recent F17 operation for channel (X+1).

1.8 Test Functions

1.8.1 Run a Test from the Test Registers

1.8.1.1 Select a Pattern

1.8.1.1.1 Select the Test Registers

F(17)•A(4): Select the Test Register for the next F20 operation.

1.8.1.1.2 Select a Pattern

F(20)•A(X): Program the Test Register if it was selected by the most recent F17 operation.

X	Pattern
0	001001001001
1	010010010010
2	100100100100
3	111111111111

1.8.1.2 Run A Test

F(25)•A0: Digital test. Initiates a data acquisition cycle using the value stored in the Test Register by the most recent F20 command.

1.8.2 Run A Front End Full Scale Test

Models 7166/7166H, 7167/7167H, 7186/7186H and 7187/7187H

F(25)•A1: Initiates a data acquisition cycle using a simulated event of approximately 1/3 full scale applied to the front end.

F(25)•A2: Initiates a data acquisition cycle using a simulated event of approximately 2/3 full scale applied to the front end.

Model 7164/7164H

F(25)•A1: Initiates a data acquisition cycle using a simulated event of approximately 1/20 full scale applied to the front end.

F(25)•A2: Initiates a data acquisition cycle using a simulated event of approximately 1/4 full scale applied to the front end.

1.9 LAM

LAM is set during digitization when pedestal corrected data for at least one channel falls between that channel's Upper and Lower Thresholds.

F(24): Disable LAM. Occurs on the S2 strobe. The address lines have no effect on this command.

F(26): Enable LAM. Enables LAM on the S1 strobe. The address lines have no effect on this command.

F(8): Test LAM. A Q=1 response is generated if LAM is present and enabled. The address lines have no effect on this command.

F(10): Clear LAM. Occurs on S2 strobe. The address lines have no effect on this command.

1.10 Resets

F(9): Clear the Module. Resets front end, clears and disables LAM, disables pedestals and thresholds. The address lines have no effect on this command.

F(11)•A(0): Reset the Control Register. Occurs on S2 strobe.

F(11)•A(1): Reset the Hit Register and LAM. No effect on data memory. Occurs on S2 strobe.

F(11)•A(2): Reset the Test Register. Occurs on S2 strobe.

F(11)•A(3): Reset the Hit Register, LAM and data memory. Occurs on S2 strobe.

2. CAMAC NON-DATAWAY COMMANDS

C, Z: Reset the front end, clear and disable the LAM, disable pedestal and thresholds and clear the Hit Register. Occurs on the S2 strobe.

I: Inhibits front end functions.

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APPENDIX A

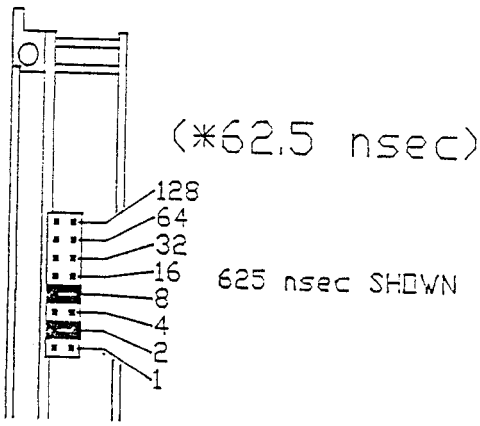
7167 / 7167H

PROGRAMMING

JUMPERS

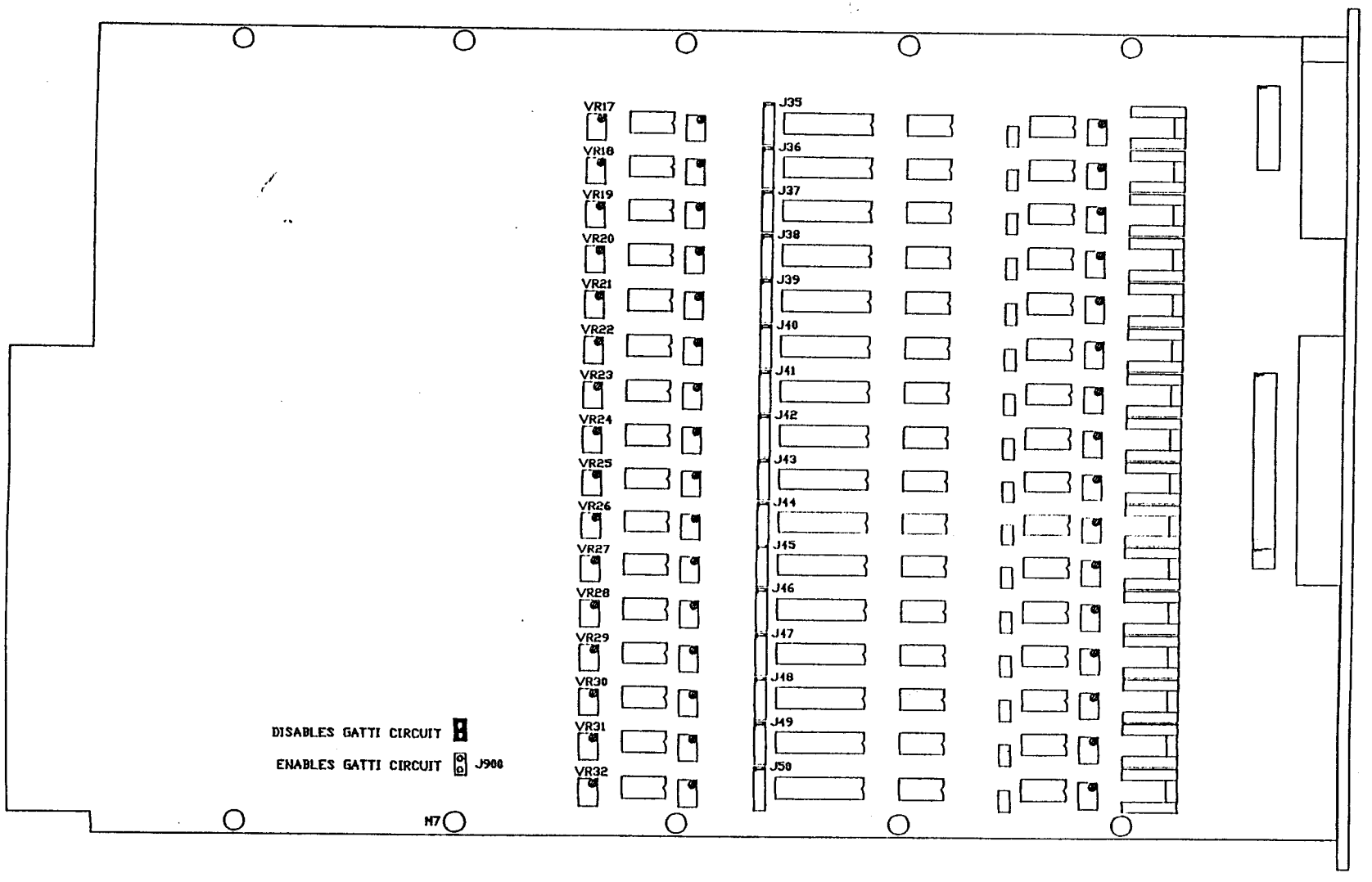
7166/7167 REAR JUMPER PROGRAMING

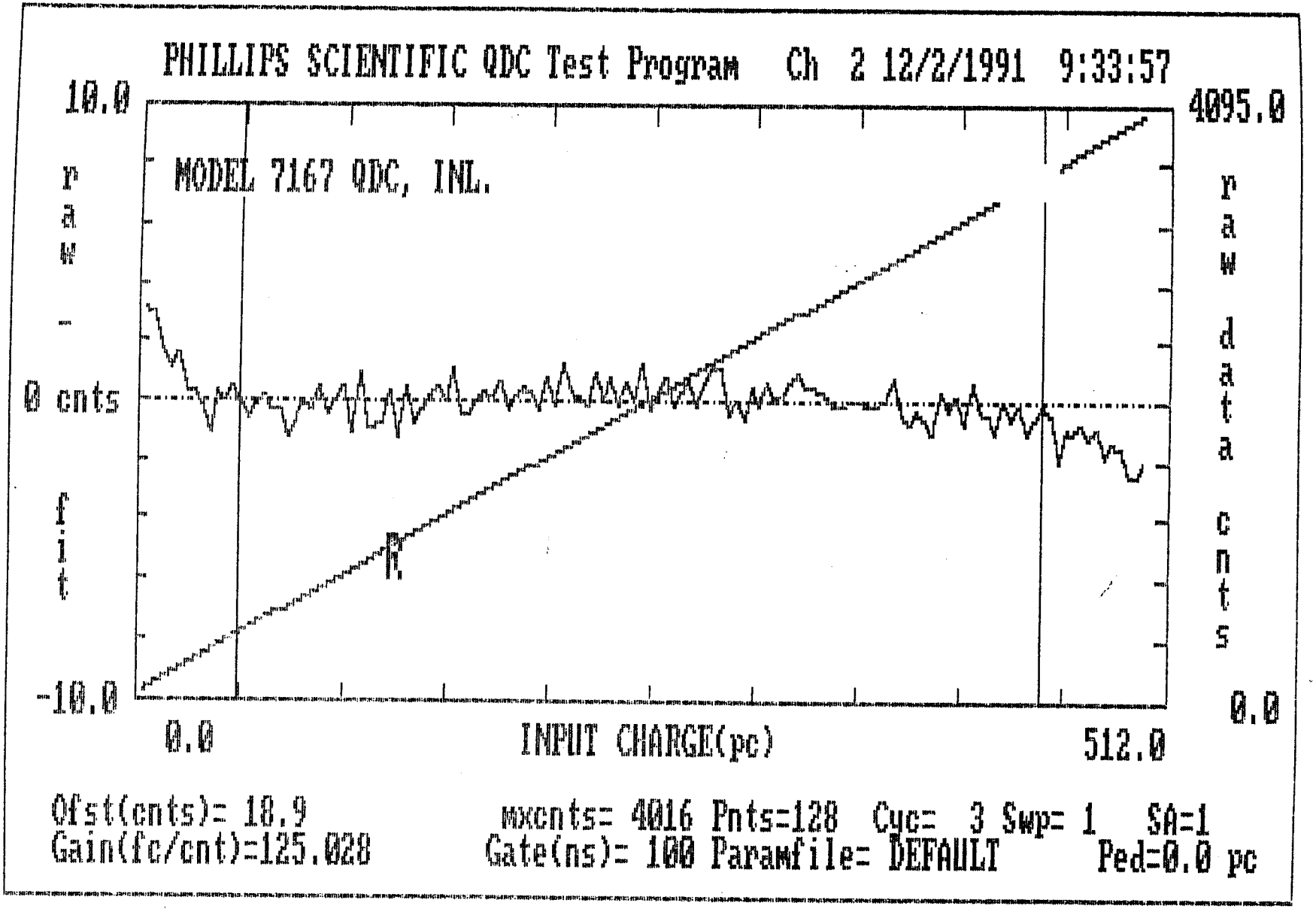
CONVERSION DELAY TIME MULTIPLIER



VIEWED FROM TOP REAR OF MODULE

7166/7167 GATTI ENABLE/DISABLE JUMPER LOCATION

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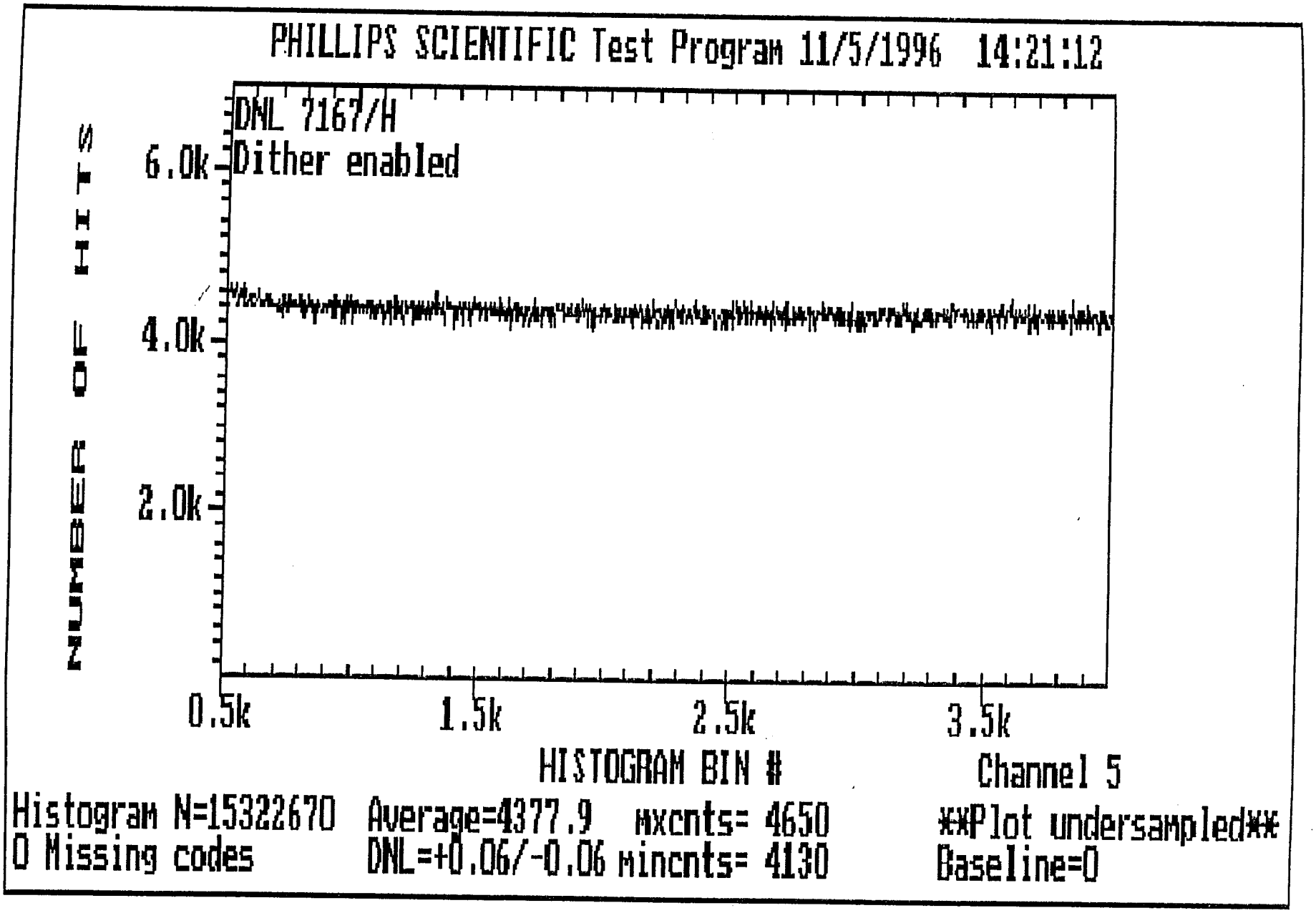
MODEL 7167 QDC, INL.
10.0
raw - fit
0 cnts
-10.0
4095.0
raw data cnts
0.0
0.0
INPUT CHARGE(pc)
512.0
Ofst(cnts)= 18.9
Gain(fc/cnt)=125.028
Mxcnts= 4016 Pnts=128 Cyc= 3 Swp= 1 SA=1
Gate(ns)= 100 Paramfile= DEFAULT
Ped=0.0 pc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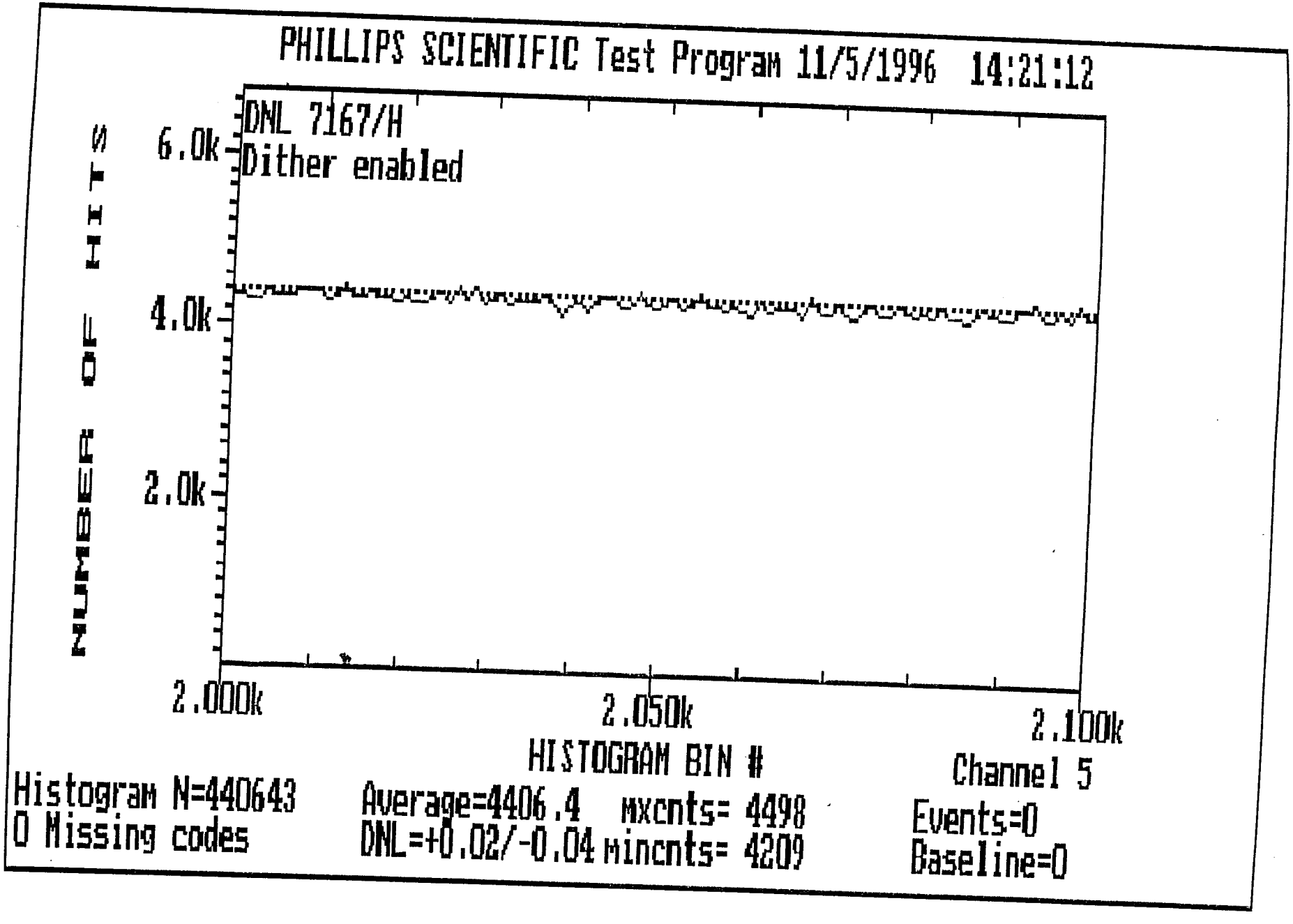
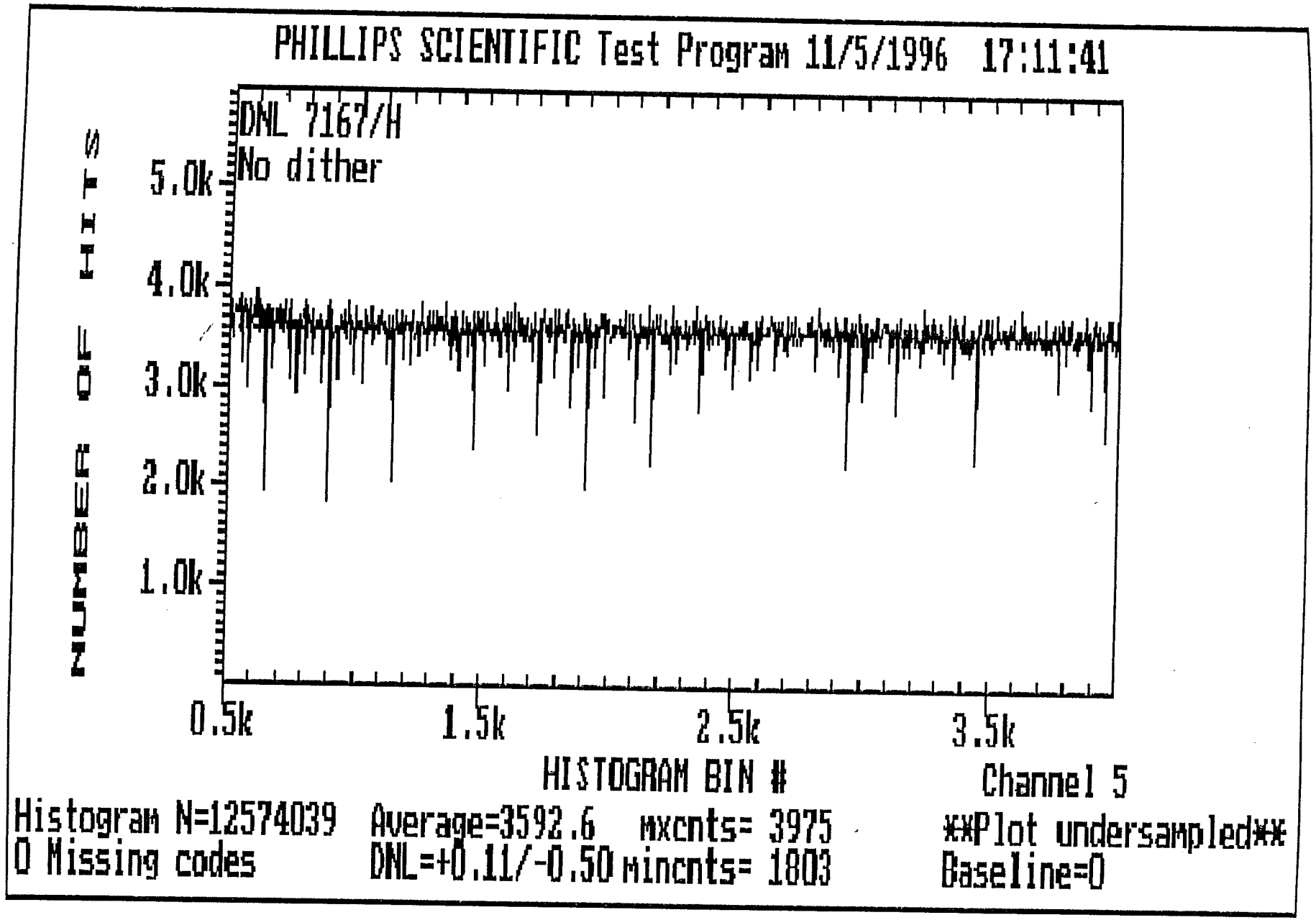
DNL 7167/H
Dither enabled
NUMBER OF HITS
6.0k
4.0k
2.0k
0.5k
1.5k
2.5k
3.5k
HISTOGRAM BIN #
Channel 5
Histogram N=15322670 Average=4377.9 mxcnts= 4650
0 Missing codes DNL=+0.06/-0.06 mincnts= 4130
Plot undersampled
Baseline=0


PHILLIPS SCIENTIFIC Test Program 11/5/1996 14:21:12
DNL 7167/H
Dither enabled
NUMBER OF HITS
6.0k
4.0k
2.0k
2.000k
2.050k
2.100k
HISTOGRAM BIN #
Channel 5
Histogram N=440643
0 Missing codes
Average=4406.4 mxcnts= 4498
DNL=+0.02/-0.04 mincnts= 4209
Events=0
Baseline=0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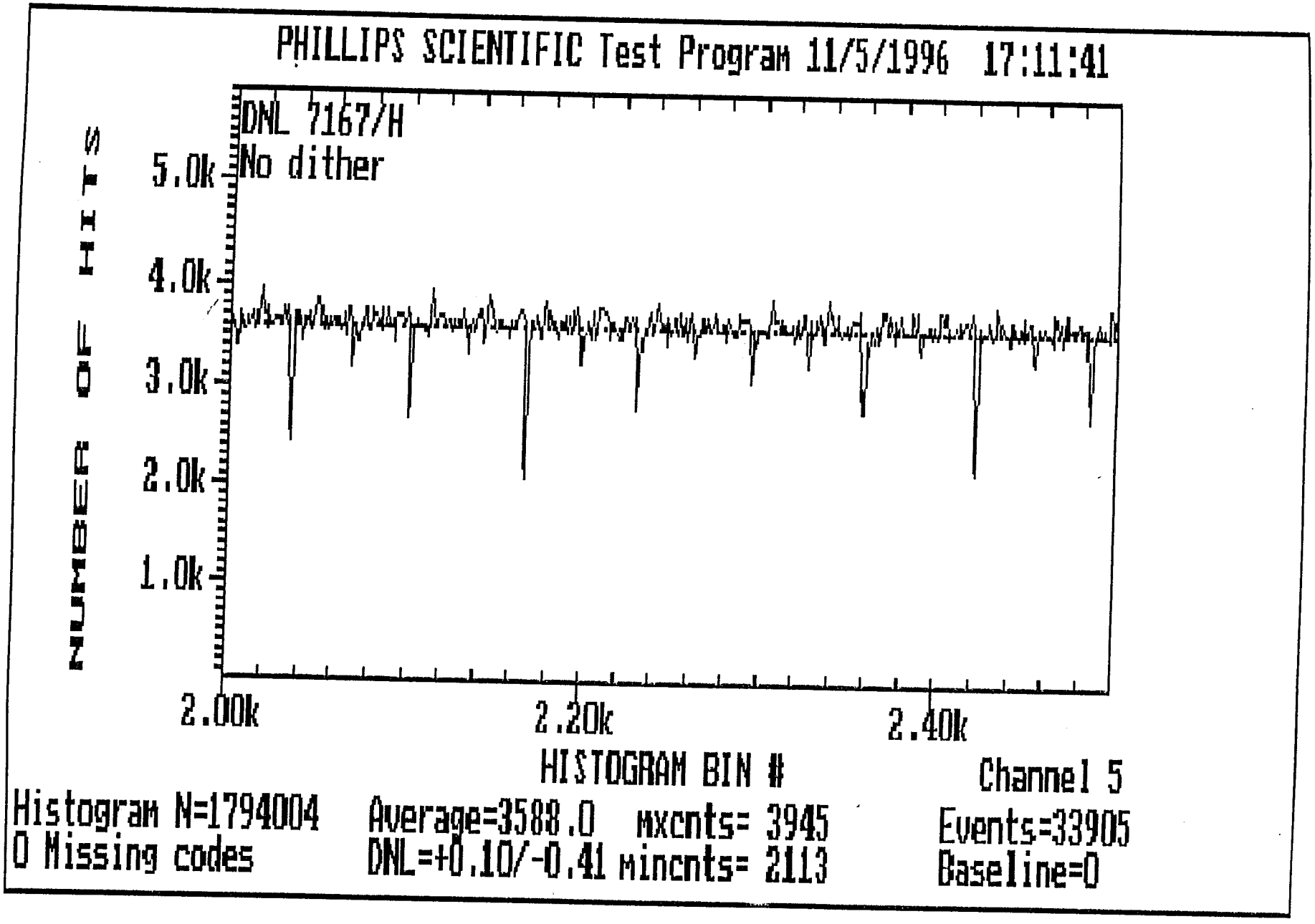
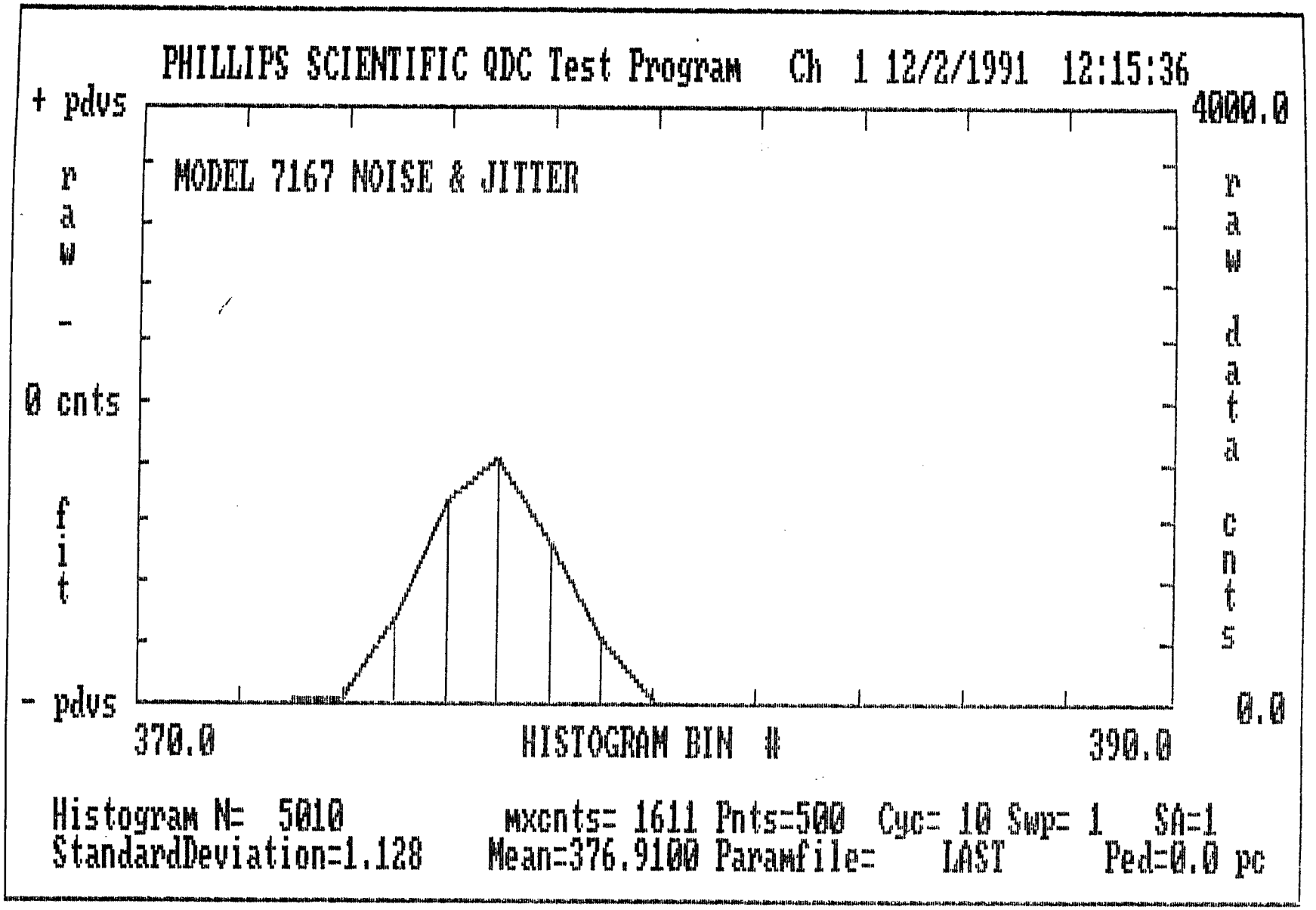
DNL 7167/H
No dither
NUMBER OF HITS
5.0k
4.0k
3.0k
2.0k
1.0k
0.5k
1.5k
2.5k
3.5k
HISTOGRAM BIN #
Channel 5
Histogram N=12574039
0 Missing codes
Average=3592.6
DNL=+0.11/-0.50
mxcnts= 3975
mincnts= 1803
Plot undersampled
Baseline=0


PHILLIPS SCIENTIFIC Test Program 11/5/1996 17:11:41
DNL 7167/H
No dither
NUMBER OF HITS
5.0k
4.0k
3.0k
2.0k
1.0k
2.00k
2.20k
2.40k
HISTOGRAM BIN #
Channel 5
Histogram N=1794004
0 Missing codes
Average=3588.0
DNL=+0.10/-0.41
mxcnts= 3945
mincnts= 2113
Events=33905
Baseline=0


PHILLIPS SCIENTIFIC QDC Test Program Ch 1 12/2/1991 12:15:36
+ pdvs
4000.0
MODEL 7167 NOISE & JITTER
raw - fit
raw data cnts
0 cnts
- pdvs
0.0
370.0
HISTOGRAM BIN #
390.0
Histogram N= 5010
mxcnts= 1611 Pnts=500 Cyc= 10 Swp= 1 SA=1
StandardDeviation=1.128
Mean=376.9100 Paramfile= LAST
Ped=0.0 pc

PRODUCT WARRANTY

PHILLIPS SCIENTIFIC warrants its products to be free from defects in materials and workmanship and to meet performance specifications under normal use and operating conditions for a period of one year from the date of product shipment. The provisions of this warranty shall not apply to any product that has been subjected to misuse or which has been repaired or altered in any way by the purchaser.

Obligations under this warranty is hereby limited to the repair or replacement of the product, or part thereof, which is returned to Phillips Scientific within the warranty period. The foregoing constitutes the entire warranty in lieu of other warranties, expressed or implied, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose with respect to a product and the accompanying written materials. In no event will Phillips Scientific be liable for damages, including any loss of profits, or other direct, incidental or consequential damages arising out of use of or inability to use the product, even if Phillips Scientific or an authorized representative, agent or employee has been advised of the possibility of such damages. Phillips Scientific will not be liable for any such claim by any other party.

To obtain service under this warranty, the purchaser must in advance be issued a returned material authorization (RMA), and ship products prepaid to Phillips Scientific with documentation explaining the malfunction noted. The items will be evaluated, repaired or replaced and promptly returned prepaid if warranty claims are substantiated.