MOD. 4418/V

CAMAC 8-INPUT ADC

User's Guide

OPERATING INSTRUCTIONS

* FERA is a trademark of Le Croy Corp.

TECHNICAL DESCRIPTION

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SILENA CAMAC
MOD. 4418/V

SILENA CAMAC MODEL 4418/V ADC
for Pulse Amplitude Analysis

- 8 INPUT CHANNELS in a single-width CAMAC module
- PULSE PEAK MEASUREMENT of gated-selected signals
- SPECTROSCOPY GRADE PERFORMANCE:
  - High resolution
  - Wide dynamic range
  - High linearity, both integral and differential
  - Low temperature coefficient
  - High long-term stability
- Fast conversion:
  4 μsec for every valid input channel
- Lower and upper threshold control through CAMAC (8-bit)
- Offset control through CAMAC (8-bit)
- Common threshold for noise rejection through CAMAC (8-bit)
- Programmable zero suppression
- Header and Pattern word available
- Sequential or random access CAMAC readout
- Data memory
- ECL readout logic – System compatibility with Le Croy FERA (*) (Fast Encoding and Readout ADC) modules
- System compatibility with CES modules
- Common test feature

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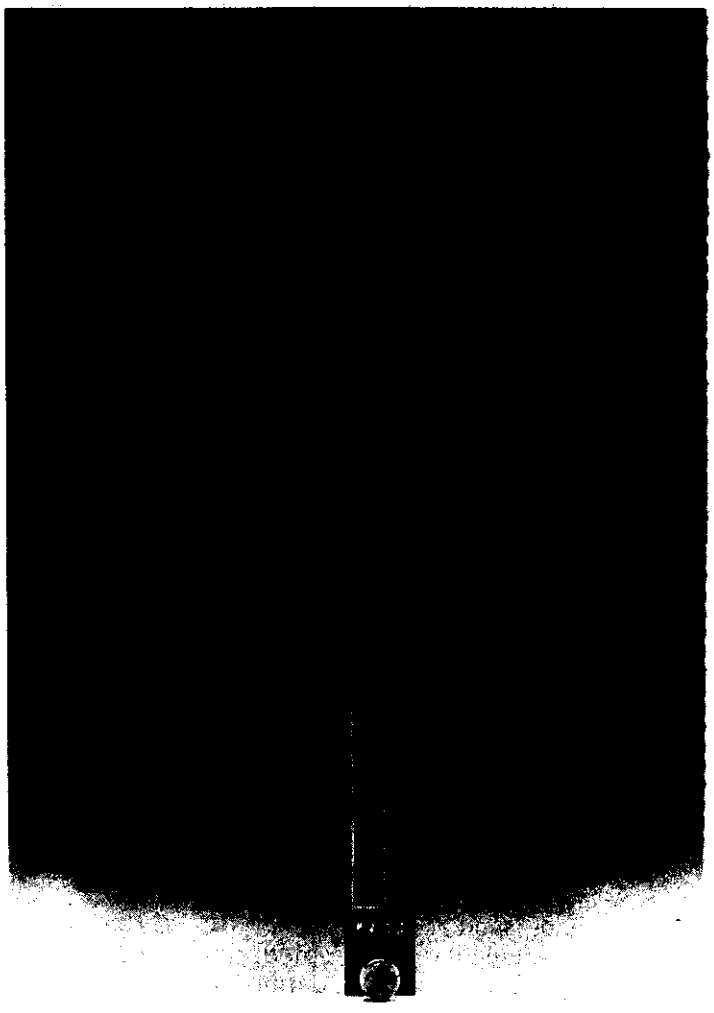


DESCRIPTION

The SILENA Mod. 4418/V combines, in a single CAMAC module, a high resolution analog-to-digital converter with 8 input channels to perform simultaneous data acquisition and pulse amplitude analysis.
The Mod. 4418/V is a highly stable module offering superior integral and differential linearity performance, combined with fast conversion capabilities.

It features a conversion time of 4 μS for each valid channel.
The Mod. 4418/V represents a significant advance in data acquisition from multiple inputs. It has been designed for use in a variety of experimental situations employing many ADC's to perform high resolution, high stability pulse amplitude analysis.

ADVANCED ELECTRONICS
SILENA
SOCIETA PER L'ELETTRONICA AVANZATA

The Mod. 4418/V uses the most advanced surface-mounting techniques to offer a previously unattained combination of operational features and specifications in a highly compact module.
In this pulse amplitude acquisition module, the 8 input channels acquire the peak voltage of the input signals which occur within the time interval marked by a common gate command. The circuit accepts all the typical pulse shapes of nuclear electronic modules, such as spectroscopy amplifiers, time-to-amplitude converters, etc.: RC-RC shaped pulses, semi-gaussian pulses, approximately square pulses.
The overall performance (wide dynamic range, high linearity, etc.) of the input channels and ADC makes the module suitable for high resolution spectroscopy.

SPECIFICATIONS

- *Analog Inputs:* 8
- *Connector:*
  8x2-pin front panel connector (ANSLEY 609-1607)
  The 8 pins of the left row are positive signal inputs; the 8 pins of the right row are ground returns.
- *Input Sensing:*
  Peak voltage
- *Range:*
  100mV to 10V
- *Coupling:*
  D.C.
- *Impedance:*
  1 KΩ; other values available on request
- *Signal Polarity:*
  Positive
- *Signal Shape:*
  All typical shapes from nuclear electronic modules, such as semi gaussian, RC-RC shaped, quasi rectangular are accepted, provided that the pulse peaking time Tpk (defined as the time from the onset of the pulse to the point where the pulse reaches its maximum height) is within the range. 8 μsec ⩾ Tpk ⩾1 μsec.
- *Selection of Acceptable Analog Inputs:*
  By means of the common threshold level for all channels for noise rejection under CAMAC control with 8-bit resolution (0 ÷ 1 Volt) and separate lower and upper level discriminators for each channel under CAMAC control with 8-bit resolution (LLD from 0 to 10%, ULD from 100% to 85%).
- *Resolution:*
  3840 channels (4096 minus 256 channels for sliding scale) corresponding to 2.5 mV/channel.
- *Conversion Time:*
  3 μS for every valid input channel.
- *System Busy Time with "Zero Suppression":*
  Variable as a function of the number of valid channels.
  Valid Channel:
  4 μS
  Channel without Signal-In:
  0.23 μS.
  Channel with Signal In but outside the preselected Window (LLD-ULD):
  1.1 μS.
  Total Busy Time:
  $BT_{Ch\ 1} + BT_{Ch\ 2} + \ldots BT_{Ch\ 8} + 1$ μS.
- *System Busy Time without "Zero Suppression":*
  Fixed 33 μS
- *DC Offset Control (Zero Energy Intercept):*
  ± 3% of full scale value under CAMAC control with 8-bit resolution.
- *Integral Linearity:*
  Typically ± 0.025% of F.S., better than 0.05%; in any case over 95% of the dynamic range. Measured with 0.5 μS semi-gaussian pulse shape. (Tpk = 1,2 μS).
- *Differential Linearity:*
  Typically ± 0.5%, better than ± 1%, in any case over 95% of the dynamic range.
- *Gain Stability:*
  ⩽ 100 ppM/°C.
- *Zero Stability:*
  ⩽ 200 μV/°C.
- *Cross Talk between two Adjacent Inputs:*
  >66 db (measured with 0,5 μS semi-gaussian pulse shape).
- *Count Rate Shift:*
  Not detectable at 100 KHz.

ECL BUS
(Command Bus)

- *Connector:*
  8x2-pin front panel connector. The input matching resistors and output pull-down resistors may be removed to achieve high input and output impedances.
  When these resistors are mounted, the associated LED indicator (RPON) is lit up.
- *Input Level:*
  Differential ECL.
- *Impedance:*
  100 Ω differential.
- *Output Level:*
  Differential ECL (into 100 Ω differential).
- *Gate input (GATE):*
  Common for all analog inputs. For optimum results the gate signal must be applied delayed with respect to the analog signal, but before the pulse to be measured reaches its peak, and must be maintained at least up to this instant.
- *Clear Input (CLR):*
  Common for all analog and digital logic.
  Pulse width ⩾50 ns.
  The module is ready to process a new event after 1,2 μS.

There is sequential readout.
CAMAC Readout function F(Ø) . A(Ø) or F(2) - A(Ø)

2) Without zero suppression (Sequential readout):
CSR=1 and CCE=Ø
EEN=1 ECL Port Readout
EEN=Ø CAMAC Readout

There is always sequential readout of 8 words.
OVF : Overflow Indication; enabled with OVF=Ø (Status Word Bit)
SUB : Channel Subaddress, enabled with SUB=Ø (Status Word Bit)

Always 8 words

R16	R15	R12 ... R1
OVF	SUB	DATA - CHANNEL Ø
OVF	SUB	DATA - CHANNEL 1
OVF	SUB	DATA - CHANNEL 2
OVF	SUB	DATA - CHANNEL 3
OVF	SUB	DATA - CHANNEL 4
OVF	SUB	DATA - CHANNEL 5
OVF	SUB	DATA - CHANNEL 6
OVF	SUB	DATA - CHANNEL 7

3) CAMAC Addressed Readout
CSR=Ø CCE=Indifferent
EEN=Ø Only CAMAC Readout

There is Camac Addressed Readout with F(Ø) . A(Ø-7) or F(2) . A(Ø-7) functions
F(2) . A(7) clears the module during S2
Header Word can be readout with F(Ø) . A(14) or F(2) . A(14)

Pattern Word can be readout with F(Ø) . A(15) or F(2) . A(15)
OVF : Overflow Indication; enabled with OVF=Ø (Status Word bit)
SUB : Channel Subaddress; enabled with SUB=Ø (Status Word bit)

Max 8 Words

R16	R15	R12 ... R1
OVF	SUB	A(Ø) - DATA
OVF	SUB	A(1) - DATA
OVF	SUB	A(2) - DATA
OVF	SUB	A(3) - DATA
OVF	SUB	A(4) - DATA
OVF	SUB	A(5) - DATA
OVF	SUB	A(6) - DATA
OVF	SUB	A(7) - DATA

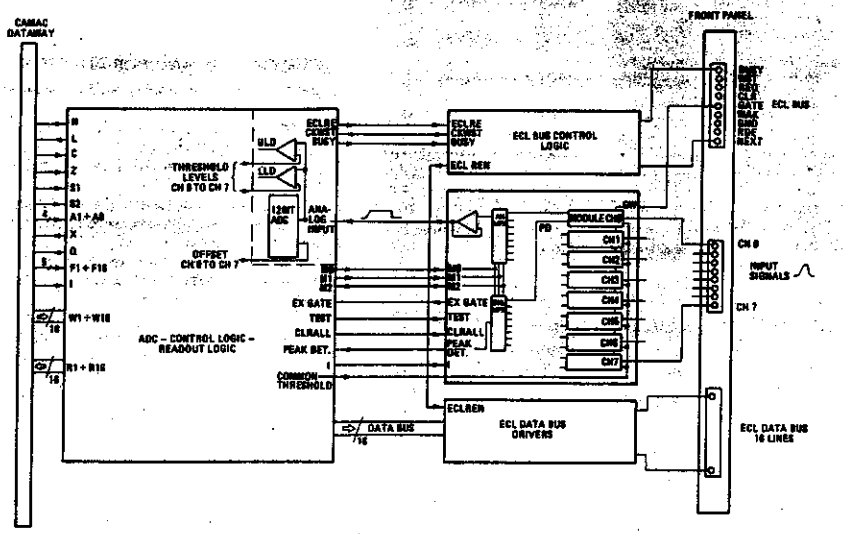
GENERAL

Packaging. RF-shielding 1-width CAMAC module

Power Requirements:
+ 24V at 0,3A, -24V at 0,3A; + 6V at 1,4A;
-6V at 1,55A

Note: When all output pull-down and input matching resistors are removed, the current at -6V is reduced to 1,4 A.

SILENA 4418/V - EIGHT CHANNELS ADC BLOCK DIAGRAM



Specifications are subject to changes without notice.

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- *Request Output (REQ):*
  Indicates that the module is ready to send data to the ECL DATA BUS. The REQ signal is generated at the end of conversion if the bit related to ECL READOUT in the Status Register has been selected.
- *Write Strobe Output (WST):*
  Indicates the time period during which the data present in the ECL Data Bus can be stored in the external memory. WST is generated in a minimum of 10 ns after the data is ready. Its width is higher than 40 ns.
  During the entire WST pulse, the ECL Data Bus data is maintained stable.
- *Write Acknowledge Input (WAK):*
  This input receives the acknowledge signal indicating that the data present on the ECL bus has been loaded into memory and the next data word may be sent.
  The next WST signal is generated at least 50 ns after the WAK signal.
  Minimum WAK width must be 30 ns.
- *Busy Output (BUSY):*
  This output is set to the "1" state 1 μS after the end of the GATE signal and is held to this state until after the end of the read-out cycle (ECL Read-out or CAMAC Read-out). The BUSY state may be reset only by sending a CLEAR signal via CAMAC or via ECL BUS (CLR). The ADC is ready to start a new conversion 1,2 μS after the end of the BUSY state.

ECL PORT ENABLE/NEXT

- *Readout Enable Input (RDE):*
  1x2-pin panel connector. The RDE signal indicates to the module that it can take control of the ECL Data Bus; RDE must be maintained during entire readout time.
  The signal enables the ECL Data Bus, WST Output and WAK input if the module is ready for data transfer (REQ output ON).
- *Input Level:*
  Differential ECL.
- *Input Impedance:*
  100 Ω differential.
- *Next Output (NEXT):*
  1x2-pin front-panel connector.
  Indicates that the module is not ready to transfer data present on the ECL Data Bus or it has finished data transfer.
  The NEXT output signal is generated by the RDE line in the absence of the REQ internal command or, if this command is present, at the end of data read-out.
  The transit time between RDE and NEXT output is typically 3 ns if the module does not include data read-out capabilities.
- *Output Level:*
  ECL differential (iqto 100 Ω differential).

ECL PORT OUTPUT

- *Connector:*
  17x2-pin front-panel connector (ANSLEY 609-3407).
  The last two pins are not connected.
- *Output Level:*
  Differential ECL level (into 100 Ω differential).
  The pull-down resistors must be removed for high impedance outputs.
  When these resistors are mounted, the associated LED indicator (RP ON) is lit up.
- *Data Word Size:*
  16 bits.
- *Read-out Mode:*
  Sequential.
- *Max Read-Out Frequency:*
  8 MHz

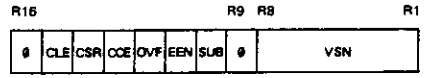
CAMAC COMMANDS AND FUNCTIONS

Z : Initialize; clears the module and the Status Register.
C : Clears the module; does not clear the Status Register and Memory
I : Inhibits the front-panel GATE during CAMAC inhibit command.
X : X response is generated for all valid functions
Q : Q response is generated when the function can be executed
L : LAM (Look-at-me) is set after the end of conversion, if it was enabled, with CAMAC Readout enabled.

F(Ø) . A(Ø) or F(2) . A(Ø)	Read Data	a) CSR=1 CCE=1 with zero suppression b) CSR=1 CCE=Ø without zero suppression

Note: CSR and CCE are STATUS WORD bits (see Status Word)

F(Ø) . A(Ø-7) or F(2) . A(Ø-7)	Reads Data: CSR = Ø CCE = X addressed readout
F(Ø) . A(14) or F(2) . A(14)	Reads Header Word
F(Ø) . A(15)	Reads Pattern Word
F(2) . A(15)	Reads Pattern Word and clears LAM
F(1) . A(0-7)	Reads Threshold Memory (Upper Threshold - ULD)
F(1) . A(8-15)	Reads Threshold Memory (Lower Threshold - LLD)
F(4) . A(Ø-7)	Reads Offset Memory
F(4) . A(9)	Reads Common Threshold
F(4) . A(14)	Reads Status Word Register

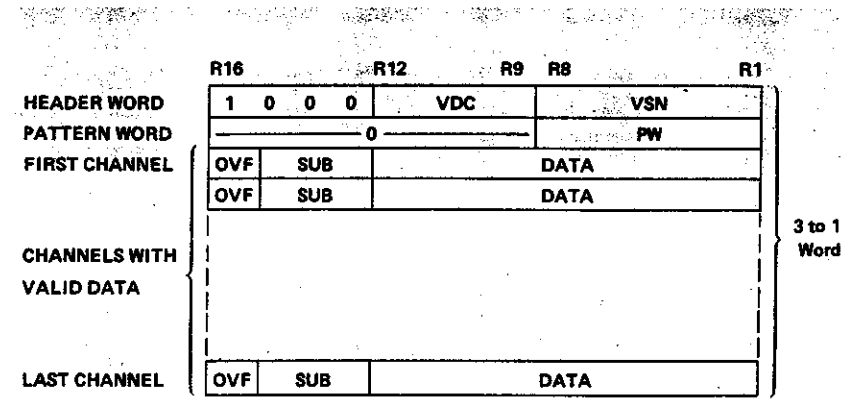


R1-R8 (VSN)	Logical address of the Module: index source for sequential readout with zero suppression.
R10 (SUB)	Channel Subaddress Enable (enabled when SUB=Ø).
R11 (EEN)	ECL Readout Enable. EEN=1 ECL Port Readout EEN=Ø CAMAC Readout
R12 (OVF)	Overflow Indication Enable (enabled when OVF=Ø)
R13 (CCE) R14 (CSR)	Acquisition and Readout Control: - With zero suppression (sequential readout) CSR=1 and CCE=1 - Without zero suppression (sequential readout) CSR=1 and CCE=Ø - Addressed readout (without zero suppression) CSR=Ø and CCE=X
R15 (CLE)	CAMAC LAM Enable (enabled when CLE=1)
F8 - A(Ø)	Tests LAM. Q=1 if LAM is pre
F9 . A(Ø)	Clears the Module
F10 . A(Ø)	Clears LAM
F16 . A(Ø-7)	Reserved for ADC 4418/Q
F17 . A(Ø-7)	Writes Threshold Memory (Upp Threshold - ULD)
F17 . A(8-15)	Writes Threshold Memory (Lov Threshold - LLD)
F20 . A(Ø-7)	Writes Offset Memory
F20 . A(9)	Writes Common Threshold
F20 . A(14)	Writes Status Word
F25 . A(Ø)	Test Function

Readout Format

Note: EEN, CSR and CCE are Status Word bits (see Status Word)

1) With zero suppression (sequential readout):
   CSR=1 CCE=1
   EEN=1 ECL Port Readout
   EEN=Ø CAMAC Readout



VSN : Virtual Station Number; loaded in the associated Memory
VDC : Number of Valid Data following Pattern Word (from 1 to 8)
PW : Valid Data View: R1 is referred to channel Ø R8 is referred to channel 7
OVF : Overflow Indication; enabled with OVF=Ø (Status Word bit)
SUB : Channel Subaddress, enabled with SUB=Ø (Status Word bit)
DATA : 12-bit output Data

1.1 FRONT PANEL

ECL BUS
(section 1.10.1)

BUSY LED

BUSY = BUSY output
WST = write strobe line
REQ = request bus line
CLR = fast CLEAR
GATE = GATE input
WAK = write acknowledge
GND = GROUND

RDE = readout enable input
NEXT = readout enable output

} ECL LEVEL differential

LED on if matching and pull-down resistors are mounted on the ECL BUS (section 1.10.1)

Analog inputs IN signal (section 1.3)
⏚ ground

LED on if data bus pull-down resistors are mounted on the ECL DATA BUS (section 1.10)

ECL DATA bus outputs (section 1.10)

Last 2 pins not connected

1.2 General

The SILENA Mod. 4418/V ADC incorporates 8 analog memories with associated peak detectors and linear gates provided with thresholds featuring a common level adjustable via a CAMAC-programmable 8-bit DAC.

The analog memories outputs are routed, through an analog multiplexer, to a fast analog-to-digital converter (3/uS) featuring offset control and two thresholds : a lower (LLD) and an upper (ULD) threshold.

This makes it possible to assign different threshold and offset (zero energy intercept) values to each measuring channel.

A "Parameters Memory" contains the LLD, ULD and OFFSET values of each single channel, as well as the input common threshold value.

A 6-bit register (STATUS REGISTER) allows different data acquisition and readout modes of the 8 measuring channels.

Data may be read-out either via CAMAC or via the ECL Data Bus, depending upon the Status Register state.

Both the Status Register and Parameters Memory must be previously loaded via CAMAC.

If enabled, the ECL Data Bus, located on the front-panel, sends analog-to-digital conversion data sequentially in words of 16 bits with differential ECL levels (the first 12 bits are data bits plus 3 subaddress bits, plus the "Overflow" bit, if it exists).

A REQ output signal is generated when the ECL Data Bus is ready to deliver data.

In CAMAC mode, data is always read in 16 bit words in either sequential (Q stop mode) or addressed mode.
When data is ready, a LAM signal may be generated and there is Q=1 with the readout function N.F(Ø) or N.F(2).
The instrument includes provisions for testing the 8 input modules of the 4418/V ADC via a CAMAC-controlled TEST signal with function N.F(25) . A(Ø).
This signal simulates a GATE command and applies a pulse corresponding to about 1/6 of the dynamics to the input of each channel.
The ADC may be in any of two states: "Idle" or "Busy", depending on the GATE, CLEAR and internal CLEAR signals. (Internal CLEAR is applied after a conversion if there is no valid data or when data readout is performed in sequential mode).
GATE and CLEAR may be sent either via front-panel (ECL Command Bus) or via CAMAC.
After a CLEAR signal, the ADC is in the "Idle" state, that is it is ready to receive a GATE signal (front-panel or test).
The Status Register and the Parameters Memory may be loaded only when the module is in the "Idle"state.
The GATE signal (front-panel or test) causes the ADC to go to the "Busy" state, during which no further GATE signal is allowed.
Data conversion is enabled approximately 1 µS after the GATE signal, and at the end of the conversion time data readout is initiated.
At this point, depending on the state of the Status Register and the data converted by the ADC, any of three conditions may occur :

- Data readout via ECL port only (EEN = 1, see Status Register).
- Data readout via CAMAC only (EEN = Ø).
- No data to be read. In this case, no data readout is performed.

During the "Busy" state, to disable the ongoing data conversion or to accept further GATE signals, it is necessary to apply a CLEAR signal.
The ADC is ready to perform a new data acquisition 1,2/uS after the CLEAR signal

1.3 Analog Inputs

The 8 analog inputs are designed for positive signals.
Input impedance is 1KΩ with respect to the ground.
When long-distance cables and short pulse shaping times are used (i.e. 0,5/uS), it is advisable to replace the 1KΩ resistor with a resistor corresponding to the impedance of the cable used.
A threshold value common to all 8 inputs must be programmed via CAMAC to prevent the input noise associated with the gate signal from generating busy time.

1.4 CLEAR Function

The CLEAR function may be enabled either by an ECL CLEAR command of the front-panel ECL Bus or by CAMAC functions Z,C and N.F(9) . A(Ø) strobed by S2 or by an internal command generated after completion of sequential data readout or at the end of conversion, if no valid data is present.
After a CLEAR signal, the ADC changes to the "Idle" state and is held in this state until the next GATE signal is applied.
During the CLEAR signal (duration of about 1,2/uS) the input GATE is inhibited.
It is recommended to avoid sending new GATE commands in coincidence with the end of the CLEAR signal.
This will prevent generation of sliced GATE commands.

1.5 External GATE Input

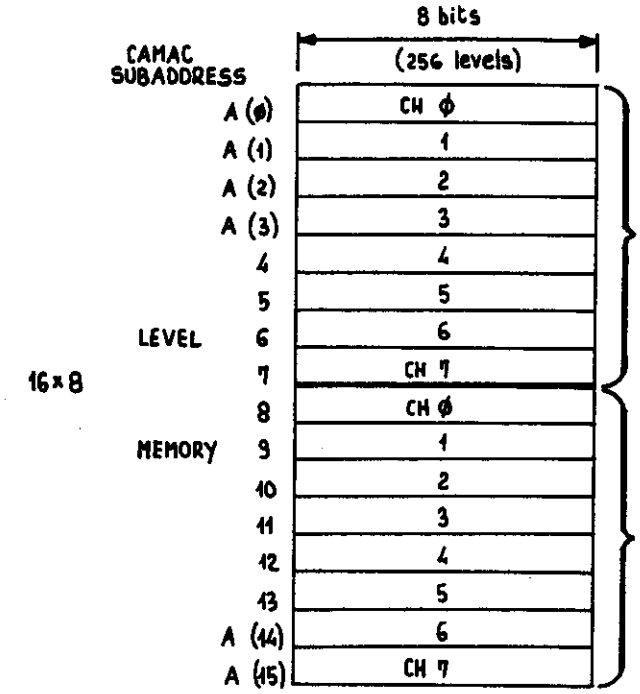
The GATE command should be sent only when the module is in the "Idle" state.
It should never be sent in coincidence with the CLEAR signal (at least 1,2 /uS after the CLEAR function has been initialized).
The GATE input may be inhibited by line I (CAMAC inhibit).
A GATE signal activates the following functions:

- Enable the Peak Detector circuit and hold the peak value
- The end of the GATE signal automatically inhibits the GATE input disabling further GATE signals.

After a 1/uS time delay it starts conversion, causing the ADC to change to the "Busy" state.
For optimum results the GATE signal must be applied delayed with respect to the analog signal, but before the pulse to be measured reaches its peak, and must be maintained at least up to this instant.

1.6 ADC Thresholds - Offset Memory

The 4418/V ADC includes a Parameters Memory made up of two 16x8 words groups. With the module in the "Idle" state, the threshold values (Low Level Discriminator-LLD; Upper Level Discriminator ULD), as well as the Offset, Common Threshold and VSN (Virtual Station Number) values can be loaded into the Parameters Memory. Different threshold (ULD and LLD) and offset values may be assigned to each input; whereas the threshold is common to all the 8 input modules.
A schematic diagram of the ADC Parameters Memory is illustrated in the following drawing.



ULD value

Ø corresponds to 85% full scale
255 corresponds to 100% full scale

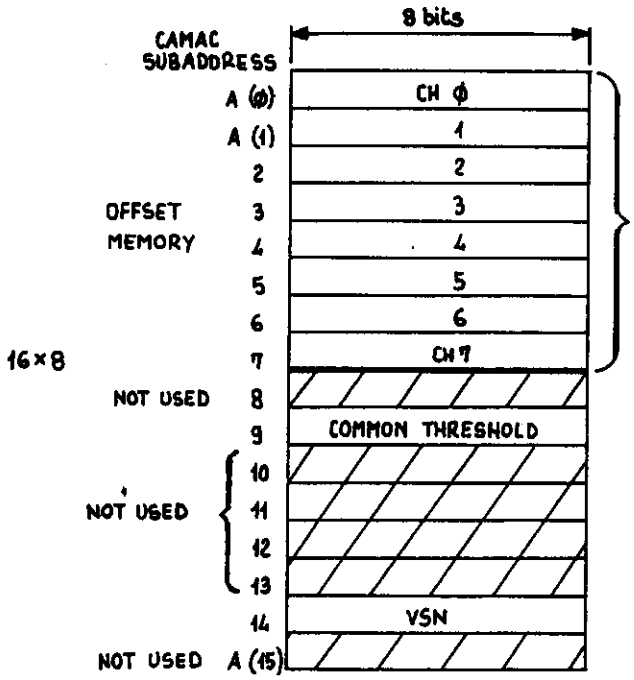
CAMAC FUNCTIONS

Read N.F1.A(Ø-7)
Write N.F17.A(Ø-7)

LLD value

Ø corresponds to Ø% full scale
255 corresponds to 10% full scale

Read N.F1.A(8-15)
Write N.F17.A(8-15)



OFFSET value

128=Ø
Ø=-3% of full scale
255=+3% of full scale

CAMAC FUNCTIONS

Read N.F4.A(Ø-7)
Write N.F20.A(Ø-7)

Ø = Ø
255 = 1,2 Volt

Read N.F4.A(9)
Write N.F20.A(9)

VSN = Logical Address (Ø ÷ 255)for the Module : index source sequential readout with zero suppression

Read N.F4.A(14)
Write N.F20.A(14)

ADC 4418/V PARAMETERS MEMORY

1.7 Test Function

The TEST function is initiated by the CAMAC command N.F(25).A(Ø) strobed by S2. If accepted, Q is equal to 1.
This function is accepted only when the ADC is in the "Idle" state.
This function performs the following operations:

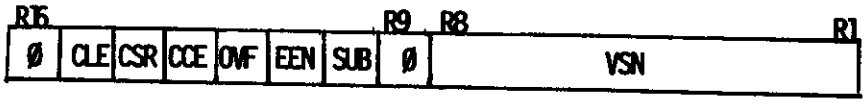
- Applies a voltage pulse to the analog memories inputs.
- Generates a GATE signal in coincidence with the pulse peak. During the entire duration of this pulse no signal is allowed on any of the analog inputs, even if the interconneting cable may remain connected.
  The GATE command (front panel) must not be sent while the Test function is in progress.

1.8 Overflow

The ADC actual dynamics is 3840 channels (4096-256) - 256 channels are reserved for the Sliding Scale Circuit.
Data having a content greater than or equal to 3840 is not considered to be valid for measurement.
If this data is present, an Overflow indication is generated by the ADC control circuit.
Via the Status Register bit (R12) (See Status Register) it is possible to enable the Data Memory to associate the Overflow information with the conversion Data and store it into the DATA WORD at position R16 (see ECL or CAMAC Data Structures),

1.9 Status Register

The Status Register is a memory into which the Status Word is loaded.
The Status Register is made up of two distinct sections.
The first (low order 8-bit) consists of a word of the Parameters Memory and contains the address number of the module (VSN-Virtual Station Number).
This is used to identify the data source during sequential readout with zero suppression mode.
The other section contains the information that determines the data acquisition and readout modes.
The Status Register is written by the CAMAC function N.F20.A(14) strobed by S1 and is readout by function N.F4.A(14).
These two functions are accepted only when the module is in the "Idle" state; there is Q response when the functions are accepted.
After switching on the module, the content of the Status Register is undefined. The CAMAC initialization function (Z) sets the 6 Status Register bits (R10 through R16) to the "1" state, but will not affect the VSN register, whose content remains undefined.
The other CLEAR signals will not reset the Status Register.



The six functions of the Status Register are as follows :

SUB (W10-R10) Channel Subaddress Enable

If enabled (SUB=Ø), in addition to the ADC data, the binary addresses of the 8 analog memories (Ø for the Ø channel, etc.) are loaded into the Data Memory at positions R13, R14, R15.
If SUB=1, the value of R13-R14-R15 in the Data Word is always "zero".

EEN (W11-R11) ECL Bus Enable

If EEN =1, only the ECL port readout is enabled.
If EEN =Ø, only CAMAC readout is enabled.

OVF (W12-R12) Overflow Indication Enable

If OVF =Ø, the Overflow indication, if it exists, is loaded into the Data Memory at position R16.
If OVF =1, the value of R16 in the Data Memory is always "zero".

CCE (W13-R13) Zero Suppression Enable

CSR (W14-R14) Sequential Readout Enable

These two bits allow 3 different data acquisition and readout modes to be performed.

- "With Zero Suppression" CSR = 1 and CCE = 1

  Data conversion takes place only in valid channels (i.e. channels with pulses above the Common Threshold and falling within the LLD-ULD window).
  These valid channels are readout in sequential mode either via the ECL bus or CAMAC.

- "Without Zero Suppression" CSR=1 and CCE=Ø

  All the 8 input channels are converted and read sequentially.

  Readout may be either via the ECL BUS or CAMAC.

- "Addressed Readout" CSR=Ø and CCE=Indifferent.

  All the 8 channels are converted and the ADC data is read by CAMAC only in addressed mode with any of two functions N.F(Ø).A(Ø-7) or N.F(2).A(Ø-7). The read-out channel is identified by Subaddress A: A(Ø) = channel Ø etc.

CLE (W15-R15) CAMAC LAM Enable

If CLE =1, the LAM output is enabled to indicate that there is valid data to be read by CAMAC; in the "Zero Suppression" mode, if no valid data is present, LAM will not be enabled.

If CLE = Ø, the LAM output will be disabled.

NOTE: After the CAMAC initialization (Z) the 6 bits of the Status Register are set to "1". This means : "With Zero Suppression mode", ECL readout, SUB and OVF disabled.

1.10 ECL Data Bus

The module delivers 16-bit data words with complementary ECL outputs at the ECL Data Bus connector.
The maximum readout frequency is 8 MHz.
If several modules are connected, the pull-down resistors must be removed in all modules, except for the last module (see fig. 1.3).
When these resistors are mounted, the associated EED indicator is lighted.
If several modules are connected, only the positive ECL output is used; the negative output should be connected to ground.
See Section 1.10.3 for data structure.

1.10.1 ECL BUS - RDE/NEXT

In addition to the ECL CLEAR and GATE signals, all those signals with ECL levels that control and allow use of the ECL DATA Read-out are present at the ECL Bus and RDE/NEXT connectors.
These signals include :

° **Request Output (REQ):**

Indicates that the module is ready to send data to the ECL Data Bus. The REQ signal is generated at the end of conversion if the bit related to ECL Readout in the Status Register has been set.
The REQ signal remains until after the last data word has been read or a CLEAR command has been given.

° **Write Strobe Output (WST)**

Indicates the time period during which the data word present on the ECL Data Bus can be stored in the external memory.
WST is generated a minimum of 10 ns after the data is ready.
Its width is higher than 40 ns.
The ECL Data Bus data is maintained stable as long as the WST pulse lasts.

° **Write Acknowledge Input (WAK)**

This input receives the acknowledge signal indicating that the data present on the ECL Bus has been loaded into memory and the next data word may be sent.
The next WST signal is generated at least 50 ns after the WAK signal.
Minimum WAK width must be 30 ns.

° **Busy Output (BUSY)**

This output is set to the "1" state 1/uS after the end of the GATE signal and is held to this state until after the end of the readout cycle (ECL Readout or CAMAC Readout).
The BUSY state may be reset only by sending a CLEAR signal via CAMAC or via ECL Bus (CLR).
The ADC is ready to start a new conversion 1,2/uS after the end of the BUSY state.

ECL PORT ENABLE/NEXT

° **Readout Enable Input (RDE)**

The RDE signal indicates to the module that it can take control of the ECL Data Bus; RDE must be maintained during the entire readout time.

The signal enables the ECL Data Bus, WST Output and WAK input if the module is ready for data transfer (REQ output ON).
If there is no data present (REQ=OFF) the RDE signal automatically generates the NEXT signal, which becomes RDE for the next module.

° **Next Output (NEXT)**

Indicates that the module is not ready to transfer data present on the ECL Data Bus or it has completed data transfer.
The NEXT output signal is generated by the RDE line in the absence of the REQ internal command or, if this command is present, at the end of data readout.
The transit time between the RDE and NEXT output is typically 3 ns (6 ns max) if the module does not include data readout capabilities.

As previously mentioned for the ECL Data Bus, if several modules are connected, it is necessary to remove the pull-down resistors in all modules, except for the last one.
The LED indicator is lighted when the resistors are mounted. (see fig. 1.3).
The timing sequence of ECL Data transfer is described in the following.

1. After data conversion, the ADC module sends the REQ signal and waits for the RDE Readout Enable.
2. An external driver provides the RDE line.
3. The RDE signal clocks the internal flip-flop in the requesting ADC module and inhibits the NEXT output. The non-requesting ADC's closer to the driver are disabled by the same RDE signal.

The non-requesting ADCs far away from the driver do not receive the RDE signal because it is stopped in the requesting module (no NEXT signal).
Moreover the RDE signal sets the WST line high and enables the first data word to transit through the ECL Data Bus.
The module remains in this state waiting for the WAK signal.
As soon as the WAK signal is received,the WST signal is released and is held to this position for at least 60 ns by an internal protection.
During this time the module makes available the next data word which is loaded into the ECL Data Bus with the leading edge of the next WST signal.

4. After the last data word from an ADC has been read, the request REQ signal is removed and the RDE signal is routed to the NEXT output, thus enabling readout of the next ADC module.

5. If a far off ADC has sent in a request, the common REQ line remains high and data readout from this module is initiated.

6. If a module closer to the driver has data ready, it waits until the RDE signal goes low and as soon as this occurs it sends its own REQ signal.
(This module was disabled by the RDE signal).

1.10.2 ECL Bus Readout Interrupt

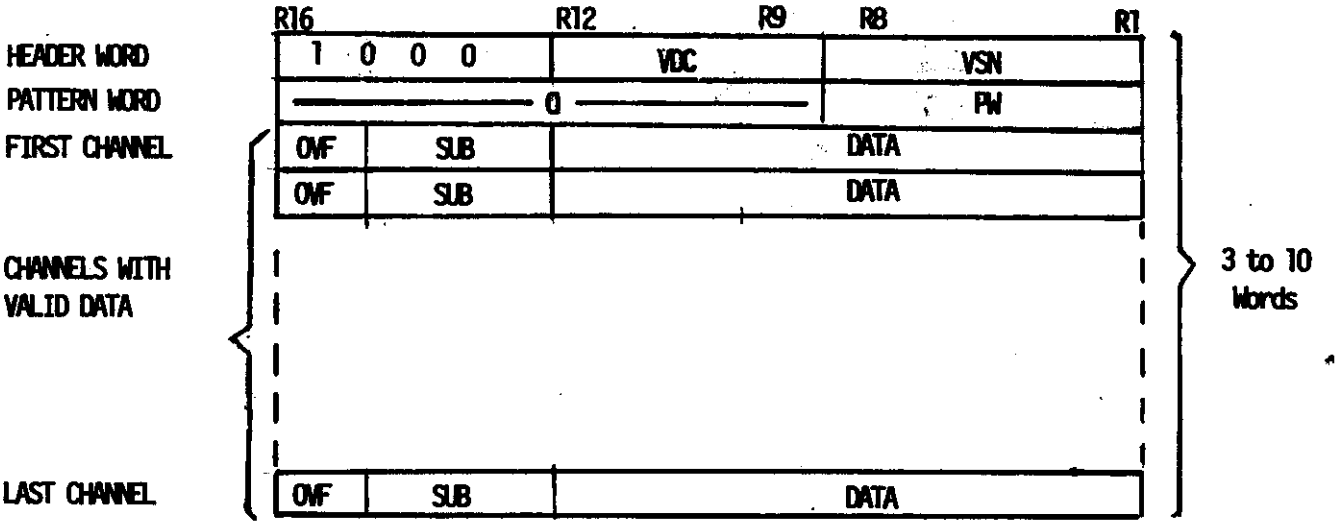
An ongoing ECL Bus readout may be momentarily interrupted in two different ways.

- By not sending a WAK signal after a WST signal.
  In this case, the data word on the ECL Data Bus remains until the WAK signal is received.
- By interrupting the WAK signal, stopping it after the first transition. If this occurs, the WST command is terminated and the next data word is placed on the ECL Data Bus, but it is only upon release of the WAK signal that the next WST will be activated again.

1.10.3 ECL Data Structures

NOTE: EEN, CSR and CCE are STATUS WORD bits.

1) **EEN=1, CSR=1, CCE=1**



Zero suppression is on. Up to 8 data words is to be read. Sequential readout only is possible on ECL BUS. Bit 16=OVF (overflow) is enabled when OVF-bit in Status Register is Ø.

Subaddress bits are enabled when SUB bit in S.R. is Ø.

2) **EEN=1, CSR=1, CCE=Ø**

R16	R12	R8 R4 R1	Offset
OVF	SUB	Ø-DATA	1
OVF	SUB	1-DATA	2
OVF	SUB	2-DATA	3
OVF	SUB	3-DATA	4
OVF	SUB	4-DATA	5
OVF	SUB	5-DATA	6
OVF	SUB	6-DATA	7
OVF	SUB	7-DATA	8

Always 8 data words are to be readout. Sequential readout only is possible on ECL BUS.

Bit 16=OVF (overflow) is enabled when OVF-bit in Status Register is Ø.

Subaddress bits are enabled when SUB bit in S.R. is Ø.

1.11 CAMAC Commands and Functions

NOTE :

If the module is in BUSY Status (BUSY LED on), only data readout and clear functions can be executed. Busy is released after clear and when all data is readout.

The BUSY line is connected on the Common ECL Bus.

F(0) A (0)

Reads the data memory sequential (CSR=1). Memory address is incremented with S2. Q-response is 1 if there is the data to be readout.

F(0) A (0-7)

Reads data addressed (CSR=0). Q-response is 1 if there is the data to be readout.

F(0) A (14)

Reads Header Word (Q=1 if module is in BUSY status).

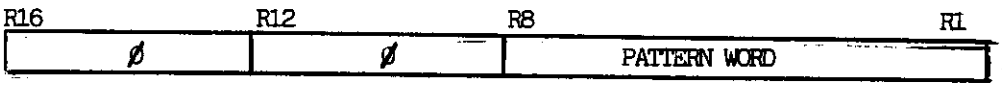
HEADER WORD

Header Word contains an information about the logical address of the module (VSN virtual station number bit 1-8) loaded to STATUS REGISTER, and an information about a number of valid data (VDC valid data counter). Q-response is 1 if there is the data to be readout.

F (Ø) A (15)

Reads Pattern Word (Q=1 if module is in BUSY Status)

PATTERN WORD



Pattern Word contains a bit muster that shows which channel has a valid data. Bit R1 corresponds to ch.Ø.

F(1) A (Ø-7)

Reads threshold Memory (upper threshold). Q=1 if BUSY=Ø

F(1) A (8-15)

Reads threshold Memory (lower threshold). Q=1 if BUSY=Ø

F(2) A (Ø)

Reads the data memory sequential (CSR=1). Memory address is incremented with S2. Q-response is 1 if there is the data to be readout.

F(2) A(Ø-7)

Reads data addressed (CSR=Ø) and clears with F(2)A(7) strobed on S2. Q-response is 1 if there is the data to be readout.

F(2) A (14)

Reads Header Word in data addressed mode (CSR=Ø)(Q=1 if module is in BUSY status).

F(2) A (15)

Reads Pattern Word and clears LAM (Q=1 if module is in BUSY status).

F(4) A(Ø-7)

Reads offset memory (Q=1 if module isn't in BUSY status).

F(4) A(9)

Reads common threshold (Q=1 if module isn't in BUSY status).

F(4) A(14)

Reads Status Word Register (Q=1 if module isn't in BUSY status).

F(8) A (Ø)

Tests LAM. Q=1 if LAM is set.

F(9) A (Ø)

Clears ADC and control logic. Doesn't clear memories and status register.

F(10) A (Ø)

Clears LAM . Q=1

F(16) A (Ø-7)

Reserved for ADC 4418/Q

F(17) A (Ø-7)

Writes threshold memory (upper thr.). 8 bits (Ø-255) correspond to 85-100% full scale. (Q=1 if module isn't in BUSY status).

F(17) A (8-15)

Writes threshold memory (lower thr.). 8 bits (Ø-255) correspond to Ø-10% full scale. (Q=1 if module isn't in BUSY Status).

F (20) A (Ø-7)

Writes offset memory. 8 bits (Ø-255) correspond to ±3% of full scale. 128 correspond to ØV. (Q=1 if module isn't in BUSY status).

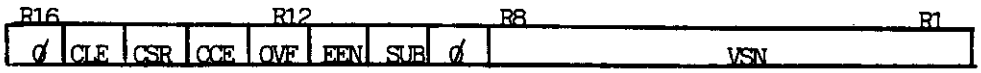
F(20) A (9)

Write common threshold 8 bits (Ø-255). (Q=1 if module isn't in BUSY status).

F(20) A (14)

Writes Status Word Register (Q=1 if module isn't in BUSY status).

STATUS WORD



R1-R8 (VSN) Logical address of the Module

R10 (SUB) when SUB=Ø subaddress enabled (see data structure)

R11 (EEN) when EEN=1, ECL readout enabled (EEN=Ø ⇒CAMAC enabled)

R12 (OVF) when OVF=Ø, the overflow bit enabled (see data structure)

R13 (CCE) when CCE=1, zero suppression enabled, only if CSR=1

R14 (CSR) when CSR=1, CAMAC sequential readout enabled

R15 (CLE) when CLE=1, CAMAC LAM enabled.

NOTE:

The all bits of S.W.R. are set to 1 by CAMAC Z=init. function

F(25) A (Ø)

Test function (Q=1 if module isn't in BUSY status).

Z:

Initialize; clears the module and sets the Status Register bits 9-16 to 1. Does not clear the memory.

C:

Clears the Module. Does not clear the Status Register and memory.

I:

Inhibits the Gate input.

X:

X response is generated for all valid functions.

Q:

Q response is generated when the function can be executed.

L:

LAM set, if enabled, after the end of conversion and if there is valid Data to be read.

The Status Word Register CLE, CSR, CCE, OVF, EEN, SUB bits, VSN - virtual station number and Parameters Memory must be written before acquisition begins.

1.11.1 CAMAC Readout

CAMAC Readout may be performed in either "sequential" mode or "addressed" mode, depending upon the state of the CSR bit of the Status Register.

CSR = 1 enables "Sequential Readout": at the end of the conversion cycle the first data word is available on the CAMAC Dataway. The Q response is given as long as there is data to be read. After the last data word has been read, the internal CLEAR signal causes the ADC to go to the "Idle" state. Data is read with functions N.F(Ø).A(Ø) or N.F2.A(Ø).
On completion of the readout of each single data word (at the end of S2) the address of the ADC Data Memory is incremented and the next data word is sent.

CSR = Ø enables "Addressed Readout": at the end of the conversion cycle, the various channels can be read by addressing the channel to be read via CAMAC with Subaddress A.
Readout functions are N.F(Ø).A(Ø-7) or N.F.(2).A(Ø-7).
With function N.F(Ø).A(Ø-7) the Q response is given each time a data word is read and the module is maintained enabled to send the requested data until a CLEAR function is released.
With function N.F(2).A(Ø-7) the Q response is given each time a data word is read but the CLEAR function is automatically generated by Subaddress 7 [N.F(2).A(7)] strobed by S2.

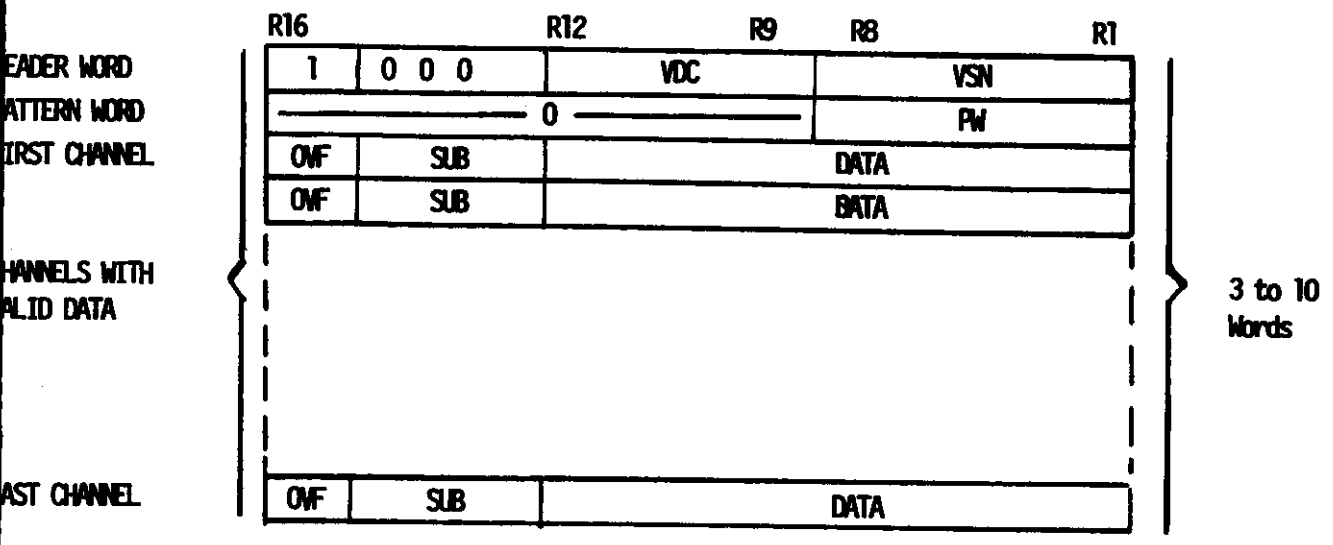
1.11.2 LAM Handling

The LAM (Look-at-me) is activated when the related bit of the Status Register is set to "1". It is activated as soon as data is ready for CAMAC readout. During "Sequential Readout" the LAM is reset after the last data word has been read.
Function N.F(8).A(Ø) is used to test the state of the LAM.
Q = 1 if the LAM is present.
The LAM may also be cleared by the following functions ECL CLEAR + front panel, Z, C, N.F(9).A(Ø) strobed by S2.

1.11.3 CAMAC Data Structures

NOTE : EEN, CSR and CCE are Status Word bits.

1) **Read Data F(Ø)A(Ø), F(2)A(Ø), EEN=Ø, CSR=1, CCE=1**



Zero suppression is on. Up to 8 data words are to be read.
Sequential readout is on. Bit 16=OVF (overflow) is enabled when OVF-bit in Status Register is Ø. Subaddress bits are eneabled when SUB bit in S.R. is Ø.

2) **Read Data F(Ø)A(Ø), F(2)A(Ø), EEN=Ø, CSR=1, CCE=Ø.**

R16		R12 R8 R4 R1	Offset
OVF	SUB	1-DATA	1
OVF	SUB	2-DATA	2
OVF	SUB	3-DATA	3
OVF	SUB	4-DATA	4
OVF	SUB	5-DATA	5
OVF	SUB	6-DATA	6
OVF	SUB	7-DATA	7
OVF	SUB	8-DATA	8

Always 8 data words are to be readout. Sequential readout is on.

HW can be read with F(Ø)A(14) or F(2)A(14).
PW can be read with F(Ø)A(15) or F(2)A(15).

Bit 16=OVF (overflow) is enabled when OVF bit in Status Register is Ø. Subaddress bits are enabled when SUB bit in S.R. IS Ø

3) **Read data F(Ø)A(Ø-7), F(2)A(Ø-7), EEN=Ø, CSR=Ø, CCE=X**

R16		R12	R8	R4	R1	Offset
OVF	SBB	A(Ø)+DATA				1
OVF	SUB	A(1)-DATA				2
OVF	SUB	A(2)-DATA				3
OVF	SUB	A(3)-DATA				4
OVF	SUB	A(4)-DATA				5
OVF	SUB	A(5)-DATA				6
OVF	SUB	A(6)-DATA				7
OVF	SUB	A(7)-DATA				8

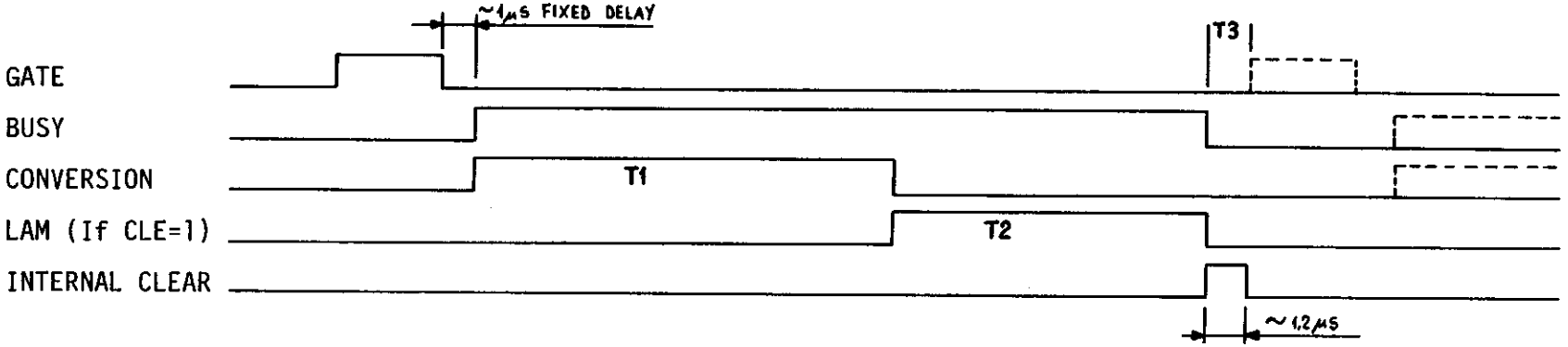
CAMAC Addressed (random) readout. Bit 16=OVF (overflow) is enabled when OVF bit in Status Register is Ø. Subaddress bits are enabled when SUB bit in Status Register is Ø.

1.12 Readout Timing Diagram

The Figures (Fig. 1.1 and 1.2) in the next two pages show the readout timing sequence via CAMAC and via ECL BUS.

Acquisition and CAMAC Readout Timing

NOTE: This diagram does not define the logic state of the signals: Low=FALSE High=TRUE



T1 depends on CSR and CCE status

CSR=1 and CCE=1	T1= N.4/uS	(N=number of valid channels)
CSR=1 and CCE=Ø or CSR=Ø and CCE=X	T1=32/uS	

T2 depends on CSR and CCE status

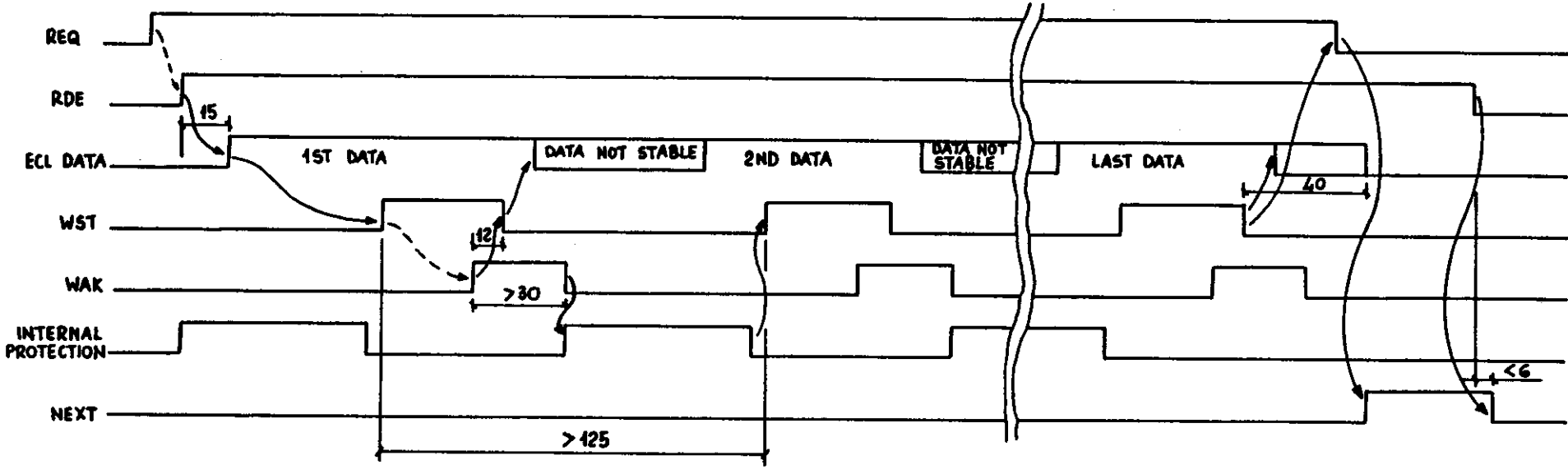
CSR=1 and CCE=1	T2=(2+N).t	(N=number of valid channels; t=single CAMAC readout period)
CSR=1 and CCE=Ø	T2=8.t	
CSR=Ø and CCE=X	T2 with function N.F(Ø).A(Ø-7) terminates upon release of the CLEAR function; with function N.F(2).A(Ø-7) terminates with function N.F(2).A(7) strobed by S2	

T3 protection time : next gate must follow the end of LAM for at least 1,2/us

- FIG. 1.1. -

ECL BUS TIMING

NOTE : THIS DIAGRAM DOES NOT DEFINE THE LOGIC STATE OF THE SIGNALS ; LOW = FALSE HIGH = TRUE



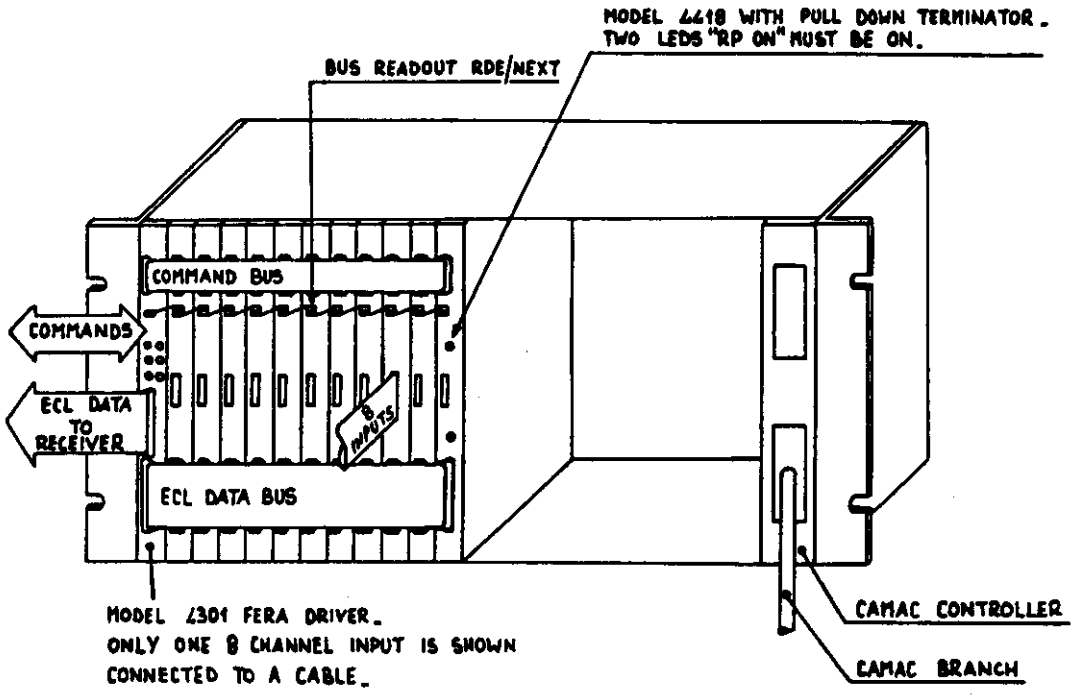
INTERNAL ACTION

EXTERNAL DRIVER ACTION

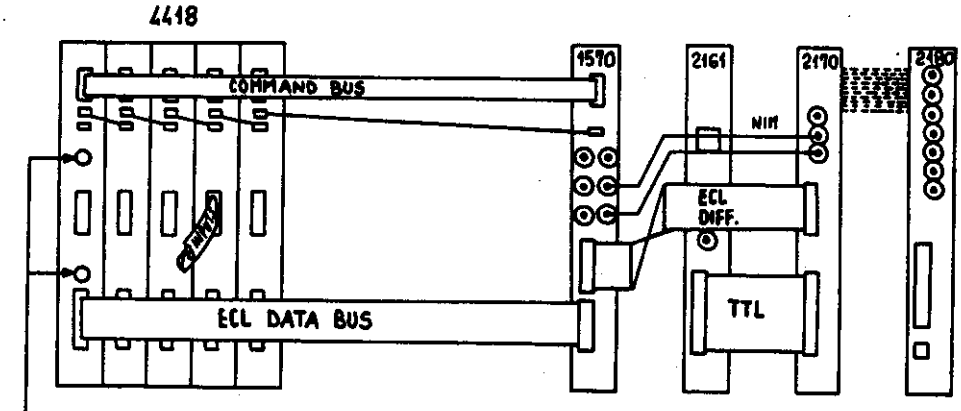
TIME INDICATION IN n SEC, TYPICAL

4418-FIG. 1.2

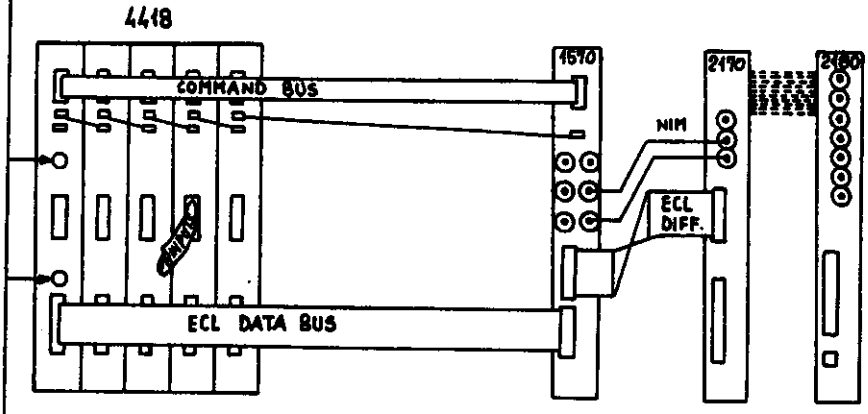
1.13 FERA SYSTEM CONNECTIONS



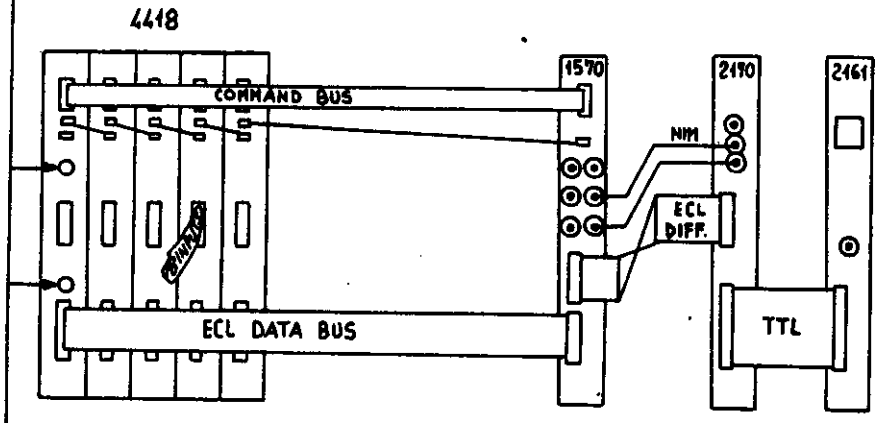
1.14 CES SYSTEM CONNECTION



LIST MODE THROUGH 2180
HIST MODE THROUGH 2161



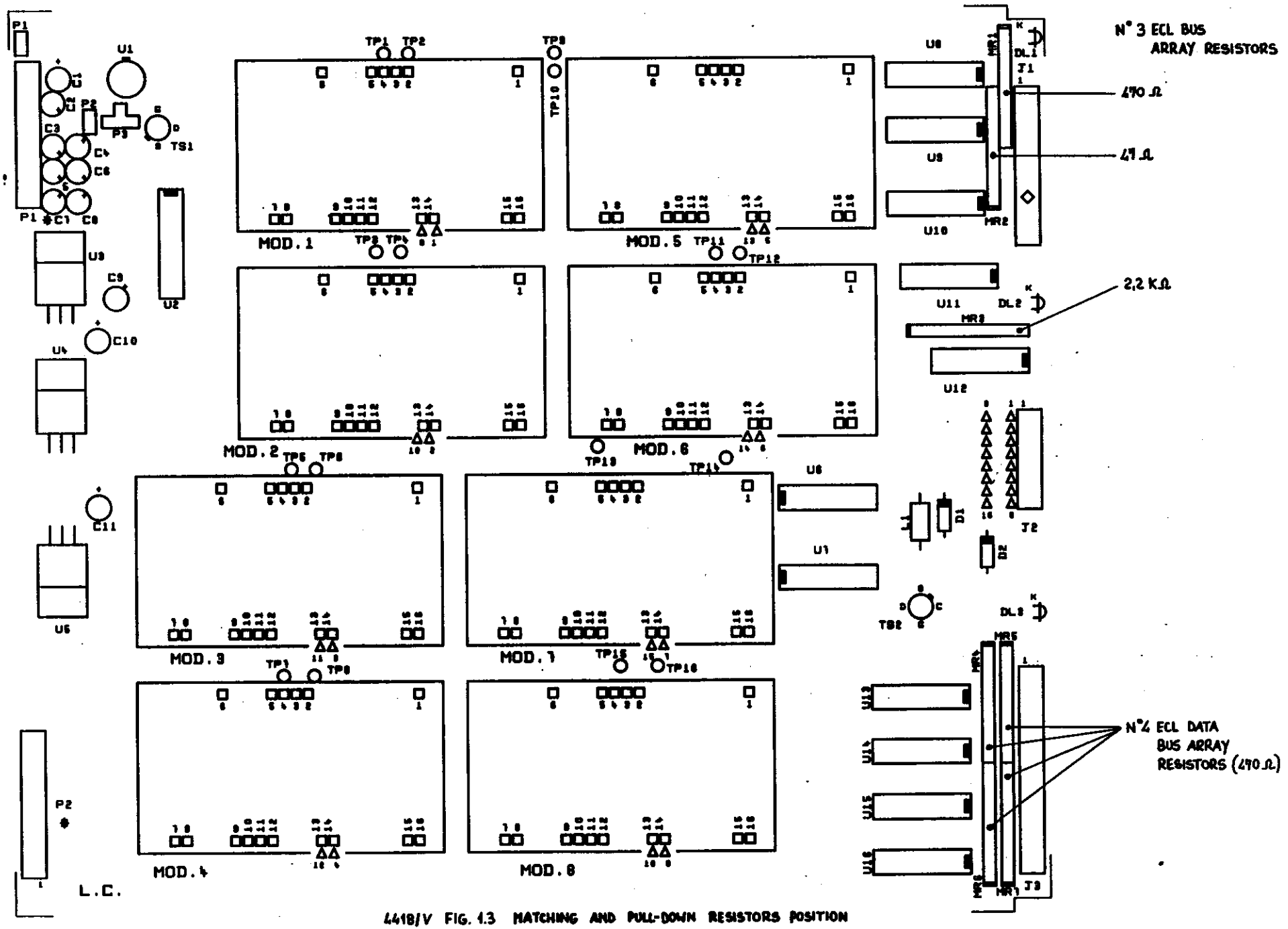
LIST MODE THROUGH 2180



MODEL 4418 WITH PULL DOWN TERMINATOR.
TWO LEDS "RP ON" MUST BE ON

LIST OR HIST MODE THROUGH 2161

ONLY ONE 8 CHANNEL INPUT IS SHOWN
CONNECTED TO A CABLE.



4418/V FIG. 1.3 MATCHING AND PULL-DOWN RESISTORS POSITION

2.1 General

The 4418/V module is made up with three types of printed board :

- A Mother Board including the GATE, test and ECL logic circuitry and the TTL → ECL adapting circuitry related to the front-panel Bus. This circuit also support the 8 analog modules.
- Eight analog modules (analog memories)
- A circuit including the Analog-to-Digital Converter, Thresholds, DAC's and the entire ADC logic circuitry.

2.2 Description (see fig. 2.1 and Fig. 2.2)

A GATE input signal or a monostable triggered by the TEST function N.F(25).A(Ø).S2 initiates the following sequence:

- Enables the peak detector and analog storage of the input pulse.
- At the end of the GATE signal, inhibits the front panel GATE input and trigger the "ΔT" monostable (waiting time for analog multiplexer setting time and LLD-ULD and offset preset).
- The end of the " ΔT" monostable sets "BUSY" state and starts conversion. During the "BUSY" state in the CAMAC decoder, all functions except the read out and CLEAR functions are disabled. Storage of the peak value of the input signal is individually performed for each single channel via a module using SMT (Surface Mounting Technology) mounting techiniques.

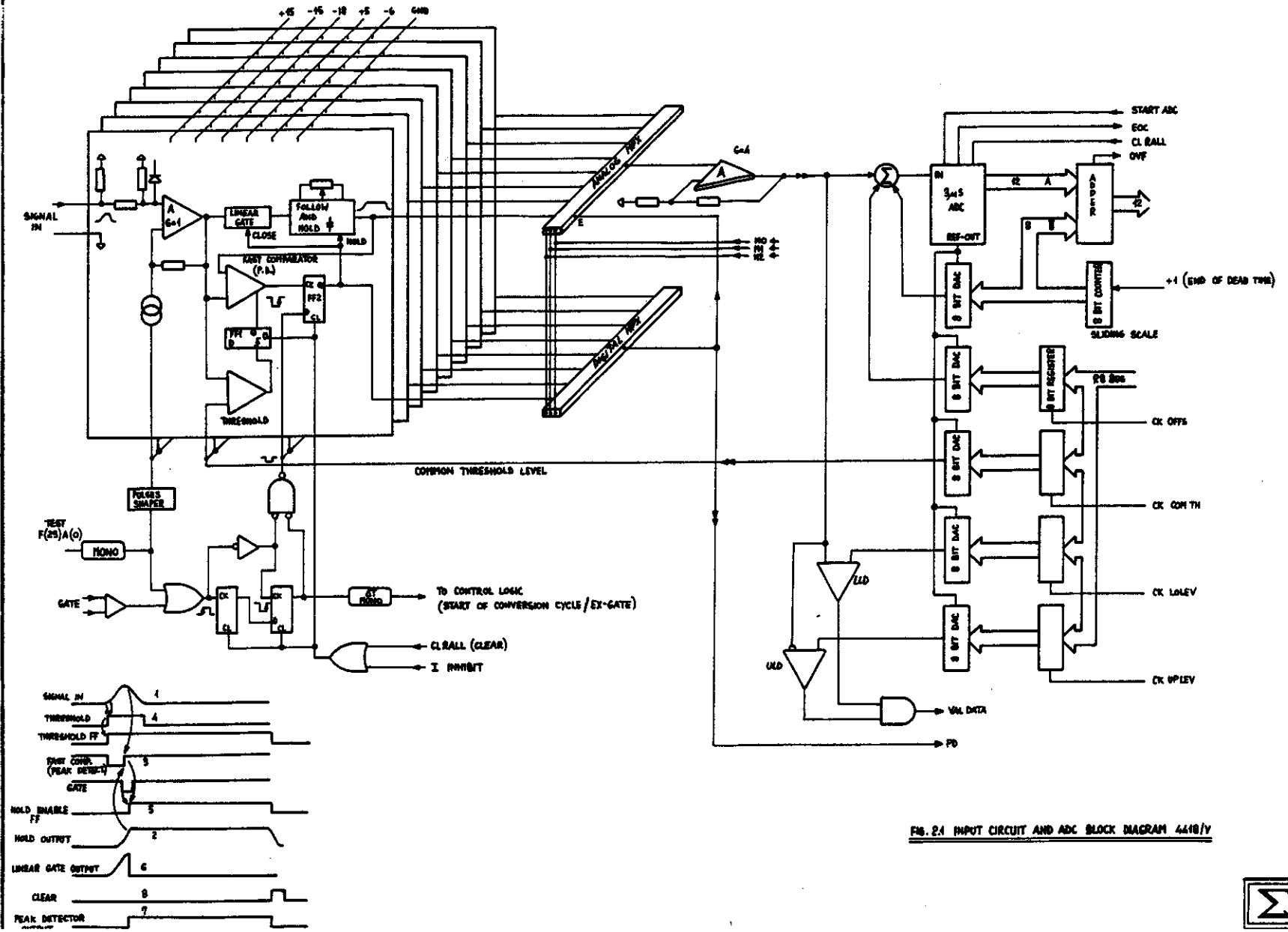


FIG. 2.1 INPUT CIRCUIT AND ADC BLOCK DIAGRAM 4418/V

SILENA S.p.A.
MILANO - ITALY

The operating principle is based upon comparison between the input and the output signal of a "Follow and Hold" circuit in order to determine the instant when the signal reaches the peak and then go from the "Follow" state to the "Hold" state.
The input signal, after passing through a 4 to 1 attenuator (10V F.s. to 2.5V F.s.) and a 1 gain amplifier, is applicated to the threshold circuit (*).

On overcoming the preset threshold value, flip-flop FF1 is set. This flip-flop activates the comparison (Fast Comparator) between the input signal and the output signal from the "Follow and Hold" circuit.

As soon as the input signal goes below the output signal the comparator sets flip-flop FF2.

This flip-flop inhibits the input linear GATE and sets the analog memory to the "Hold" position.

The analog outputs from the 8 modules are connected to an analog multiplexer. Three lines (MØ M1 and M2) sequentially select the inputs of both the analog and digital multiplexer (Peak Detector).

(*) NOTE:

Since the threshold circuit is d.c. coupled with the input, if a d.c. level overlaps the signal, the following error conditions will occur:

a) Positive DC level - The threshold isheld to the "ON" state and no peak is detected. The result is that the value converted by the ADC will be zero. Corrective action: the value of the Common Threshold should be incremented via CAMAC command

b) Negative DC level. - The input pulses lying between - VIN (DC) and V THRESHOLD are not accepted. Corrective action: the direct level should be corrected by external control.

Only if PEAK DETECTOR is ON the output from the analog MPX is enabled.

After being amplified by 4 (from 2.5V F.S. to 10V F.S.) it is routed to the ADC.

The ADC used is a successive approximation type (SAR) with correction of the differential linearity using the sliding scale method devised by Prof. E. GATTI.

The Common Threshold level is stored into the associated register through the CKCOMTH line during the "Idle" state via CAMAC function N.F(20).A(9).

The values of the Upper Threshold (ULD), Offset and Lower Threshold (LLD) of the 8 measurement inputs are stored into the Parameter Memory while the module is in the "Idle" state by the following functions:

N.F(17).A(0-7) ULD

N.F(17).A(8-15)LLD

N.F(20).A(0-7) OFFSET

These values are loaded into the associated registers before each single data conversion by the following commands :

CKUPLEV = loads the value in the upper level register
- 0 corresponds to 85% F.S
- 255 corresponds to 100%F.S.

CKOFFS = Loads the value in the offset register
- 0 corresponds to -3% F.S.
- 128 corresponds to 0
- 255 corresponds to +3% F.S.

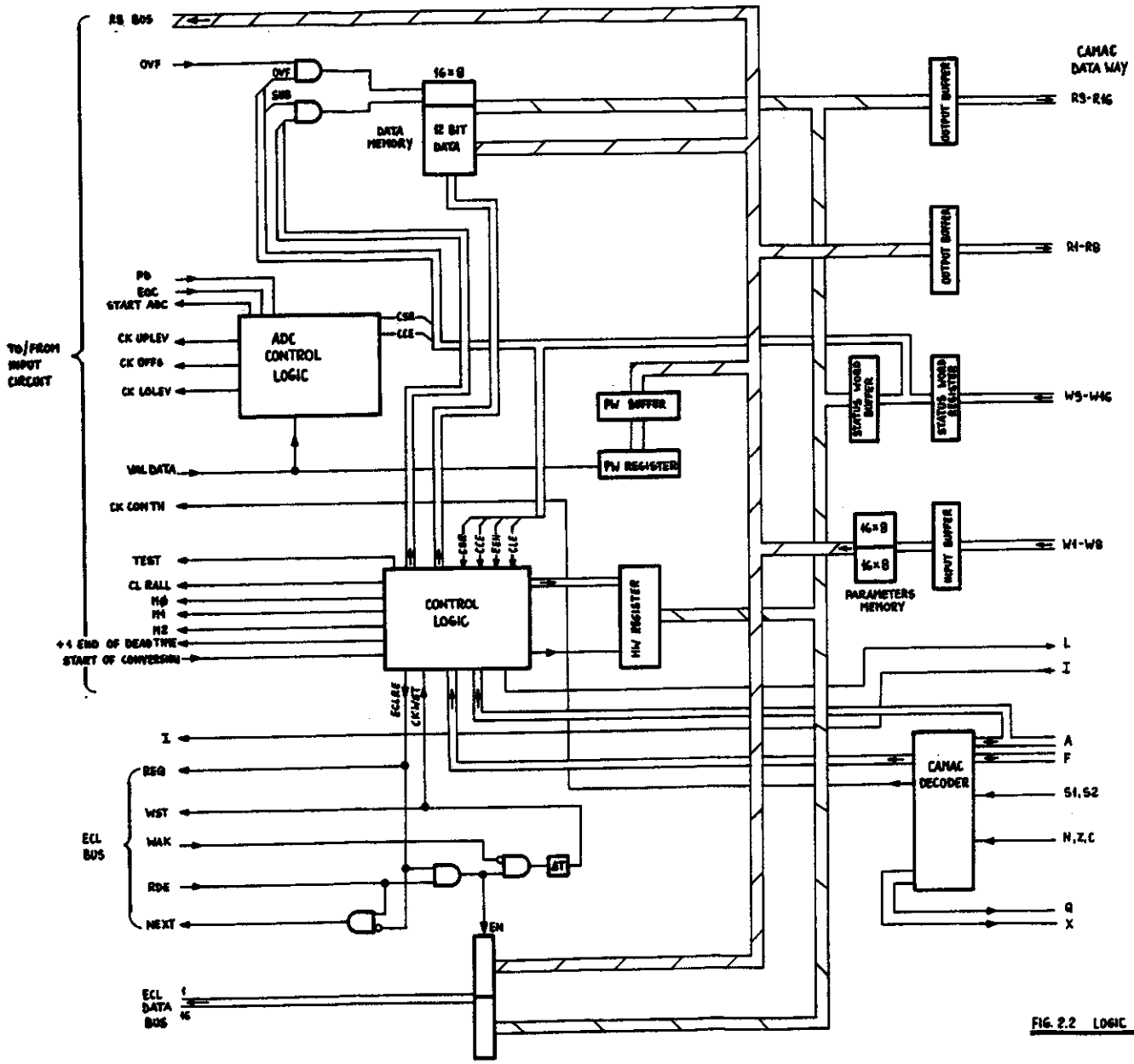


FIG. 2.2 LOGIC CIRCUIT BLOCK DIAGRAM 4418/V

SILENA S.p.A.
MILANO - ITALY

DWG.

CKLOLEV = loads the value in the lower level register Ø corresponds to Ø% F.S.

255 corresponds to 10% F.S.

If the module is set for operation in "Zero Suppression Mode" data conversion takes place only for the measuring channels with Peak Detector indication, provided that their values are higher than the preset LLD level and lower than the ULD level.

If the module is set for operation "Without Zero Suppression Mode" or "Addressed Readout Mode" data conversion takes place on all 8 inputs independently of the Peak Detector and threshold values.

The analog Multiplexer reamins inhibited in the presence of inputs without Peak Detector indication with the result that the converted value will be "zero volt" ± the preset offset value.

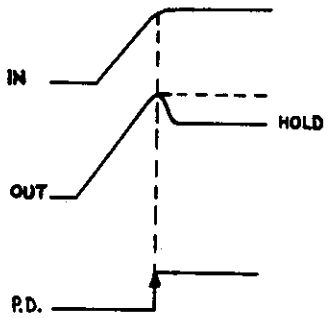
2.3 Acceptable Signal In and Gating Time

This paragraph provides information regardin acceptable input pulses and the sampling time (Gating Time) to be used to achieve the best results.

As mentioned in the technical specifications, the leading edge of the pulse is the main limitation.

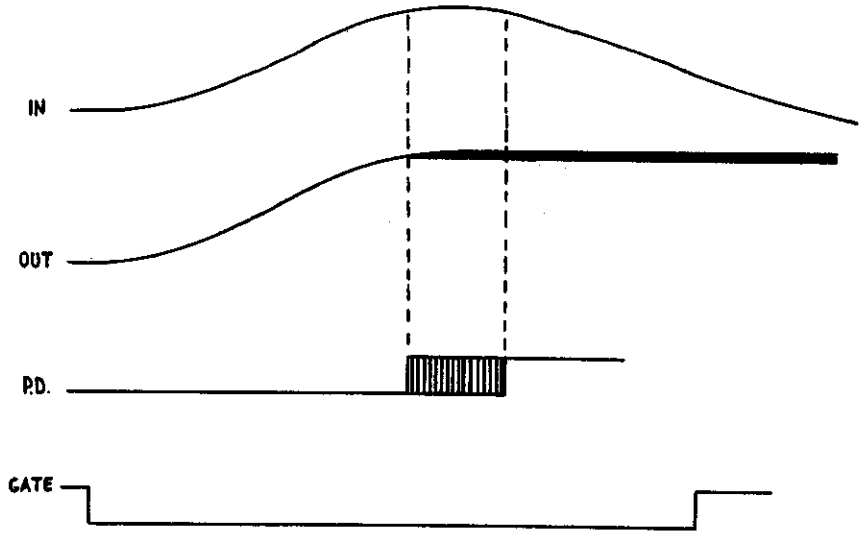
This should be $\geq 1/uS$ and $\leq 8/uS$.

With fast leading edge the main limitation is posed by the "Setting Time" of the "Follow and Hold" circuit, whose response to a fast step is as follows:

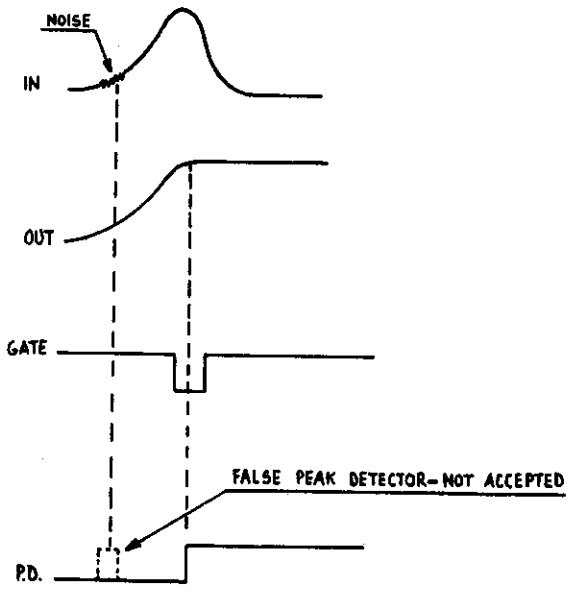


As can be seen, the peak detector is activated on occurrence of the output pulse overshoot with the result that an incorrect peak value is stored.

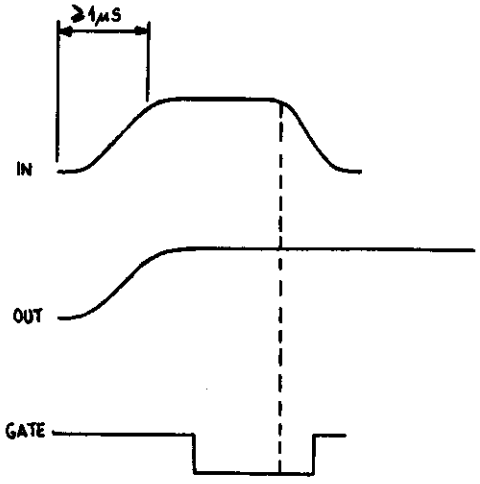
When pulse shaping times are too long, false peak detections may occur due to the gain of the comparator and the noise added to the pulse.



To prevent false peak detections from occuring even with not too long pulse shaping times it is advisable that the gate covers only the peak value.



If rectangular-shaping pulses (flat top) are used, proceed as indicated below.



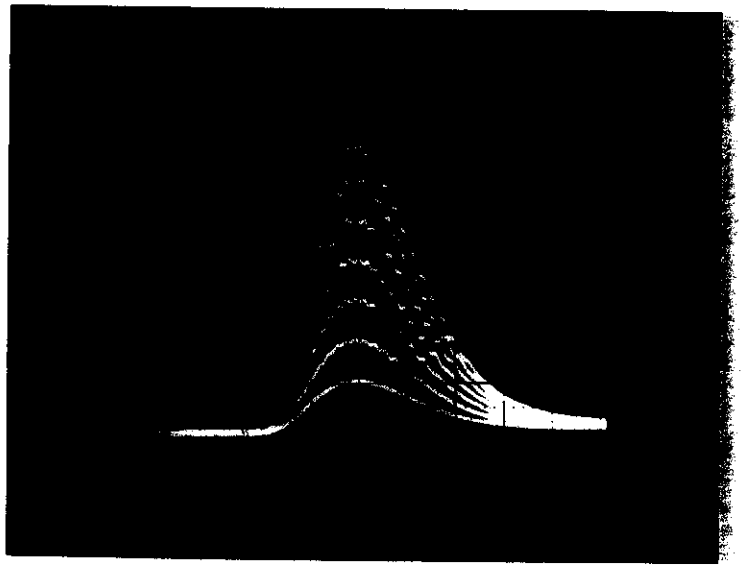
2.4 Analog Input Impedance

In the standard version, the input impedance of the measuring channels is 1KΩ .

If long connecting cables and fast signals (i.e. 0.5 μS semigaussian shaping time) are used, the cable must be terminated with the impedance of the cable itself; otherwise possible oscillations due to the non-terminated cable may result in remarkable differential non-linearities.

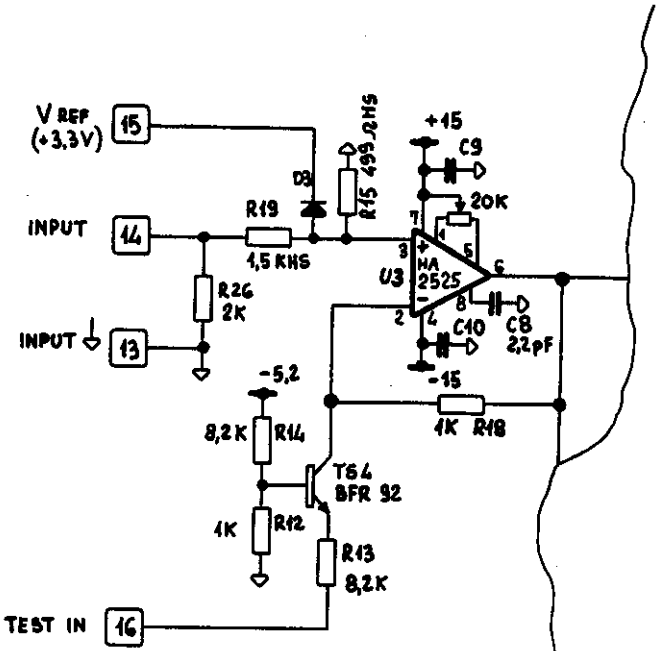
To locate the resistor that determines the input impedence, refer to the electrical diagram of the Input Module (Fig. 2.3) and to the associated component layout (fig. 2.4).

Example of connection with closing impedance differing from the characteristic impedance of the cable used.
The amplitude and frequency of the oscillations change or they disappear depending upon the signal width owing the non-terminated cable which is considered by the shaper-amplifier as a capacity.



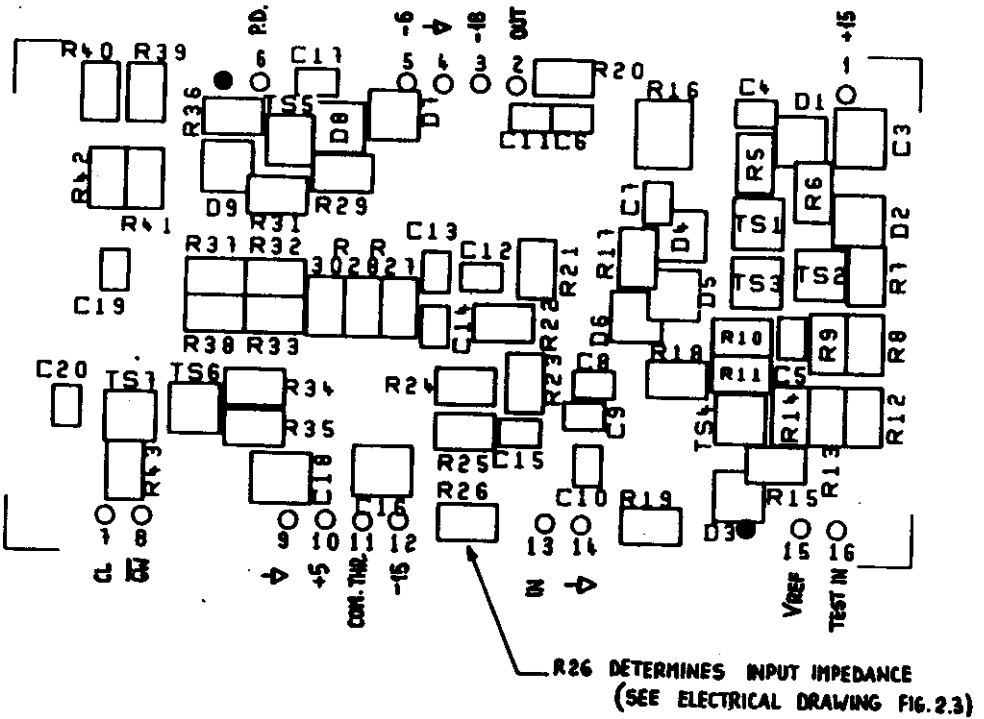
INPUT SIGNAL

SPECTRUM WITH SLIDING PULSE GENERATOR



$$Z_o = \frac{R26 \cdot (R19 + R15)}{R26 + R19 + R15}$$

FIG. 2.3 ANALOG INPUT STAGE - 4418/V



4418/V FIG. 2.4 INPUT MODULE - COMPONENTS LAYOUT