

SIS3800
VME Scaler/Counter

User Manual

SIS GmbH
Moorhof 2d
22399 Hamburg
Germany

Phone: ++49 (0) 40 60 87 305 0
Fax: ++49 (0) 40 60 87 305 20

email: info@struck.de
<http://www.struck.de>

Version: 1.2 as of 29.1.99

Revision Table:

| Revision | Date | Modification |
|----------|----------|--|
| 1.1 | 18.09.98 | Generation |
| 1.2 | 29.01.99 | introduction of revision table LEMO control/flat cable counter front panel included |

1 Table of contents

| | | |
|--------|---|----|
| 1 | Table of contents | 3 |
| 2 | Introduction..... | 5 |
| 3 | Technical Properties/Features | 6 |
| 3.1 | Board Layout..... | 6 |
| 3.2 | Counter Design and Modus Operandi..... | 7 |
| 3.3 | Count Enable Logic..... | 8 |
| 3.4 | Clear Logic..... | 8 |
| 4 | Getting Started..... | 9 |
| 4.1 | Factory Default Settings..... | 9 |
| 4.1.1 | Addressing..... | 9 |
| 4.1.2 | System Reset Behaviour..... | 9 |
| 5 | Firmware Selection | 9 |
| 5.1 | Examples | 10 |
| 6 | Front Panel LEDs | 11 |
| 7 | VME addressing..... | 12 |
| 7.1 | Address Space..... | 12 |
| 7.2 | Base Address..... | 12 |
| 7.2.1 | VME..... | 12 |
| 7.2.2 | VIPA/VME64x..... | 12 |
| 7.3 | Address Map..... | 13 |
| 8 | Register Description | 14 |
| 8.1 | Status Register (0x0)..... | 14 |
| 8.2 | Control Register (0x0)..... | 15 |
| 8.3 | Module Identification and IRQ control register (0x4)..... | 16 |
| 8.4 | Count disable register 0xC | 17 |
| 8.5 | Overflow registers 0x380, 0x3A0, 0x3C0, 0x 3E0..... | 17 |
| 8.6 | Broadcast Addressing..... | 17 |
| 9 | VME Interrupts | 19 |
| 10 | Data Format..... | 20 |
| 10.1 | D16..... | 20 |
| 10.2 | D32..... | 20 |
| 11 | Readout Schemes | 20 |
| 11.1 | Read Shadow Register..... | 20 |
| 11.2 | Read and Clear all Counters | 20 |
| 11.3 | Read Counter..... | 20 |
| 12 | Input Configuration | 21 |
| 12.1 | ECL..... | 21 |
| 12.2 | NIM..... | 22 |
| 12.3 | TTL..... | 23 |
| 12.3.1 | TTL/LEMO..... | 23 |
| 12.3.2 | TTL/Flat Cable | 23 |
| 13 | Connector Specification..... | 23 |
| 14 | Control Input Modes | 24 |
| 14.1 | Version 1 | 24 |
| 14.2 | Version 2 | 24 |
| 15 | Signal Specification..... | 25 |
| 15.1 | Control Signals | 25 |
| 15.2 | Inputs | 25 |
| 16 | Operating Conditions..... | 25 |
| 16.1 | Power Consumption/Voltage requirement..... | 25 |
| 16.2 | Cooling..... | 25 |
| 16.3 | Insertion/Removal..... | 25 |
| 17 | Test..... | 26 |
| 17.1 | LED (selftest)..... | 26 |
| 17.2 | Internal pulser tests | 26 |
| 17.2.1 | Single Pulse..... | 26 |
| 17.2.2 | 25 MHz Pulser..... | 26 |

| | | |
|--------|--|----|
| 17.3 | Reference pulser channel 1 | 26 |
| 17.4 | Signal-Input Priority..... | 26 |
| 18 | Software Support | 27 |
| 18.1 | Contents of the included Floppy | 27 |
| 19 | Appendix..... | 28 |
| 19.1 | Address Modifier Overview..... | 28 |
| 19.2 | Front Panel Layout..... | 29 |
| 19.3 | Flat cable Input/Output Pin Assignments | 30 |
| 19.3.1 | ECL..... | 30 |
| 19.3.2 | TTL..... | 31 |
| 19.4 | List of Jumpers..... | 32 |
| 19.5 | Jumper and rotary switch locations | 32 |
| 19.5.1 | Addressing mode and base address selection | 32 |
| 19.5.2 | J500 (Bootfile Selection) and J520 (SYSRESET Behaviour)..... | 33 |
| 19.6 | Board Layout..... | 34 |
| 19.7 | FLASHROM Versions..... | 35 |
| 19.8 | Row d and z Pin Assignments | 36 |
| 19.9 | Geographical Address Pin Assignments | 37 |
| 19.10 | Additional Information on VME..... | 37 |
| 20 | Index..... | 38 |

2 Introduction

The SIS3800 is one of the classic VME counter/scaler implementations on the base of the SIS360x/38xx printed circuit board. The unit has 32 counter channels and a maximum counting frequency of 200 MHz (ECL and NIM) 100 MHz (TTL) respective. As all boards of the family it is of single slot double Eurocard form factor and available with flat cable connectors for ECL and TTL levels and LEMO connectors for NIM and TTL levels.

The SIS360x/38xx card is a flexible concept to implement a variety of latch and counter firmware designs. The flexibility is based on two to six Xilinx FPGAs in conjunction with a FLASHROM from which the firmware files are loaded into the FPGAs. Depending on the stuffing options of the printed circuit board, the user has the possibility to cover several purposes with the same card, hence the manual is a combination of firmware and hardware description.

All cards of the family are equipped with the 5 row VME64x VME connectors, a side cover and EMC front panel, as well as the VIPA LED set. For users with VME64xP subracks VIPA extractor handles can be installed. The base board is prepared for VIPA style addressing, the current first version of the SIS3800 firmware does not feature VIPA modes yet however.

As we are aware, that no manual is perfect, we appreciate your feedback and will try to incorporate proposed changes and corrections as quickly as possible. The most recent version of this manual can be obtained by email from info@struck.de, the revision dates are online under <http://www.struck.de/manuals.htm>. A list of available firmware designs can be retrieved from <http://www.struck.de/sis3638firm.htm>

3 Technical Properties/Features

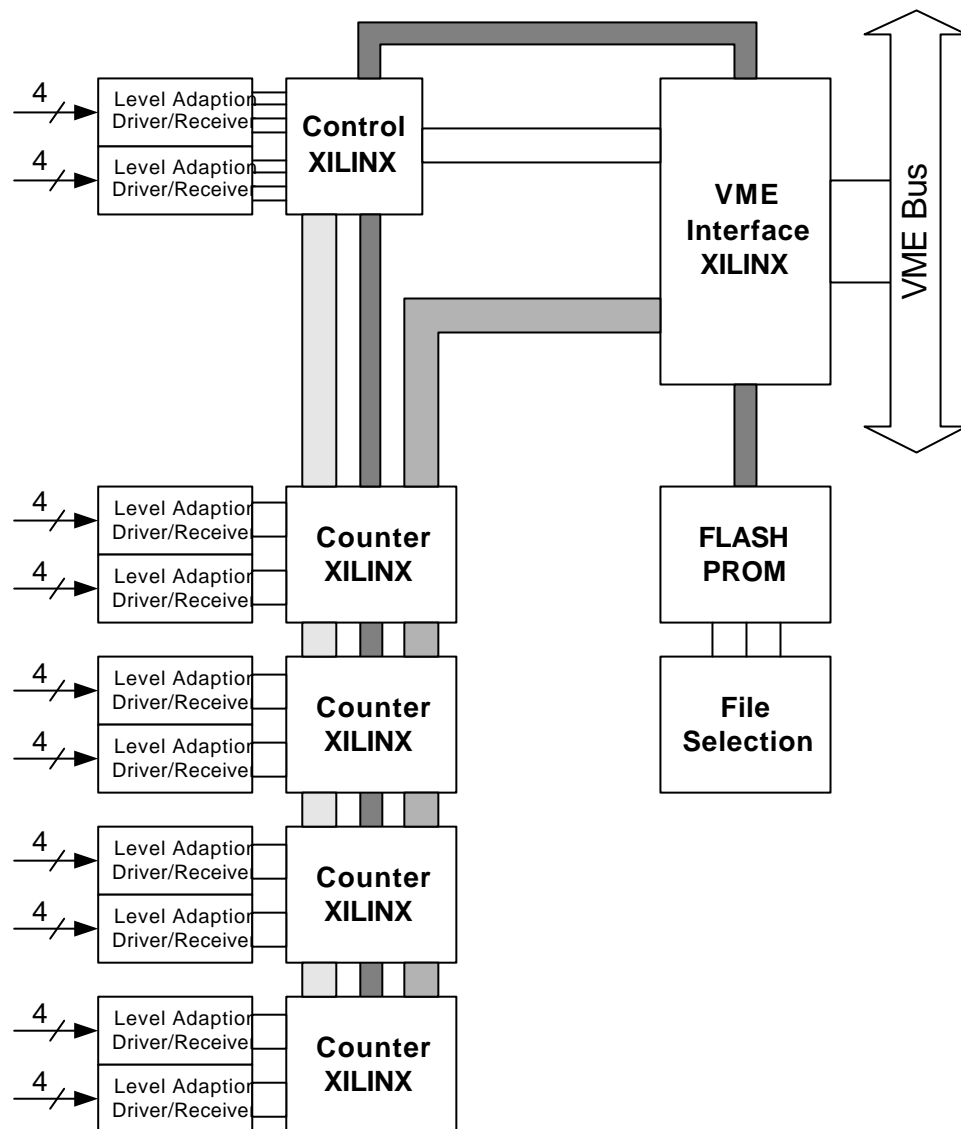
The SIS3800 is rather a firmware design in combination with given board stuffing options, than a name for the board (this is the reason, why the modules are named SIS360x/38xx on the front panel and the distinction of the units is made by the module identifier register). The firmware makes use of part of the possibilities of the SIS360x/38xx PCB, if the SIS3800 or other firmware designs of the family come close to what you need, but something is missing, a custom firmware design may be an option to consider.

Find below a list of key features of the SIS3800.

- 32 channels
- 200 MHz counting rate (ECL and NIM), 100 MHz for TTL
- 32-bit channel depth
- NIM/TTL/ECL versions
- flat cable (TTL/ECL) and LEMO (TTL/NIM) versions
- Shadow register
- Read on the fly
- A16/A24/A32 D16/D32/BLT32 (CBLT32 prepared)
- Base address settable via 5 rotary switches (A32-A12) and one jumper (A11)
- VME interrupt capability
- VIPA geographical addressing prepared
- VIPA LED set
- Reference Pulser Capability
- Up to eight firmware files
- single supply (+5 V)

3.1 Board Layout

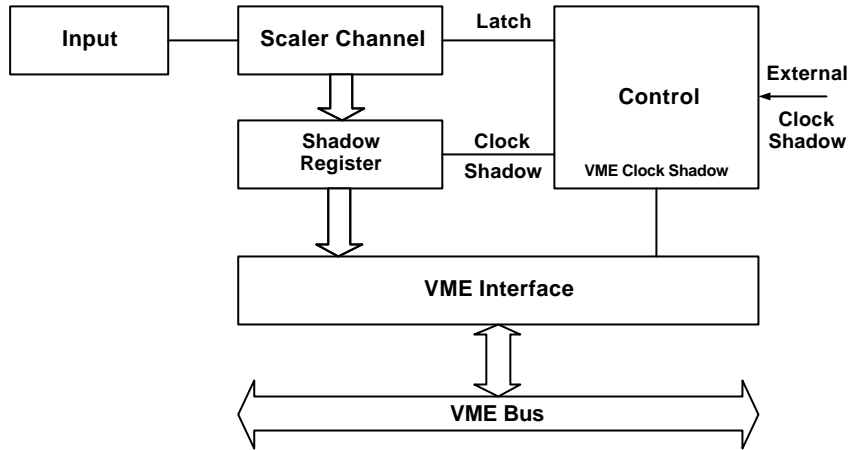
Xilinx FPGAs are the working horses of the SIS360x/38xx board series. The counter (prescaler, latch, ...) logic is implemented in one to four chips, each chip handles eight front end channels. The VME interface and the input and output control logic reside in two Xilinx chips also. The actual firmware is loaded into the FPGAs upon power up from a FLASH PROM under jumper control. The user can select among up to eight different boot files by the means of a 3-bit jumper array. The counter and control inputs can be factory configured for ECL, NIM and TTL levels, on the control outputs the same levels are the available as options. The standard SIS3800 version 1 design has no outputs implemented. The front panel is available as flat cable (ECL and TTL) or LEMO (NIM and TTL) version. The board layout is illustrated with the block diagram below:



SIS3800 Block Diagram

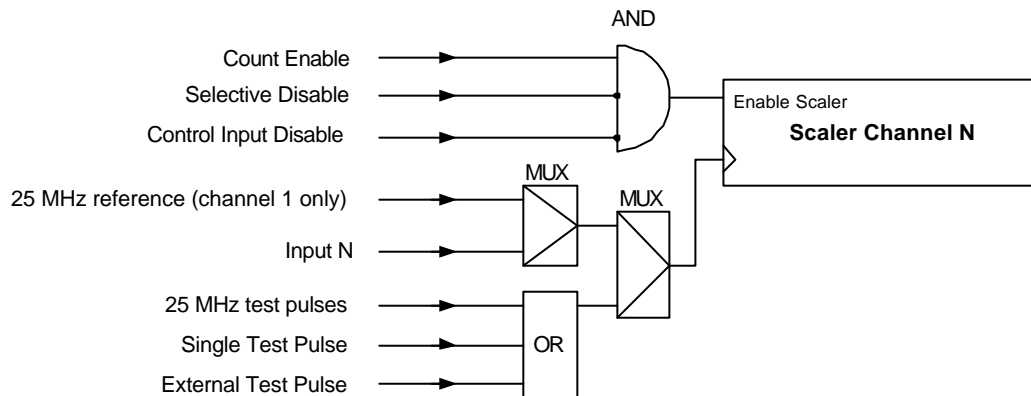
3.2 Counter Design and Modus Operandi

The counters are implemented in XILINX FPGAs. One of the counter FPGAs holds 8 32-bit deep counter channels. The actual scaler contents are passed to the VME bus via a shadow register. The scaler data have to be copied into the shadow register before readout via a software command or a front panel hardware pulse. This can take place in parallel to the acquisition of counts, what is called read on the fly. On a read on the fly the status of the lowest 6 bits may be not accurate, i.e. the counter readout value is accurate modulo 64. (read on the fly readout accuracy down to one count can be achieved with the SIS3801 multiscaler). No pulses are missed during a read on the fly, i.e. the frontend continues counting. A diagram of the setup is shown in the figure below. The different readout schemes are addressed in the key register section.



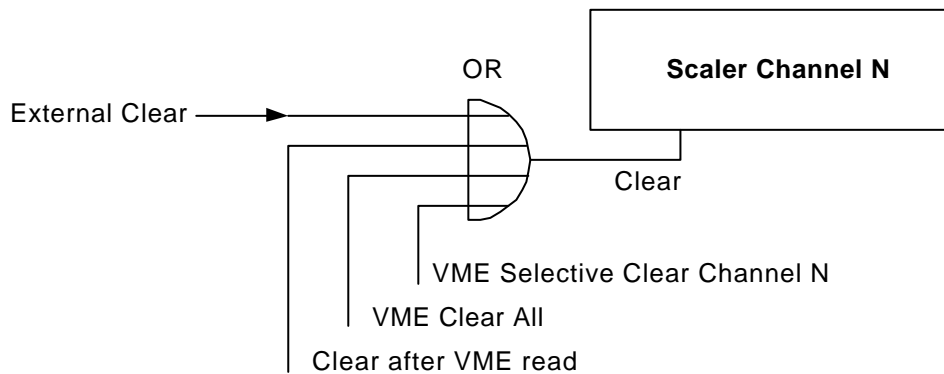
3.3 Count Enable Logic

A channel acquires input or test counts, if the selective count enable and the global count enable conditions are true. Via the test enable toggle bits in the control register the input of the counter is switched to test pulses or front panel signals.



3.4 Clear Logic

The contents of the counters can be cleared via VME access or a front panel pulse. The four possible clear sources are ored as shown in the diagram below.



4 Getting Started

The minimum setup to operate the SIS3800 requires the following steps:

- Check the proper firmware design is selected (should be design zero, i.e. all jumpers of jumper array J500 set).
- Select the VME base address for the desired addressing mode
- Select the VME SYSRESET behaviour via J520
- turn the VME crate power off
- install the scaler in the VME crate
- connect your signals to the counter
- turn crate power back on
- set global count enable via key address 0x28
- read all counters with clock shadow register via block transfer from start address 0x280 (read) or 0x300 (read and clear) or subsequent single word reads.

A good way of checking first time communication with the SIS3800 consists of switching on the user LED by a write to the control register at offset address 0x0 with data word 0x1 (the LED can be switched back off by writing 0x1000 to the control register)..

4.1 Factory Default Settings

4.1.1 Addressing

SIS3800 boards are shipped with the En_A32, the En_A24 and the En_A16 jumpers installed and the rotary switches set to:

| Switch | SW_A32U | SW_A32L | SW_A24U | SW_A24L | SW_A16 | J A_11 | Bits 7-4 | Bits 3-0 |
|---------|---------|---------|---------|---------|--------|--------|----------|----------|
| Setting | 3 | 8 | 3 | 8 | 3 | 8 | 0 | 0 |

Jumper A_11 is open (bit 11 set).

Hence the unit will respond to the following base addresses:

| Mode | Base address |
|------|--------------|
| A32 | 0x38383800 |
| A24 | 0x383800 |
| A16 | 0x3800 |

Firmware Design

Design 1 of the FLASH PROM is selected (lowest jumper of jumper array J500 open, the others set).

4.1.2 System Reset Behaviour

J520 is set, i.e. the SIS3800 is reset upon VME reset.

5 Firmware Selection

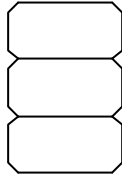
The FLASH PROM of a SIS360x/38xx board can contain several boot files. A list of available FLASH PROM versions can be found on our web site <http://www.struck.de> in the manuals page. If your FLASH PROM has more than one firmware design, you can select the

desired firmware via the firmware selection jumper array J500 . You have to make sure, that the input/output configuration and FIFO configuration of your board are in compliance with the requirements of the selected firmware design (a base board without FIFO can not be operated as multi channel scaler e.g.). A total of 8 boot files from the FLASHROM can be selected via the three bits of the jumper array. The array is located towards the rear of the card between the VME P1 and P2 connectors. The lowest bit sits towards the bottom of the card, a closed jumper represents a zero, an open jumper a one.

5.1 Examples

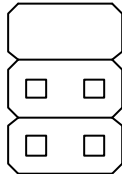
The figures below show jumper array 500 with the soldering side of the board facing the user and the VME connectors pointing to the right hand side.

Bootfile 0 selected



With all jumpers closed boot file 0 is selected

Bootfile 3 selected



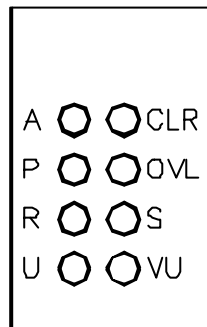
With the lowest two jumpers open bit 0 and bit 1 are set to 1 and hence boot file 3 is selected

6 Front Panel LEDs

The SIS3800 has 8 front panel LEDs to visualise part of the units status. Three LEDs according to the VME64xP standard (Power, Access and Ready) plus 5 additional LEDs (VME user LED, Clear, Overflow, Scaler enable and VIPA user LED).

| Designation | LED | Color | Function |
|-------------|---------------|--------|--|
| A | Access | yellow | Signals VME access to the unit |
| P | Power | red | Flags presence of VME power |
| R | Ready | green | Signals configured logic |
| U | VME user LED | green | To be switched on/off under user program control |
| CLR | Clear | yellow | Signals soft or hardware clear |
| OVL | Overflow | red | Signals Overflow in one or more channels |
| S | Scaler Enable | green | Signals one or more enabled channels |
| VU | VIPA user LED | green | for future use |

The LED locations are shown in the portion of the front panel drawing below.



The VME Access, the Clear and the Scaler enable LED are monostable (i.e. the duration of the on phase is stretched for better visibility), the other LEDs reflect the current status. An LED test cycle is performed upon power up (refer to the chapter 17.1).

7 VME addressing

7.1 Address Space

As bit 11 is the lowest settable bit on the 360x/38xx board, an address space of 2 Kbytes (Offset plus 0x000 to 0x7ff) is occupied by the module.

7.2 Base Address

7.2.1 VME

The VME addressing mode (A16/A24/A32) is selected via the jumpers EN_A16, EN_A24 and EN_A32. The mode is selected by closing the corresponding jumper, it is possible to enable two or all three addressing modes simultaneously.

The base address is set via the five rotary switches SW_A32U, SW_A32L, SW_A24U, SW_A24L and SW_A16 and the jumper J_A11. The table below lists the switches and jumpers and their corresponding address bits.

| Switch/Jumper | Affected Bits |
|---------------|---------------|
| SW_A32U | 31-28 |
| SW_A32L | 27-24 |
| SW_A24U | 23-20 |
| SW_A24L | 19-16 |
| SW_A16 | 15-12 |
| J_A11 | 11 |

In the table below you can see, which jumpers and switches are used for address decoding in the three different addressing modes (fields marked with an x are used).

| | SW_A32U | SW_A32L | SW_A24U | SW_A24L | SW_A16 | J_A11 |
|-----|---------|---------|---------|---------|--------|-------|
| A32 | x | x | x | x | x | x |
| A24 | | | x | x | x | x |
| A16 | | | | | x | x |

Note: J_A11 closed represents a 0, J_A11 open a one

7.2.2 VIPA/VME64x

As the VME64x and the VME64xP (VIPA) standard are not yet standards to refer to and to declare conformity with, addressing modes (like geographical addressing e.g.) according to these standards are prepared but not yet implemented in the current firmware revisions.

7.3 Address Map

The SIS360x/38xx boards are operated via VME registers, VME key addresses and the FIFO (where installed). The following table gives an overview on all SIS3800 addresses and their offset from the base address, a closer description of the registers and their function is given in the following subsections.

| Offset | Key | Access | Type | Function |
|-----------------|-----|--------|-------------------|---|
| 0x000 | | R/W | D16/D32 | Control and Status register |
| 0x004 | | R/W | D16/D32 | Module Identification and IRQ control register |
| 0x00C | | W | D16/D32 | Selective count disable register |
| 0x020 | KA | W | D16/D32 | clear all counters and overflow bits |
| 0x024 | KA | W | D16/D32 | clock shadow register |
| 0x028 | KA | W | D16/D32 | global count enable |
| 0x02C | KA | W | D16/D32 | global count disable |
| 0x030 | KA | W | D16/D32 | Broadcast; clear all counters and overflow bits |
| 0x034 | KA | W | D16/D32 | Broadcast; clock shadow register |
| 0x038 | KA | W | D16/D32 | Broadcast; global count enable |
| 0x03C | KA | W | D16/D32 | Broadcast; global count disable |
| 0x040 | KA | W | D16/D32 | clear counter group and overflow channel 1-8 |
| 0x044 | KA | W | D16/D32 | clear counter group and overflow channel 9-16 |
| 0x048 | KA | W | D16/D32 | clear counter group and overflow channel 17-24 |
| 0x04C | KA | W | D16/D32 | clear counter group and overflow channel 25-32 |
| 0x050 | KA | W | D16/D32 | enable reference pulser channel 1 |
| 0x054 | KA | W | D16/D32 | disable reference pulser channel 1 |
| 0x060 | KA | W | D16/D32 | reset register (global reset) |
| 0x068 | KA | W | D16/D32 | Test pulse (generate a single pulse) |
| 0x100- 0x17C | KA | W | D16/D32 | clear counter N and its overflow bit |
| 0x180- 0x1FC | KA | W | D16/D32 | clear overflow bit of counter N |
| 0x200- 0x27C | | R | D16/D32/ BLT32 | read shadow register (does not initiate clock shadow) |
| 0x280- 0x2FC | | R | D16/D32/ BLT32 | read counter (initiates clock shadow also) |
| 0x300- 0x37C | | R | D16/D32/ BLT32 | read and clear all counters |
| 0x380 | | R | D16/D32 | Overflow register channel 1-8 |
| 0x3A0 | | R | D16/D32 | Overflow register channel 9-16 |
| 0x3C0 | | R | D16/D32 | Overflow register channel 17-24 |
| 0x3E0 | | R | D16/D32 | Overflow register channel 25-32 |

Note: D08 is not supported by the SIS38xx boards

8 Register Description

8.1 Status Register (0x0)

The status register reflects the current settings of most of the SIS3800 parameters in read access, in write access it functions as the control register.

| Bit | Function |
|-----|--|
| 31 | 0 |
| 30 | Status VME IRQ source 2 (test IRQ) |
| 29 | Status VME IRQ source 1 (ext. clock shadow) |
| 28 | Status VME IRQ source 0 (Overflow) |
| 27 | VME IRQ |
| 26 | internal VME IRQ |
| 25 | 0 |
| 24 | 0 |
| 23 | 0 |
| 22 | Status VME IRQ Enable Bit Source 2 |
| 21 | Status VME IRQ Enable Bit Source 1 |
| 20 | Status VME IRQ Enable Bit Source 0 |
| 19 | 0 |
| 18 | 0 |
| 17 | 0 |
| 16 | reserved (read back as 0 at power up) |
| 15 | Global Count Enable |
| 14 | General Overflow Bit |
| 13 | Status enable reference pulser channel 1 |
| 12 | 0 |
| 11 | 0 |
| 10 | 0 |
| 9 | 0 |
| 8 | 0 |
| 7 | Status broadcast mode handshake controller |
| 6 | Status broadcast mode |
| 5 | Status input test mode |
| 4 | Status 25 MHz test pulses |
| 3 | Status input mode bit 1 |
| 2 | Status input mode bit 0 |
| 1 | Status IRQ source 2 for software IRQ testing |
| 0 | Status user LED |

The reading of the status register after power up or key reset is 0x0 (see default settings of control register).

8.2 Control Register (0x0)

The control register is in charge of the control of most of the basic properties of the SIS3800 board in write access. It is implemented via a selective J/K register, a specific function is enabled by writing a 1 into the set/enable bit, the function is disabled by writing a 1 into the clear/disable bit (which has a different location within the register). An undefined toggle status will result from setting both the enable and disable bits for a specific function at the same time.

On read access the same register represents the status register.

| Bit | Function |
|-----|---|
| 31 | reserved |
| 30 | disable IRQ source 2 (*) |
| 29 | disable IRQ source 1 (*) |
| 28 | disable IRQ source 0 (*) |
| 27 | reserved |
| 26 | reserved |
| 25 | reserved |
| 24 | clear reserved bit |
| 23 | reserved |
| 22 | enable IRQ source 2 |
| 21 | enable IRQ source 1 |
| 20 | enable IRQ source 0 |
| 19 | reserved |
| 18 | reserved |
| 17 | reserved |
| 16 | set reserved bit |
| 15 | disable broadcast mode handshale controller (*) |
| 14 | disable broadcast mode (*) |
| 13 | disable input test mode (*) |
| 12 | disable 25 MHz test pulses (*) |
| 11 | clear input mode bit 1 (*) |
| 10 | clear input mode bit 0 (*) |
| 9 | clear IRQ test source 2 |
| 8 | switch off user LED (*) |
| 7 | enable handshake controller for broadcast mode |
| 6 | enable broadcast mode |
| 5 | enable input test mode |
| 4 | enable 25 MHz test pulses |
| 3 | set input mode bit 1 |
| 2 | set input mode bit 0 |
| 1 | set IRQ test (source 2) |
| 0 | switch on user LED |

(*) denotes the default power up or key reset state

8.3 Module Identification and IRQ control register (0x4)

This register has two basic functions. The first is to give information on the active firmware design. This function is implemented via the read only upper 20 bits of the register. Bits 16-31 hold the four digits of the SIS module number (like 3800 or 3600 e.g.), bits 12-15 hold the version number. The version number allows a distinction between different implementations of the same module number, the SIS3801 for example has the 24-bit mode with user bits and the straight 32-bit mode as versions.

| Bit | Read/Write access | Function |
|-----|-------------------|---|
| 31 | read only | Module Identification Bit 15 |
| 30 | read only | Module Identification Bit 14 |
| 29 | read only | Module Identification Bit 13 |
| 28 | read only | Module Identification Bit 12 |
| 27 | Read only | Module Identification Bit 11 |
| 26 | read only | Module Identification Bit 10 |
| 25 | read only | Module Identification Bit 9 |
| 24 | read only | Module Identification Bit 8 |
| 23 | read only | Module Identification Bit 7 |
| 22 | read only | Module Identification Bit 6 |
| 21 | read only | Module Identification Bit 5 |
| 20 | read only | Module Identification Bit 4 |
| 19 | read only | Module Identification Bit 3 |
| 18 | read only | Module Identification Bit 2 |
| 17 | read only | Module Identification Bit 1 |
| 16 | read only | Module Identification Bit 0 |
| 15 | read only | Version Bit 3 |
| 14 | read only | Version Bit 2 |
| 13 | read only | Version Bit 1 |
| 12 | read only | Version Bit 0 |
| 11 | read/write | VME IRQ Enable (0=IRQ disabled, 1=IRQ enabled) |
| 10 | read/write | VME IRQ Level Bit 2 |
| 9 | read/write | VME IRQ Level Bit 1 |
| 8 | read/write | VME IRQ Level Bit 0 |
| 7 | read/write | IRQ Vector Bit 7; placed on D7 during VME IRQ ACK cycle |
| 6 | read/write | IRQ Vector Bit 6; placed on D6 during VME IRQ ACK cycle |
| 5 | read/write | IRQ Vector Bit 5; placed on D5 during VME IRQ ACK cycle |
| 4 | read/write | IRQ Vector Bit 4; placed on D4 during VME IRQ ACK cycle |
| 3 | read/write | IRQ Vector Bit 3; placed on D3 during VME IRQ ACK cycle |
| 2 | read/write | IRQ Vector Bit 2; placed on D2 during VME IRQ ACK cycle |
| 1 | read/write | IRQ Vector Bit 1; placed on D1 during VME IRQ ACK cycle |
| 0 | read/write | IRQ Vector Bit 0; placed on D0 during VME IRQ ACK cycle |

The second function of the register is interrupt control. The interrupter type of the SIS3800 is D08(O). Via bits 0-7 of the module identifier and interrupt control register you can define the interrupt vector, which is placed on the VME bus during the interrupt acknowledge cycle. Bits 8 through 10 define the VME interrupt level, bit 11 is used to enable (bit set to 1) or disable (bit set to 0) interrupting.

Module identification and version example:

The register for a SIS3801 in straight 32-bit mode (version 1) reads 0x38011nnn, for a SIS3801 in 24-bit mode (version 2) it reads 0x38012nnn. (the status of the lower 3 nibbles is denoted with n in the example).

8.4 Count disable register 0xC

The count disable register can be used to disable single channels or arbitrary groups of channels. Note, that both the external (if used) and the internal conditions have to be in status enable for the given channel.

The register is write only.

If bit N of the register is set, channel N+1 is disabled.

Example: If 0x5 is written to the count disable register, counting of channel 1 and 3 is disabled.

8.5 Overflow registers 0x380, 0x3A0, 0x3C0, 0x3E0

Each overflow register holds the overflow bit of eight counter channels (i.e. of one counter XILINX) in its lowest eight bits.

Example: register 0x380 holds the overflow bits of channels 1-8 as shown in the table below.

| | | | | | | | | | |
|-----|------|------|------|------|------|------|------|------|-----------|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | Bits 23-1 |
| | Ch 8 | Ch 7 | Ch 6 | Ch 5 | Ch 4 | Ch 3 | Ch 2 | Ch 1 | undefined |

8.6 Broadcast Addressing

Broadcast addressing is an efficient way to issue the same command to a number of modules. It can be used in A24 and A32 mode on SIS360x/38xx boards. The higher address bits are used to define the broadcast class, the distinction of the modules is done via the A16 rotary switch and the A_11 jumper. If broadcast addressing is used, the A32_U, the A_32_L, the A24_U and the A24_L rotary switches must have the same setting in A32 mode, in A24 mode the A24_U and A24_L setting must be the same on all participating units. One of the participating units must be configured as broadcast handshake controller by setting bit 7 in the units control register. All of the participating units must have set bit 6 (enable broadcast) in the control register. The broadcast time jitter was measured to be less than 40 ns within a VME crate, i.e. you have the possibility issue commands under software control with a maximum uncertainty of 40 ns (like clear all counters), what sure is worse, than a hard wired front panel clear, but is much better than a VME single cycle loop over a number of units. The four broadcast commands are executed via the VME key addresses at offset 0x030 through 0x3C.

A32 Broadcast Example:

Let four SIS3800 participate by setting the A_32 jumper and setting the base address of the units to:

```
Unit 1: 0x32001000
Unit 2: 0x32001800
Unit 3: 0x32002000
Unit 4: 0x32002800
```

Switch on enable broadcast by setting bit 6 in the control register of the four units.

Enable broadcast handshake controller on unit 4 by setting bit 7 of its control register.

An A232 write to address 0x32000034 will clock the shadow register on units 1 through 4.

A24 Broadcast Example:

Let three SIS3800 participate by setting the A_24 jumper and setting the base address of the units to:

```
Unit 1: 0x541000
Unit 2: 0x542000
Unit 3: 0x543000
```

Switch on enable broadcast by setting bit 6 in the control register of the three units.

Enable broadcast handshake controller on unit 1 by setting bit 7 of its control register.

An A24 write to address 0x540030 will clear the counters on units 1 through 3.

9 VME Interrupts

Three VME interrupt sources are implemented in the SIS3800 firmware design:

- Overflow
- External Latch Shadow Input
- Test Interrupt

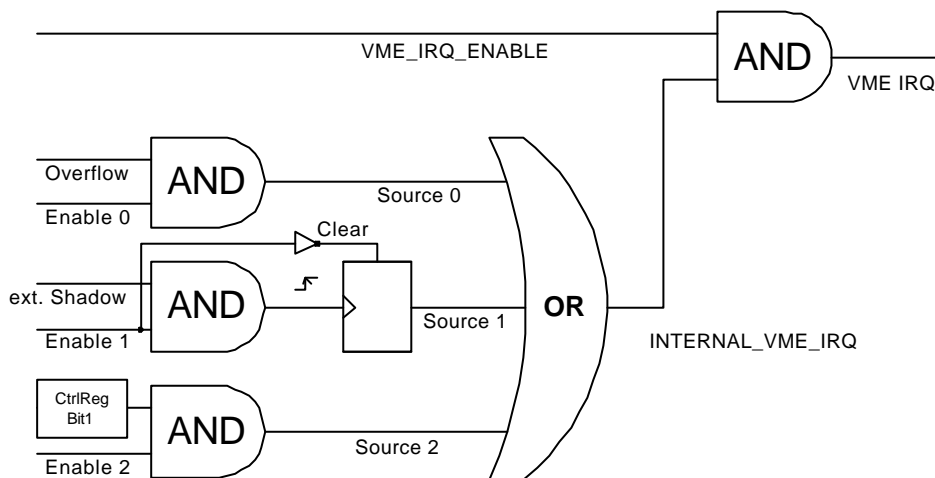
The interrupter is of type D8(O).

The interrupt logic is shown below. For VME interrupt generation the corresponding interrupt source has to be enabled by setting the respective bit in the VME control register (disabling is done with the sources J/K bit). Interrupt generation has to be enabled by setting bit 11 in the IRQ and version register. The internal VME interrupt flag can be used to check on an IRQ condition without actually making use of interrupts on the bus.

The VME interrupt level (1-7) are defined by bits 8 through 10 and the VME interrupt vector (0-255) by bits 0 through 7 of the VME IRQ and version register.

In general an interrupt condition is cleared by disabling the corresponding interrupt, clearing the interrupt condition (i.e. clear overflow) and enabling the IRQ again.

Note: In most cases your experiment may not require interrupt driven scaler readout, but the interrupt capability of the SIS3800 provides a way to overcome the problem of missing front panel inputs on most commercial VME CPUs.



10 Data Format

The data format of the actual counter values (read via the shadow register) for D16 and D32 reads is shown in the two tables below.

10.1 D16

| | high Byte | low Byte |
|-------------|-----------------|-----------------|
| first read | Data Bits 31-24 | Data Bits 23-16 |
| second read | Data Bits 15-8 | Data Bits 7-0 |

10.2 D32

| Data Bits 31-24 | Data Bits 23-16 | Data Bits 15-8 | Data Bits 7-0 |
|-----------------|-----------------|----------------|---------------|
| | | | |

11 Readout Schemes

Scaler data can be read from different locations. The read location has an impact on the counter behaviour.

11.1 Read Shadow Register

In a single cycle or block transfer read from the shadow register (0x200-0x27C) the data from the last transfer to the shadow register are obtained. No automatic clock shadow is initiated, i.e. if the user wants to read the actual scaler values he has to ensure a soft- or hardware clock shadow before the read.

11.2 Read and Clear all Counters

In a single cycle or block read from the read and clear all counter registers (0x300-0x37C) the data are transferred into the shadow register, all counters are cleared after the transfer and the shadow data are read.

Note: If your CPU does not support block transfer you can ensure synchronicity to 5 ns by reading the first scaler value from 0x300 and the rest from the shadow registers 0x204-0x27C.

11.3 Read Counter

The read counter behaves like the read and clear all counters except that the counter values are not cleared after the copy to the shadow register.

12 Input Configuration

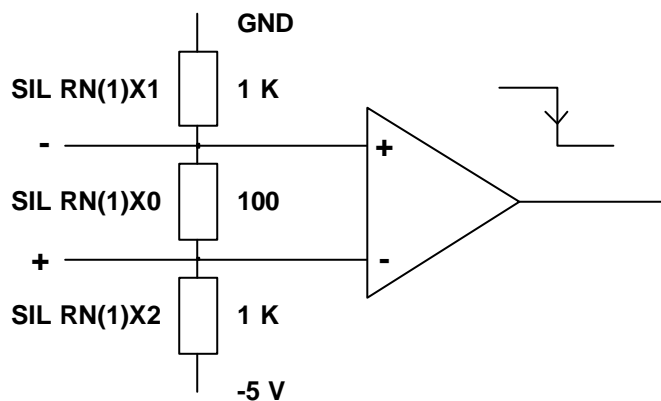
SIS36/38xx boards are available for NIM, TTL and ECL input levels and in LEMO and flat cable versions. The boards are factory configured for the specified input level and connector type, input termination is installed.

12.1 ECL

The 100 Ω input termination can be removed in groups of four channels by removing the corresponding resistor networks. The termination of single control inputs can be disabled with jumpers J101 through J108, an open jumper disables the termination of the corresponding channel.

| Network | Channels | 1 K Networks |
|---------|-------------|--------------|
| RN10 | 1-4 | RN11/12 |
| RN20 | 5-8 | RN21/22 |
| RN30 | 9-12 | RN31/32 |
| RN40 | 13-16 | RN41/41 |
| RN50 | 17-20 | RN51/52 |
| RN60 | 21-24 | RN61/62 |
| RN70 | 25-28 | RN71/72 |
| RN80 | 29-32 | RN81/82 |
| RN110 | Control 1-4 | RN111/RN112 |
| RN120 | Control 5-8 | RN121/RN122 |

The schematics of the ECL input circuitry is shown below.

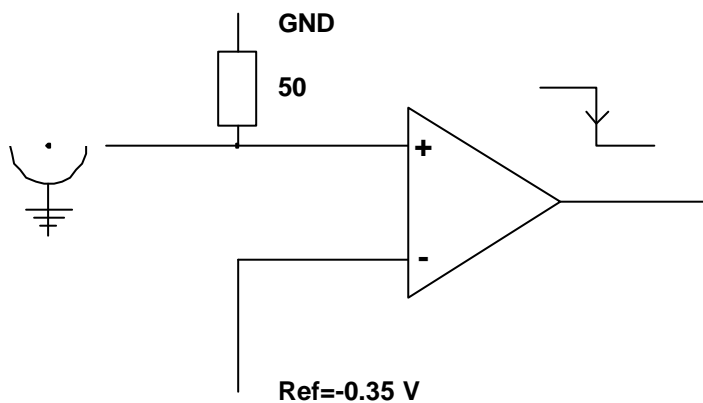


12.2 NIM

The 50 Ω input termination can be removed in groups of four channels by removing the corresponding resistor networks. The termination of single control inputs can be disabled with jumpers J101 through J108, an open jumper disables the termination of the corresponding channel.

| Network | Channels |
|----------------------------|-------------|
| U15 (Pins <u>10</u> to 6) | 1-4 |
| U15 (Pins <u>1</u> to 5) | 5-8 |
| U35 (Pins <u>10</u> to 6) | 9-12 |
| U35 (Pins <u>1</u> to 5) | 13-16 |
| U55 (Pins <u>10</u> to 6) | 17-20 |
| U55 (Pins <u>1</u> to 5) | 21-24 |
| U75 (Pins <u>10</u> to 6) | 25-28 |
| U75 (Pins <u>1</u> to 5) | 29-32 |
| U115 (Pins <u>10</u> to 6) | Control 1-4 |
| U115 (Pins <u>1</u> to 5) | Control 5-8 |

The schematics of the NIM input circuitry is shown below.



14 Control Input Modes

The assignment of the control inputs can be controlled via the input mode bits in the control register. While the standard SIS3800 firmware design (design 3800 version 1) has inputs only, design 3800 version 2 is compatible with board, where control lines 5 to 8 are configured as outputs (what is the case for SIS3801 multiscaler boards).

14.1 Version 1

Control Input Modes

| | |
|--------------------------|--|
| Mode 0 (bit1=0, bit0=0): | all control inputs are disabled |
| Mode 1 (bit1=0, bit0=1): | input 1 -> disable count all channels input 2 -> clear all channels input 5 -> external clock shadow register input 7 -> external test pulse (max 50 MHz) |
| Mode 2 (bit1=1, bit0=0): | input 1 -> disable count channels 1-16 input 3 -> disable count channels 17-32 input 2 -> clear channel 1-16 input 4 -> clear channel 17-32 input 5 -> external clock shadow register input 7 -> external test pulse (max. 50 MHz) |
| Mode 3 (bit1=1, bit0=1): | input 1 -> disable count channels 1-8 input 3 -> disable count channels 9-16 input 5 -> disable count channels 17-24 input 7 -> disable count channels 25-32 input 2 -> clear channels 1-8 input 4 -> clear channels 9-16 input 6 -> clear channels 17-24 input 8 -> clear channels 25-32 |

14.2 Version 2

Control Input Modes

| | |
|--------------------------|--|
| Mode 0 (bit1=0, bit0=0): | all control inputs are disabled |
| Mode 1 (bit1=0, bit0=1): | input 1 -> disable count all channels input 2 -> clear all channels input 3 -> external clock shadow register input 4 -> external test pulse (max 50 MHz) |
| Mode 2 (bit1=1, bit0=0): | all control inputs are disabled |
| Mode 3 (bit1=1, bit0=1): | all control inputs are disabled |

15 Signal Specification

15.1 Control Signals

The width of the clear and external latch shadow pulse has to be greater or equal 10 ns, an external inhibit has to be present for the period you desire to disable counting. An internal delay of some 15 ns has to be taken into account for all external signals.

15.2 Inputs

The SIS3800 is specified for counting rates of 200 MHz for ECL and NIM signals and 100 MHz for the TTL case. Thus the minimum high and low level duration is 2.5 ns (5 ns respective). Signal deterioration over long cables has to be taken into account.

16 Operating Conditions

16.1 Power Consumption/Voltage requirement

Although the SIS3800 is prepared for a number of VIPA features, it was decided to use an on board DC/DC converter to generate the -5 V, which are needed for driver and receiver chips, to allow for the use of the module in all 6U VME environments. The power consumption is counting rate dependent, it varies from the idle value of $+5$ V 3,3 A to $+5$ V 4,5 A with all channels counting at 200 MHz (i.e. the power consumption is < 23 W).

16.2 Cooling

Forced air flow is required for the operation of the SIS3800 board.

16.3 Insertion/Removal

Please note, that the VME standard does not support live insertion (hot swap). Hence crate power has to be turned off for installation and removal of SIS3800 scalers.

The leading pins on the SIS3800 VME64x VME connectors and connected on board circuitry are designed for hot swap in conjunction with a VME64x backplane (a VME64x backplane can be recognised by the 5 row VME connectors, while the standard VME backplane has three row connectors only).

17 Test

The SIS380x scaler series provides the user with a number of test features, which allow for debugging of the unit as well as for overall system setups.

17.1 LED (*selftest*)

During power up self test and LCA configuration all LEDs except the Ready (R) LED are on. After the initialisation phase is completed, all LEDs except the Ready (R) LED and the Power (P) have to go off. Differing behaviour indicates either a problem with the download of the firmware boot file or one or more LCA and/or the download logic.

17.2 Internal pulser tests

17.2.1 Single Pulse

A single pulse into all channels can be generated with a write to the key address 0x68 if test mode is enabled via the control register. In conjunction with the count enable register more complex count patterns, like increment patterns e.g., can be generated before readout.

17.2.2 25 MHz Pulser

Simultaneous pulsing at 25 MHz into all channels can be used to test the complete readout chain and internal counter logic of the SIS3800. The feature is activated by enabling input test mode and 25 MHz test pulses via the corresponding bits in the control register.

The 25 MHz test pulser gives easy access to your VME CPUs readout timing. By making subsequent reads to the same counter and multiplying the difference in counts with 40 ns you can measure the single word access time.

17.3 Reference pulser channel 1

The reference pulser for channel 1 can be seen rather as a monitoring feature than a test feature. It sets the counting rate of channel 1 to 25 MHz (note, that a simultaneous front panel signal on channel 1 is ignored).

17.4 Signal-Input Priority

If the user happens to enable more than one input option (enable test mode, enable reference pulser, scaler enable) at the same time, the priority is as show in the table below:

| Priority | Feature |
|----------|-----------------------------------|
| 1 | Test mode |
| 2 | Reference Pulser (channel 1 only) |
| 3 | Front Panel Inputs |

Example: If test mode and reference pulser are enabled at the same time, channel one will count test pulses (i.e. will count synchronous with the test pulser).

18 Software Support

VME multiscaler boards are tested at SIS with an OR VP6 VME CPU (Pentium II based) under Windows 95 and a National Instruments CVI user interface. The actual VME C code makes use of the OR Windows 95 DLL, which has straightforward to read and understand routines like:

```
VMEA24StdWriteWord(a32address + KEY_RESET, 0x0); /* Key Reset */  
rdata = VMEA24StdReadWord(a32address + STAT_REG);
```

In most cases the user setup will be using different hardware, a full fledged real time operating system like VxWorks, and a different user interface. We still believe, that it is helpful to have a look at the code which is used to test the units and to take it as an example for the implementation of the actual scaler readout application. A floppy with our test software is enclosed with SIS3800 shipments.

Depending on the user feedback and co-operation we expect, that we will have drivers or at least example routines for the commonly used VME CPU operating systems at hand in the mid term.

18.1 Contents of the included Floppy

The Floppy contains a readme.txt file with the most up to date information, the CVI project file and all home made files from the project. The important part of the code for the implementation of your own program is sitting in the CVI call back routines.

19 Appendix

19.1 Address Modifier Overview

Find below the table of address modifiers, which can be used with the SIS360x/38xx (with the corresponding addressing mode enabled).

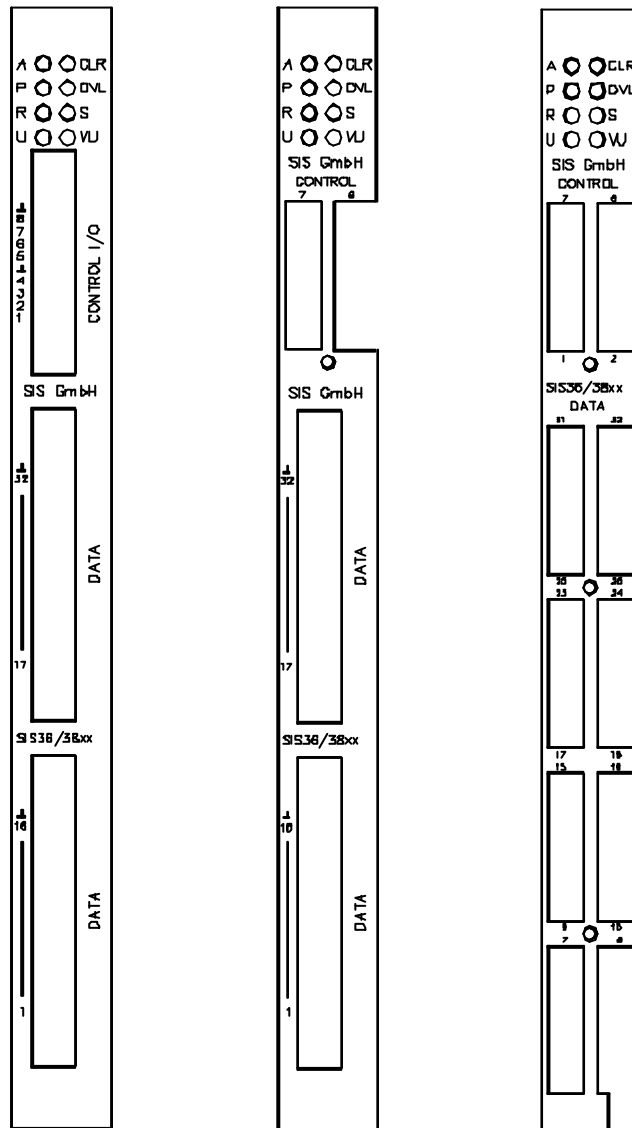
| AM code | Mode |
|---------|---|
| 0x3F | A24 supervisory block transfer (BLT) |
| 0x3D | A24 supervisory data access |
| 0x3B | A24 non-privileged block transfer (BLT) |
| 0x39 | A24 non-privileged data access |
| 0x2D | A16 supervisory access |
| 0x29 | A16 non-privileged access |
| 0x0F | A32 supervisory block transfer (BLT) |
| 0x0D | A32 supervisory data access |
| 0x0B | A32 non-privileged block transfer (BLT) |
| 0x09 | A32 non privileged data access |
| | Future option: CBLT |

19.2 Front Panel Layout

The front panel of the SIS3800 is equipped with 8 LEDs, 8 control in- and outputs and 32 counter inputs. On flat cable units (ECL and TTL) the control connector is a 20 pin header flat cable connector and the channel inputs are fed via two 34-pin headers. On LEMO (NIM and TTL) units the control in- and outputs are grouped to one 8 channel block and the counter inputs are grouped into 2 blocks of 16 channels. A mixed LEMO control/flat cable counter input version is available also. The units are 4 TE (one VME slot) wide, the front panel is of EMC shielding type. VIPA extractor handles are available on request or can be retrofitted by the user, if he wants to change to a VIPA crate at a later point in time.

In the drawing below you can find the flat cable (left hand side), the LEMO control/flat cable input (middle) and LEMO front panel layouts.

Note: Only the aluminium portion without the extractor handle mounting fixtures is shown



19.3 Flat cable Input/Output Pin Assignments**19.3.1 ECL**

Data-Connector Channel 1-16

| PIN | SIGNAL | SIGNAL | PIN |
|-----|--------|--------|-----|
| 32 | IN16 - | IN16 + | 31 |
| 30 | IN15 - | IN15 + | 29 |
| 28 | IN14 - | IN14 + | 27 |
| 26 | IN13 - | IN13 + | 25 |
| 24 | IN12 - | IN12 + | 23 |
| 22 | IN11 - | IN11 + | 21 |
| 20 | IN10 - | IN10 + | 19 |
| 18 | IN9 - | IN9 + | 17 |
| 16 | IN8 - | IN8 + | 15 |
| 14 | IN7 - | IN7 + | 13 |
| 12 | IN6 - | IN6 + | 11 |
| 10 | IN5 - | IN5 + | 9 |
| 8 | IN4 - | IN4 + | 7 |
| 6 | IN3 - | IN3 + | 5 |
| 4 | IN2 - | IN2 + | 3 |
| 2 | IN1 - | IN1 + | 1 |

Front view

INx + = ECL High active
INx - = ECL Low active

Data-Connector Channel 17-32

| PIN | SIGNAL | SIGNAL | PIN |
|-----|--------|--------|-----|
| 32 | IN32 - | IN32 + | 31 |
| 30 | IN31 - | IN31 + | 29 |
| 28 | IN30 - | IN30 + | 27 |
| 26 | IN29 - | IN29 + | 25 |
| 24 | IN28 - | IN28 + | 23 |
| 22 | IN27 - | IN27 + | 21 |
| 20 | IN26 - | IN26 + | 19 |
| 18 | IN25 - | IN25 + | 17 |
| 16 | IN24 - | IN24 + | 15 |
| 14 | IN23 - | IN23 + | 13 |
| 12 | IN22 - | IN22 + | 11 |
| 10 | IN21 - | IN21 + | 9 |
| 8 | IN20 - | IN20 + | 7 |
| 6 | IN19 - | IN19 + | 5 |
| 4 | IN18 - | IN18 + | 3 |
| 2 | IN17 - | IN17 + | 1 |

Front view

INx + = ECL High active
INx - = ECL Low active

Control-Connector Input 1-4 /Output 5-8

| PIN | SIGNAL | SIGNAL | PIN |
|-----|--------|--------|-----|
| 20 | GND | GND | 19 |
| 18 | OUT8- | OUT8+ | 17 |
| 16 | OUT7- | OUT7+ | 15 |
| 14 | OUT6- | OUT6+ | 13 |
| 12 | OUT5- | OUT5+ | 11 |
| 10 | GND | GND | 9 |
| 8 | IN4 - | IN4 + | 7 |
| 6 | IN3 - | IN3 + | 5 |
| 4 | IN2 - | IN2 + | 3 |
| 2 | IN1 - | IN1 + | 1 |

Front view

INx + = ECL High active
INx - = ECL Low active

OUTx + = ECL High active
OUTx - = ECL Low active

19.3.2 TTL

Data-Connector Channel 1-16

| PIN | SIGNAL | SIGNAL | PIN |
|-----|--------|--------|-----|
| 32 | IN16 - | GND | 31 |
| 30 | IN15 - | GND | 29 |
| 28 | IN14 - | GND | 27 |
| 26 | IN13 - | GND | 25 |
| 24 | IN12 - | GND | 23 |
| 22 | IN11 - | GND | 21 |
| 20 | IN10 - | GND | 19 |
| 18 | IN9 - | GND | 17 |
| 16 | IN8 - | GND | 15 |
| 14 | IN7 - | GND | 13 |
| 12 | IN6 - | GND | 11 |
| 10 | IN5 - | GND | 9 |
| 8 | IN4 - | GND | 7 |
| 6 | IN3 - | GND | 5 |
| 4 | IN2 - | GND | 3 |
| 2 | IN1 - | GND | 1 |

Front view

INx - = TTL Low active (74F245)

Data-Connector Channel 17-32

| PIN | SIGNAL | SIGNAL | PIN |
|-----|--------|--------|-----|
| 32 | IN32 - | GND | 31 |
| 30 | IN31 - | GND | 29 |
| 28 | IN30 - | GND | 27 |
| 26 | IN29 - | GND | 25 |
| 24 | IN28 - | GND | 23 |
| 22 | IN27 - | GND | 21 |
| 20 | IN26 - | GND | 19 |
| 18 | IN25 - | GND | 17 |
| 16 | IN24 - | GND | 15 |
| 14 | IN23 - | GND | 13 |
| 12 | IN22 - | GND | 11 |
| 10 | IN21 - | GND | 9 |
| 8 | IN20 - | GND | 7 |
| 6 | IN19 - | GND | 5 |
| 4 | IN18 - | GND | 3 |
| 2 | IN17 - | GND | 1 |

Front view

INx - = TTL Low active (74F245)

Control-Connector Input 1-4 /Output 5-8

| PIN | SIGNAL | SIGNAL | PIN |
|-----|--------|--------|-----|
| 20 | GND | GND | 19 |
| 18 | OUT8- | GND | 17 |
| 16 | OUT7- | GND | 15 |
| 14 | OUT6- | GND | 13 |
| 12 | OUT5- | GND | 11 |
| 10 | GND | GND | 9 |
| 8 | IN4 - | GND | 7 |
| 6 | IN3 - | GND | 5 |
| 4 | IN2 - | GND | 3 |
| 2 | IN1 - | GND | 1 |

Front view

INx - = TTL Low active (74F245)

OUTx - = TTL Low active (74F244)

19.4 List of Jumpers

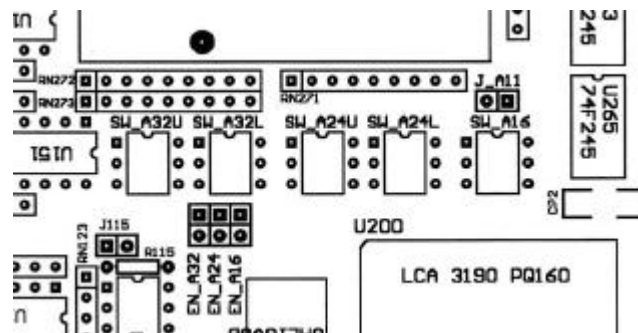
Find below a list of the jumpers and jumper arrays.

| Jumper Name | Array/Single | Function |
|-------------|--------------|--|
| J101 | Single | Input Termination Control Input 1 |
| J102 | Single | Input Termination Control Input 2 |
| J103 | Single | Input Termination Control Input 3 |
| J104 | Single | Input Termination Control Input 4 |
| J105 | Single | Input Termination Control Input 5 |
| J106 | Single | Input Termination Control Input 6 |
| J107 | Single | Input Termination Control Input 7 |
| J108 | Single | Input Termination Control Input 8 |
| J115 | Single | Level Configuration (not for end user) |
| J500 | Array | Boot File Selection |
| J520 | Single | VME SYSRESET Behaviour |
| EN_A16 | Single | Enable A16 addressing |
| EN_A24 | Single | Enable A24 addressing |
| EN_A32 | Single | Enable A32 addressing |
| J_A11 | Single | Address Bit 11 Selection |

19.5 Jumper and rotary switch locations

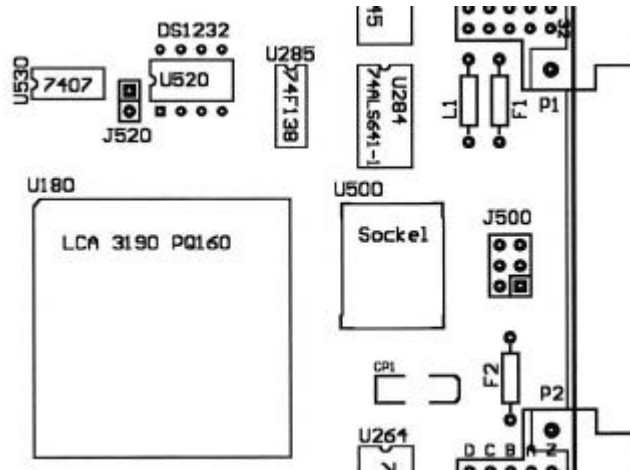
19.5.1 Addressing mode and base address selection

The EN_A32, EN_A24, EN_A16, A_11 and the 5 rotary switches are located in the middle of the upper section of the board close to the DC/DC converter, the corresponding section of the PCB is shown below.

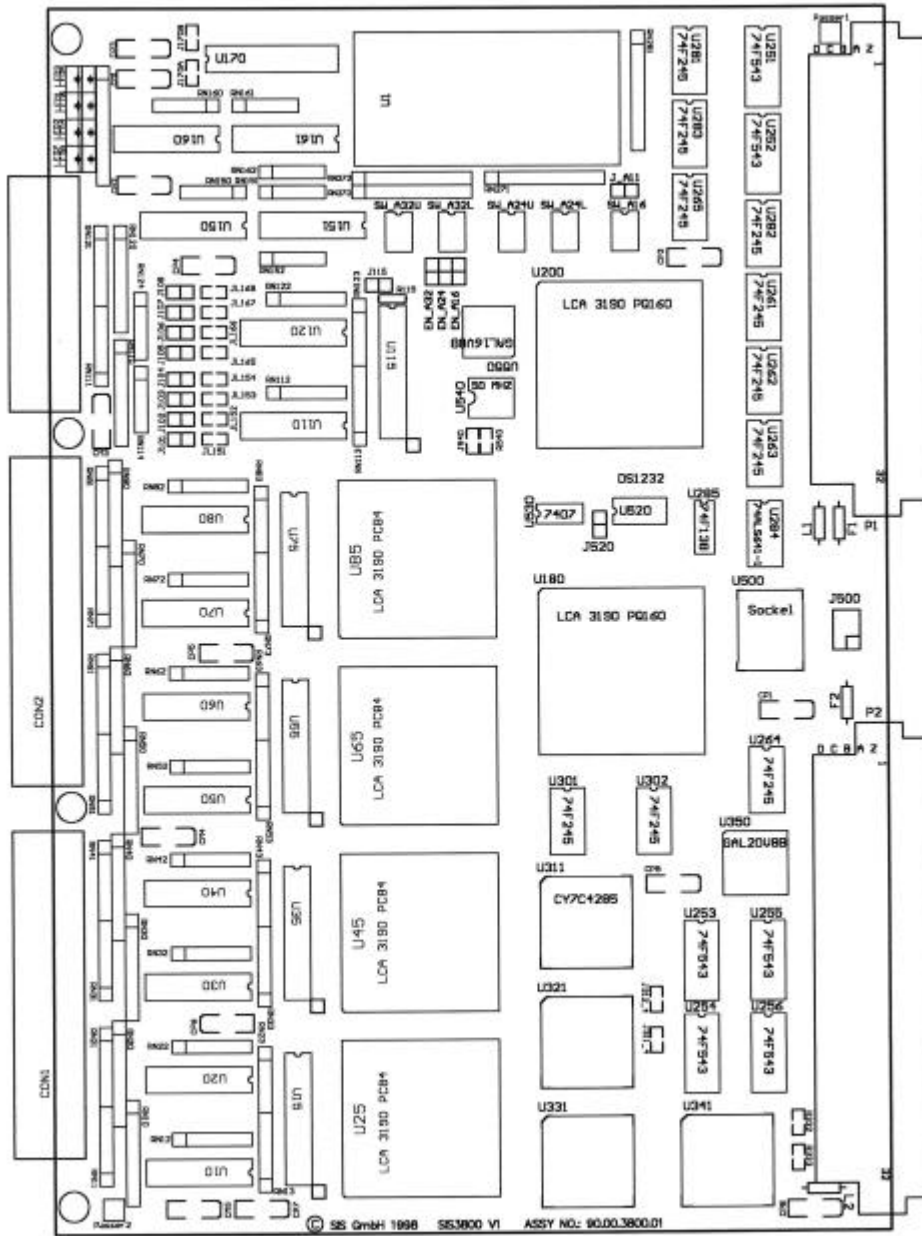


19.5.2 J500 (Bootfile Selection) and J520 (SYSRESET Behaviour)

The jumper array J500 is located between the P1 and the P2 connector. An open position in J500 defines a one (see also chapter 4), the lowest bit is next to the P2 connector. J520 is located to the left of J500 and closer to the DC-DC converter. With jumper J520 closed the SIS3800 executes a key reset upon the VME SYSRESET signal. The section of the board with the jumper array and the SYSRESET jumper is shown below.



19.6 Board Layout



19.7 FLASHPROM Versions

A list of available FLASHPROMs can be obtained from <http://www.struck.de/sis3638firm.htm>. Please note, that a special hardware configuration may be necessary for the firmware design of interest (the SIS3801 design requires the installation of a FIFO e.g.).

The table on the web is of the format shown below:

SIS36/38xx FLASHPROM table

| Design Name | Design | Boot File (s) |
|----------------|--------|-----------------------------------|
| SIS3800_201098 | 0 | SIS3800 Version 1 |
| SIS3801_201098 | 0 | SIS3800 Version 1 |
| | 1 | SIS3800 Version 2 |
| | 2 | SIS3801 Version 1 (32-bit Design) |
| | 3 | SIS3801 Version 2 (24-bit Design) |
| SIS3803_131198 | 0 | SIS3803 Version 1 |

19.8 Row d and z Pin Assignments

The SIS3800 is prepared for the use with VME64x and VME64xP backplanes. Foreseen features include geographical addressing and live insertion (hot swap). The prepared pins on the d and z rows of the P1 and P2 connectors are listed below.

| Position | P1/J1 | | P2/J2 | |
|----------|-------|---------|-------|---------|
| | Row z | Row d | Row z | Row d |
| 1 | | VPC (1) | | |
| 2 | GND | GND (1) | GND | |
| 3 | | | | |
| 4 | GND | | GND | |
| 5 | | | | |
| 6 | GND | | GND | |
| 7 | | | | |
| 8 | GND | | GND | |
| 9 | | GAP* | | |
| 10 | GND | GA0* | GND | |
| 11 | RESP* | GA1* | | |
| 12 | GND | | GND | |
| 13 | | GA2* | | |
| 14 | GND | | GND | |
| 15 | | GA3* | | |
| 16 | GND | | GND | |
| 17 | | GA4* | | |
| 18 | GND | | GND | |
| 19 | | | | |
| 20 | GND | | GND | |
| 21 | | | | |
| 22 | GND | | GND | |
| 23 | | | | |
| 24 | GND | | GND | |
| 25 | | | | |
| 26 | GND | | GND | |
| 27 | | | | |
| 28 | GND | | GND | |
| 29 | | | | |
| 30 | GND | | GND | |
| 31 | | GND (1) | | GND (1) |
| 32 | GND | VPC (1) | GND | VPC (1) |

Note: Pins designated with (1) are so called MFBL (mate first-break last) pins on the installed 160 pin connectors, VPC(1) pins are connected via inductors.

19.9 Geographical Address Pin Assignments

The SIS38xx board series is prepared for geographical addressing via the geographical address pins GA0*, GA1*, GA2*, GA3*, GA4* and GAP*. The address pins are left open or tied to ground by the backplane as listed in the following table:

| Slot Number | GAP* Pin | GA4* Pin | GA3* Pin | GA2* Pin | GA1* Pin | GA0* Pin |
|-------------|----------|----------|----------|----------|----------|----------|
| 1 | Open | Open | Open | Open | Open | GND |
| 2 | Open | Open | Open | Open | GND | Open |
| 3 | GND | Open | Open | Open | GND | GND |
| 4 | Open | Open | Open | GND | Open | Open |
| 5 | GND | Open | Open | GND | Open | GND |
| 6 | GND | Open | Open | GND | GND | Open |
| 7 | Open | Open | Open | GND | GND | GND |
| 8 | Open | Open | GND | Open | Open | Open |
| 9 | GND | Open | GND | Open | Open | GND |
| 10 | GND | Open | GND | Open | GND | Open |
| 11 | Open | Open | GND | Open | GND | GND |
| 12 | GND | Open | GND | GND | Open | Open |
| 13 | Open | Open | GND | GND | Open | GND |
| 14 | Open | Open | GND | GND | GND | Open |
| 15 | GND | Open | GND | GND | GND | GND |
| 16 | Open | GND | Open | Open | Open | Open |
| 17 | GND | GND | Open | Open | Open | GND |
| 18 | GND | GND | Open | Open | GND | Open |
| 19 | Open | GND | Open | Open | GND | GND |
| 20 | GND | GND | Open | GND | Open | Open |
| 21 | Open | GND | Open | GND | Open | GND |

19.10 Additional Information on VME

The VME bus has become a popular platform for many realtime applications over the last decade. Information on VME can be obtained in printed form, via the web or from newsgroups. Among the sources are the VMEbus handbook, <http://www.vita.com> (the home page of the VME international trade association (VITA)) and comp.bus.arch.vmebus. In addition you will find useful links on many high energy physics labs like CERN or FNAL

20 Index

- 24-bit mode 17
- 25 MHz Pulser 26
- 25 MHz test pulses 15
- 32-bit mode 17
- A_11 9, 32
- A16 9
- A24 9
- A24 Broadcast Example** 18
- A32 9
- A32 Broadcast Example** 18
- Address Map 13
- Address Modifier Overview 28
- address modifiers 28
- Address Space 12
- addressing
 - A16, A24, A32 32
- addressing mode 28
- Addressing mode 32
- addressing modes 12
- Addressing 9
- Base address 9
- Base Address 12, 32
- block diagram 6
- BLT 28
- Board Layout 34
- Boot File Selection 32
- Bootfile Selection 33
- Broadcast Addressing 17
- broadcast handshake controller 17
- broadcast mode 15
- broadcast mode handshake controller 15
- broadcast time jitter 17
- CBLT 28
- CERN 37
- Clear Logic 8
- Connector Specification 23
- Control and Status register 13
- Control Input 32
- Control Input Modes 24
- Control Register 15
- Cooling 25
- Count disable register 17
- Count Enable 8
- custom firmware 6
- CVI 27
 - call back routines 27
 - project file 27
- D08(O) 16
- D16 20
- D32 20
- Data Format 20
- DC/DC converter 32
- drivers 27
- ECL 5, 21, 30
- En_A16 9
- EN_A16 12, 32
- En_A24 9
- EN_A24 12, 32
- En_A32 9
- EN_A32 12, 32
- External Latch Shadow Input 19
- Factory Default Settings 9
- firmware 5
 - firmware design 9, 16
 - Firmware Design 9
 - Firmware Selection 10
 - Bootfile 10
 - Examples 10
 - FLASHPROM 5, 6, 9, 10
 - FLASHPROM Versions 35
 - flat cable 5
 - Floppy 27
 - FNAL 37
 - Front Panel
 - LED 11
 - Front Panel Layout 29
 - GA0* 37
 - GA1* 37
 - GA2* 37
 - GA3* 37
 - GA4* 37
 - GAP* 37
 - geographical address
 - pins 37
 - Geographical Address 37
 - geographical addressing 36
 - Getting Started 9
 - hot swap 25, 36
 - http
 - //www.vita.com 37
 - Input Configuration 21
 - input mode 15
 - Input Priority 26
 - input test mode 15, 26
 - Insertion/Removal 25
 - interrupt acknowledge cycle 16
 - interrupt condition 19
 - interrupt control 16
 - interrupt level 16, 19
 - interrupt logic 19
 - interrupt vector 16, 19
 - interrupter type 16
 - IRQ source 15
 - J_A11 12, 32
 - J101-J108 32
 - J115 32
 - J500 9, 32, 33
 - J520 9, 32, 33
 - jumper
 - firmware selection 10
 - VME addressing mode 12
 - Jumper
 - overview 32
 - Jumper and rotary switch locations 32
 - key address 13
 - LED 11
 - Access 11
 - Color 11
 - Power 11
 - Ready 11
 - user 9
 - LEMO 5
 - live insertion 25, 36
 - Module Identification and IRQ control register 13, 16
 - module number 16
 - monostable 11

| | | | |
|----------------------------|-------|-------------------------------|-----------|
| NIM | 5, 22 | SYSRESET Behaviour | 33 |
| Operating Conditions | 25 | System Reset | 10 |
| OR VP6 | 27 | Technical Properties/Features | 6 |
| Overflow | 19 | Test Interrupt | 19 |
| Overflow registers | 17 | TTL | 5, 23, 31 |
| PCB | 6 | version number | 16 |
| Pentium II | 27 | VIPA | 25 |
| Pin Assignments | 30 | addressing | 5 |
| Power Consumption | 25 | base address | 12 |
| Read and Clear Counter | 20 | extractor handles | 5 |
| Read Counter | 20 | LED set | 5 |
| read on the fly | 7 | VITA | 37 |
| Read Shadow Register | 20 | VME | 25, 37 |
| Readout Schemes | 20 | addressing mode | 12 |
| Reference pulser channel 1 | 26 | Base Address | 12 |
| rotary switch | 32 | CPU | 27 |
| shadow register | 7 | SYSRESET | 33 |
| Signal Specification | 25 | SYSRESET Behaviour | 32 |
| Control | 25 | VME addressing | 12 |
| Inputs | 25 | VME control register | 19 |
| Single Pulse | 26 | VME Interrupts | 19 |
| SIS360x/38xx | 5 | VME IRQ and version register | 19 |
| Software Support | 27 | VME64x | 12, 36 |
| Status Register | 14 | connector | 5 |
| SW_A16 | 9, 12 | VME64xP | 5, 12, 36 |
| SW_A24L | 9, 12 | Voltage requirement | 25 |
| SW_A24U | 9, 12 | VxWorks | 27 |
| SW_A32L | 9, 12 | Windows 95 | 27 |
| SW_A32U | 9, 12 | XILINX | 7 |