

THEORY OF OPERATION

INTRODUCTION

SECTION ORGANIZATION

This section of the manual contains a general summary of instrument functions followed by a detailed description of each major circuit. A basic block diagram, a detailed block diagram, and the schematic diagrams are located in the tabbed "Diagrams" section at the back of this manual. They are used to show the interconnections between parts of the circuitry, to indicate circuit components, and to identify inter-relationships with the front-panel controls.

The schematic diagram number associated with each description is identified in the text and is shown on the block diagrams. For best understanding of the circuit being described, refer to the appropriate schematic diagram and the two block diagrams.

INTEGRATED CIRCUIT DESCRIPTIONS

Digital Logic Conventions

Digital logic circuits perform many functions within the instrument. Functions and operation of the logic circuits are represented by logic symbology and terminology. Most logic functions are described using the positive-logic convention. Positive logic is a system of notation whereby the more positive of two levels is the TRUE (or 1) state; the more negative level is the FALSE (or 0) state. In this logic description the TRUE state is referred to as HI, and the FALSE state is referred to as LO. The specific voltages which constitute a HI or a LO state vary between specific devices. For specific device characteristics, refer to the manufacturer's data book.

Linear Devices

The functioning of individual linear circuit devices in this section use waveforms or other techniques such as voltage measurement and simplified diagrams to illustrate their operation.

GENERAL DESCRIPTION

NOTE

When reading this general circuit description of the 2235 Oscilloscope, refer to the basic block diagram (Figure 9-4) and to the detailed block diagram (Figure 9-5) located in the "Diagrams" section of this manual. In Figures 9-4 and 9-5, the numbered diamond symbol in each major block refers to the appropriate schematic diagram number.

Signals to be displayed on the crt are applied to either the CH 1 OR X input connector or the CH 2 OR Y input connector. These signals may be directly (DC) coupled to the Attenuator circuit or ac (AC) coupled through an input-coupling capacitor. The input signals may also be disconnected from the oscilloscope circuitry and the input attenuator grounded by setting the coupling switch to the GND position.

The output signal from the Attenuator circuit is applied to the Vertical Preamplicifier for further amplification. Additionally, the Channel 2 Attenuator can invert the Channel 2 display on the crt. Trigger Pickoff Amplifiers in each channel supply an internal trigger signal from either or both channels to the Internal Trigger Amplifier.

Input signals are selected for display by the Channel Switching circuit under control of the front-panel VERTICAL MODE switches. The output signal from the Channel Switching circuit is applied to a Diode Gate circuit to enable either the vertical or trigger view signal to drive the Delay Line Driver stage. This stage converts a current input to a voltage output and provides an impedance match for the Delay Line. The Delay Line produces approximately 90 ns of delay in the vertical signal. This allows the Horizontal circuitry time to start the sweep so that the operator can see the signal that triggered the sweep.

Final amplification of the vertical signal is performed by the Vertical Output Amplifier. This Amplifier supplies the signal levels necessary for vertical deflection of the electron beam in the crt. The upper frequency response of the Amplifier can be reduced by enabling the Bandwidth Limit circuitry. For locating the position of off-screen displays, the dynamic range of the Amplifier can be limited with the Beam Find circuitry. This circuitry also intensifies the trace and limits horizontal deflection.

The A/B Sweep Separation circuitry supplies a dc-offset current to the Vertical Output Amplifier which vertically posi-

tions the B trace with respect to the A trace when Alt Horizontal Mode is selected.

The A Trigger circuitry uses either an Internal Trigger signal, an External Trigger signal, or a Line Trigger signal obtained from the ac power line to develop the gate signal for the A Sweep Generator. The B Trigger circuitry uses only the Internal Trigger signal to gate the B Sweep Generator. A P-P Auto Trigger circuit ensures that the range of the A TRIGGER LEVEL control tracks the peak-to-peak amplitude of the trigger signal when either the P-P Auto or TV Field trigger mode is selected. This allows triggering on most signals without needing to adjust the A TRIGGER LEVEL control. In Norm mode, the A TRIGGER LEVEL control must be adjusted for the correct trigger signal level before a sweep can be generated. When the TRIG VIEW switch is activated, the signal appearing at the input of the A Trigger circuit is applied to the Delay Line Driver and displayed on the crt.

A TV Field sync circuit provides stable triggering on television vertical-sync pulses. Triggering at the television line rate is accomplished when either P-P Auto or Norm mode is selected.

The A Sweep Logic circuit controls sweep generation and Z-Axis unblanking for the A Sweep display. When the A TRIGGER Mode switches are set to either P-P AUTO or TV FIELD and no trigger signal is present, the Auto Baseline circuit causes the Sweep Logic circuit to produce a sweep for reference purposes. In the NORM setting, the Auto Baseline circuit is disabled and sweeps are inhibited until a trigger event occurs. This is useful for triggering on low-repetition-rate signals. The SGL SWP setting enables only one sweep to be generated after being reset. Following the single sweep, the A Trigger circuit is disabled until the SGL SWP button is pressed again.

The A Sweep Logic circuit controls the operation of the A Miller Sweep Generator circuit. The Sweep circuit produces a linear sweep output with a ramp time that is controlled by the A SEC/DIV switch. The sweep signal is applied to the Horizontal Preamplicifier for initial amplification and then to the Horizontal Output Amplifier to drive the crt horizontal deflection plates.

The Horizontal Preamplicifier gain is increased by a factor of 10 when the X10 Magnifier is used. Horizontal positioning of the display is accomplished in the Horizontal Preamplicifier circuit.

In the X-Y mode of operation, the Channel 1 signal from the Internal Trigger circuitry passes through the X-Y Amplifier to the Horizontal Preamp. In this operating mode, the Channel 1 Internal Trigger signal supplies the horizontal deflection to the crt, and the Miller Sweep circuit is disabled to inhibit sweep generation.

The Alternate B Sweep circuitry controls the Alt and B Horizontal mode displays and includes the B Miller Sweep Generator and B Sweep Logic circuitry. In addition to providing the B Sweep sawtooth waveform, signals are generated which control the display switching between the A and B displays.

The intensity levels of both the A and B Sweeps are set by the front-panel A and B INTENSITY controls. These controls, along with signals from the A and B Sweep Logic circuits, determine the drive level to the Z-Axis Amplifier.

The Z-Axis drive from both the A Sweep Logic circuit and the Alternate B Sweep circuit is applied to the Z-Axis Amplifier. The output signal from the Z-Axis Amplifier circuit sets the crt intensity. When using Chop Vertical mode, a blanking

signal from the Chop Oscillator circuit blanks the crt display while switching between the vertical channels.

The Dc Restorer circuit applies the output voltage of the Z-Axis Amplifier between the cathode and grid of the crt. High dc potentials on these elements prohibit direct coupling to the crt.

The Power Supply provides the necessary operating voltages for the instrument. Operating potentials are obtained from a circuit composed of the Preregulator, Inverter and Transformer, and Rectifiers and Filters. The Preregulator produces approximately +43 V dc from the ac power line which is used to drive the 20 kHz Inverter stage. The transformer secondary windings provide various ac levels that are rectified and filtered to produce the operating voltages. A high-voltage multiplier circuit produces the accelerating, focus, and cathode potentials required by the crt.

A front-panel PROBE ADJUST output is provided for use in adjusting probe compensation. The voltage at the PROBE ADJUST connector is a negative-going square wave that has a peak-to-peak amplitude of approximately 0.5 V and a repetition rate of approximately 1 kHz.

DETAILED CIRCUIT DESCRIPTION

VERTICAL ATTENUATORS

The Channel 1 and Channel 2 Attenuator circuits, shown on Diagram 1, are identical with the exception of the additional Invert circuitry in the Channel 2 Paraphase Amplifier. Therefore, only the Channel 1 Attenuator will be described and the Invert circuitry of Channel 2 will be discussed separately.

The Attenuator circuit (see Figure 3-1) provides control of input coupling, vertical deflection factor, and variable volts-per-division gain. Input signals for crt vertical deflection may be connected to the CH 1 OR X and the CH 2 OR Y input connectors. In the X-Y mode of operation, the signal applied to the CH 1 OR X connector provides horizontal (X-Axis) deflection for the display, and the signal applied to the CH 2 OR Y connector provides the vertical (Y-Axis) deflection for the display.

Input Coupling

The signal applied to the CH 1 OR X input connector can be ac coupled, dc coupled, or disconnected from the input of the High-Impedance Input Attenuator circuit. Signals applied to the CH 1 OR X input connector are routed through resistor R9100 to Input Coupling switch S1. When S1 is set for dc coupling, the Channel 1 signal is applied directly to the input of the High-Impedance Attenuator stage. When ac coupled, the input signal passes through dc-blocking capacitor C2. The blocking capacitor prevents the dc component of the input signal from being applied to the Attenuator circuit. When switched into the signal path, attenuators AT1 and AT2 attenuate the input signal by factors of 100 and 10 respectively. When S1 is set to GND, the direct signal path is opened and the input of the Buffer Amplifier is connected to ground. This provides a ground reference without the need to disconnect the applied signal from the input connector. The coupling capacitor precharges through R4 to prevent large trace shifts when switching from GND to AC.

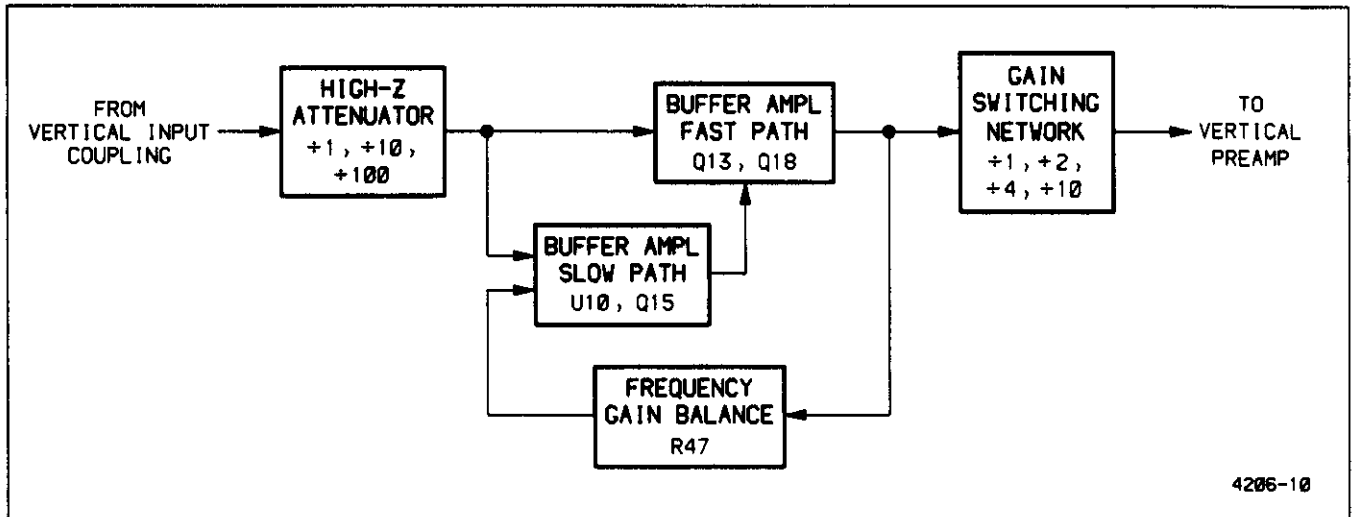


Figure 3-1. Block diagram of the Vertical Attenuators.

Buffer Amplifier and Gain Switching Network

The Buffer Amplifier presents a high-impedance, low-capacitance load to the signal from the High-Impedance Attenuator and a low output impedance to the Gain Switching Network. A dual-path amplifier is used to combine high-dc stability with high-speed performance.

In the slow path, the input signal is applied to both the gate of source-follower Q13 and the inverting input of U10 through the divide-by-two network composed of R3 and R5. Transistor Q13 and emitter-follower Q18 isolate the input signal from the loading of the Gain Switching Network. The divider network at the output of the Amplifier (R46, R47, and R48) is connected to the other input of U10. Amplifier U10 compares the two divider voltages and changes the conduction level of current-source transistor Q15 to correct for any error at the source of Q13. Capacitor C10 limits the bandwidth of U10 so that the slow path responds only to frequencies below 100 kHz.

In the fast path, input signals are coupled through R6, C6, Q13, and Q18 to the circuit output. By adjusting R47, the gain in both paths is matched. Input offset voltage compensation for U10 is provided by R10 to eliminate trace shifts when switching between Volts/Div settings.

The Gain Switching Network divides down the Buffer Amplifier output signal for application to the Paraphase Amplifier and has an output impedance of 75 Ω for all Volts/Div switch settings. The particular Volts/Div switch setting will determine which contacts of S10 are closed and therefore whether the Paraphase Amplifier will receive a $\div 1$, $\div 2$, $\div 4$, or $\div 10$ signal.

Paraphase Amplifier

The Paraphase Amplifier converts the single-ended signal from the Gain Switching Network into a differential signal for application to the Vertical Preamplifier. Included in the circuitry is switching that provides extra gain for the 2 mV position of the VOLTS/DIV switch, adjustments for amplifier dc balance, and circuitry for the Variable Volts/Div function. Additionally, the Channel 2 Paraphase Amplifier contains circuitry to invert the Channel 2 display.

The signal from the Gain Switching Network is applied to the base of one transistor in U30. The other input transistor is biased by the divider network composed of R30, R31, and R33 to a level that will produce a null between the outputs of U30 (no trace shift on the crt screen) when the VOLTS/DIV control is switched between 5 mV and 2 mV. Emitter current for the two input transistors is supplied by R21, R22, R23, and R25, with R29 serving as the gain-setting resistor between the two emitters. In the 2 mV position, amplifier gain is increased by closing contact 15 of S10 to shunt R29 with R26.

The collector current through the two input transistors serves as emitter current for the two differential output transistor pairs. Base-bias voltages for the two pairs are derived from the divider network composed of R39, R41, R42, and R43. Monolithic IC U30 has matched transistor characteristics, so the ratio of currents in the two diodes connected to pin 11 determines the current ratios in the output transistor pairs. As VOLTS/DIV Variable potentiometer R43 is rotated from the calibrated to uncalibrated position, the conduction level of the transistors connected to R35 will increase. Since the transistor pair outputs are cross-wired, this increased conduction will subtract from the signal produced by the

transistors connected to R38 and the overall gain of the Amplifier will decrease. Potentiometer R25 adjusts the balance of the Amplifier so there is minimal dc trace shift as the VOLTS/DIV Variable control is rotated.

Incorporated in the Channel 2 Paraphase Amplifier is circuitry to invert the polarity of the Channel 2 signal. When INVERT switch S90 is out, the transistor pairs in U80 are biased as they are in U30 and there is no trace inversion. For the IN position of S90, connections to the bases of the output transistor pairs are reversed to produce an inverted Channel 2 trace. Potentiometer R75 is adjusted so that there is minimal dc trace shift as the INVERT button is changed between the IN and OUT positions.

VERTICAL PREAMPLIFIERS

The Vertical Preamp, shown on Diagram 2, utilizes differential signal current from the Paraphase Amplifier to produce differential output current to drive the Delay Line Driver. Internal trigger signals for the Trigger circuitry are picked-off and channel selection for crt display is controlled by the Channel Switch circuitry.

Common-base transistors Q102 and Q103 convert differential current from the Paraphase Amplifier into level-shifted voltages that drive the bases of the input transistors of U130 and the Internal Trigger circuitry. Emitter current for the input transistors is supplied by Q114 and Q115, and the base bias is adjusted by R111. The collector current of each input transistor of U130 serves as emitter current for two differential output transistor pairs. One of the collectors of each output pair is grounded and the other provides output drive to the Delay Line Driver. The base voltages of the transistors with grounded collectors are held at ground potential by R136. The base voltages of the other transistors are controlled by the Channel Switch and Trigger View circuitry.

When Channel 1 is selected to drive the Delay Line Driver, the Q output of U540A is HI. The transistors with the ungrounded collectors will then be forward-biased and the Channel 1 signal will be conducted through to the Delay Line Driver. If Channel 1 is not selected, then the Q output of U540A is LO. The transistors with the ungrounded collectors are then reverse-biased and the output signals will be conducted to ground by the other transistor pair. The gain of the Preamp is set by adjusting R145 to determine how much signal current will be shunted between the two differential outputs.

When TRIG VIEW push button S200 is pressed in, -8.6 V is applied to R138 and R188 to turn off the transistors in U130 and U180 with ungrounded collectors. Both the

Channel 1 and Channel 2 output signals are then conducted to ground. Zener diode VR200 turns on and CR200 and CR201 become reverse biased. Trigger View transistors Q440 and Q441 are then coupled to the Delay Line Driver through forward-biased diodes CR202 and CR203. The crt trace will then be a display of the A Trigger signal.

CHANNEL SWITCH AND VERTICAL OUTPUT

The Channel Switch circuitry, shown on Diagram 2, utilizes the front-panel VERTICAL MODE switches to select the crt display format. See Figure 3-2 for a block diagram of the circuit.

When any display mode other than X-Y is selected, the XY line connected to S550 is at ground potential. VERTICAL MODE switches S545 and S550 control the connection between the XY line and the \bar{S} and \bar{R} inputs of U540A to obtain the various display formats described below.

CHANNEL 1 DISPLAY ONLY. The CH 1 position of S550 grounds the \bar{S} input of U540A while the \bar{R} input is held HI by R539. This will produce a HI and a LO on the Q and \bar{Q} outputs respectively, and the Channel 1 Preamp signal will drive the Delay Line Driver as described in the "Vertical Preamp" section. The Channel 2 Preamp will be disabled.

CHANNEL 2 DISPLAY ONLY. The CH 2 position of S550 holds the \bar{R} input of U540A LO through CR538 and the \bar{S} input is held HI by R538. The outputs will then be Q LO and \bar{Q} HI to enable the Channel 2 Preamp signal to drive the Delay Line Driver while the Channel 1 Preamp is disabled.

To display the ADD, ALT, or CHOP formats, S550 must be in the BOTH position to ground the A, C, and F pins of S545.

ADD DISPLAY. In the ADD position of S545, both the \bar{S} and \bar{R} inputs of U540A are held LO by CR534 and CR537. The Q and \bar{Q} outputs are then both HI and signal currents from the Channel 1 and Channel 2 Preamps add together to drive the Delay Line Driver.

CHOP DISPLAY. In the CHOP position, the Chop Enable line is held LO keeping the Q output of U540B HI. This enables multivibrator U537D to run at a frequency that is determined by R544, R545, and C545. The output of U537C, the inverted output of the multivibrator, is used to drive U537A and U537B.

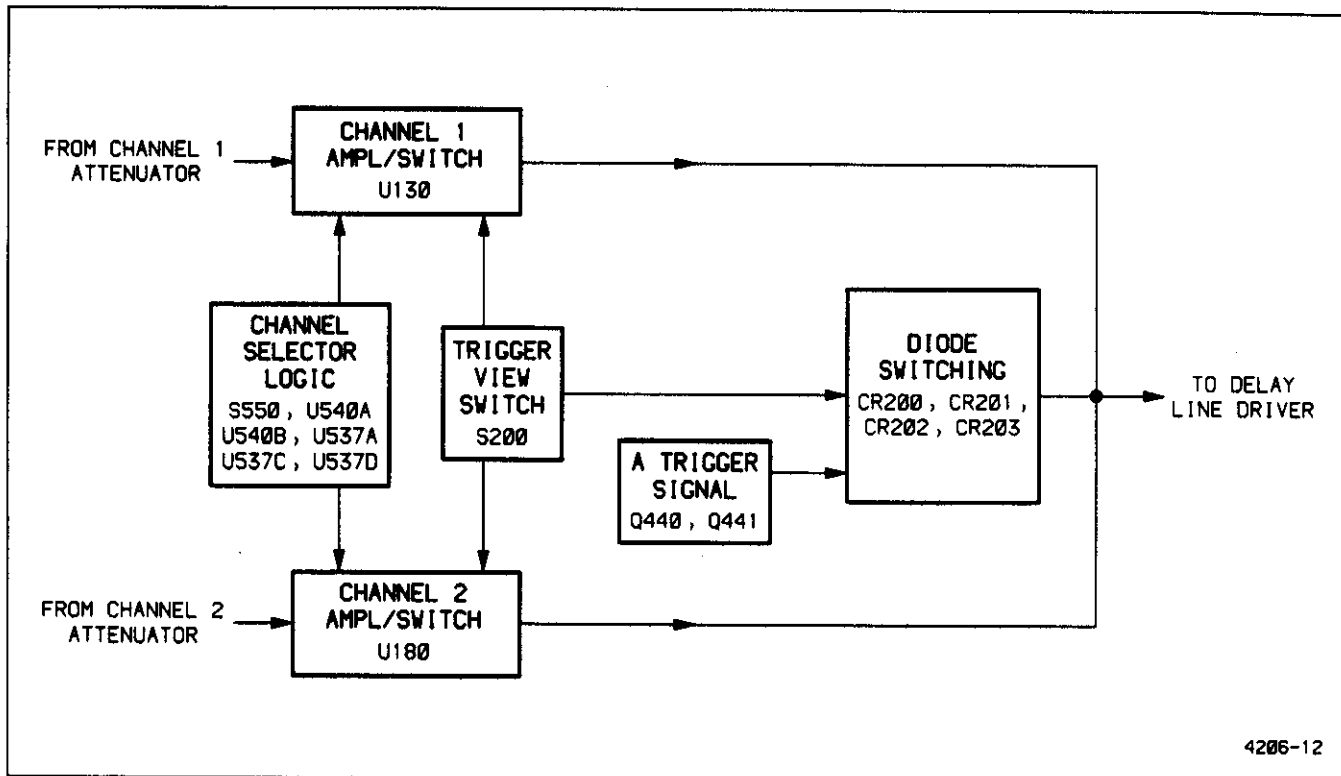


Figure 3-2. Block diagram of the Channel Switching circuitry.

Coupling capacitor C547 and resistors R547 and R548 form a differentiating circuit that produces positive- and negative-going short-duration pulses. These pulses are inverted by U537B to generate the Chop Blank signal utilized by the Z-Axis Amplifier.

The Alt Sync signal applied to one input of U537A is HI except during Holdoff. This allows the output of U537C to be inverted by U537A which drives the clock input of U540A. Since the \bar{Q} output of U540A is connected back to the D input and both the \bar{S} and \bar{R} inputs are HI, the outputs of U540A will toggle with each clock input. The Delay Line Driver will then be driven alternately by the Channel 1 and Channel 2 Preamplifiers at a rate determined by multivibrator U537D.

ALTERNATE DISPLAY. In the ALT position, the $\bar{\text{Chop Enable}}$ line is held HI and multivibrator U537D is disabled. The output of U537C will be LO and the Chop Blank signal from U537B will also be LO. Input signals to U537A will be the LO from U537C and the Alt Sync signal from the Holdoff circuitry in the A Sweep Generator. The output of U537A will then be the inverted Alt Sync signal which clocks U540A. This causes the outputs of U540A to toggle at the end of each sweep so that the Channel 1 and Channel 2 Preamplifier signals will alternately drive the Delay Line Driver.

Delay Line Driver

The Delay Line Driver converts the signal current from the Vertical Preamplifiers or the Trigger View circuitry into a signal voltage for input to the Delay Line. Transistors Q202, Q203, Q206, and Q207 form a differential shunt-feedback amplifier with the gain controlled by R216 and R217. Amplifier compensation is provided by C210 and R210 and output common-mode dc stabilization by U225. Should the voltage at the junction of R222 and R223 deviate from zero, U225 will sink or source base current to Q202 and Q203 through R202 and R203. This will return the outputs of the Delay Line Driver to an average dc value of zero volts. Delay Line DL210 provides a vertical signal delay of about 90 ns so that the Sweep Generator has sufficient time to produce a sweep before the vertical signal that triggered the sweep reaches the crt deflection plates. This permits viewing the leading edge of the internal signal that originated the trigger pulse.

Vertical Output Amplifier

The Vertical Output Amplifier provides final amplification of the input signals for application to the vertical deflection plates of the crt. Signals from the Delay Line are applied to a differential amplifier composed of Q230 and Q231 with low- and high-frequency compensation provided by the RC networks connected between the emitters. Thermal compensation is provided by RT236, and overall gain is set by R233.

The output stage of the Amplifier utilizes two totem-pole transistor pairs, Q254-Q256 and Q255-Q257, that convert the collector currents of Q230 and Q231 to proportional output voltages. Resistors R256, R258, R257, and R259 serve as feedback elements and also as divider networks so that each transistor in a pair drops half the final output voltage. The Amplifier output signals are applied to the vertical deflection plates of the crt to produce deflection of the crt beam.

BW LIMIT switch S226, C228 and C229, and a diode bridge consisting of CR226, CR227, CR228, and CR229, are utilized to reduce the bandwidth of the Amplifier if desired. With the bandwidth limit off, R226 is grounded and the nonconducting diode bridge isolates C228 and C229. With bandwidth limit on, R226 is connected to the +8.6 V supply and the diode bridge conducts. The two capacitors are no longer isolated and will attenuate high-frequency signals.

BEAM FIND switch S390 adjusts output-amplifier biasing to limit the voltage swing at the crt plates. This keeps the vertical trace within the graticule area for locating off-screen traces. With the switch in the normal out position, the -8.6 V supply provides emitter current to the Amplifier output stage through R261. When the BEAM FIND switch is in, the direct -8.6 V supply to R261 is removed and emitter current is now supplied through R261 and R262 in series. This reduces the amount of available emitter current and limits the Amplifier dynamic range.

A/B Sweep Separation Circuit

The circuit composed of Q283, Q284, Q285, and associated components provides a means of vertically positioning the B trace with respect to the A trace during Alt Horizontal Mode displays. During the B Sweep interval, the $\overline{\text{Sep}}$ signal from the Alternate Display Switching circuit is LO and Q283 is biased off. This allows A/B SWP SEP potentiometer R280 to affect the bias on one side of a differential current source composed of Q284 and Q285. This supplies a dc offset current to the Vertical Output Amplifier and changes the position of the B trace on the crt screen.

During the A Sweep interval, the $\overline{\text{Sep}}$ signal is HI and Q283 is turned on. The base voltages of Q284 and Q285 are then the same, and equal current is supplied to both sides of the Vertical Output Amplifier so that no offset of the A trace occurs.

TRIGGER AMPLIFIERS AND SWITCHING

The Trigger Amplifiers, shown on Diagram 3, provide signals to the A Trigger Generator circuit from either the Vertical Preamplifiers, the EXT INPUT connector, or the power

line. The A&B INT switch selects either Channel 1 or Channel 2 as the trigger source, and the A SOURCE switch selects between internal, line, or external trigger sources.

Internal Trigger

Signals from the Vertical Preamplifiers drive the Internal Trigger Amplifier with channel selection determined by the VERTICAL and HORIZONTAL MODE switches.

Trigger pickoff from the Preamplifiers is accomplished by Q302 and Q303 for Channel 1, and Q327 and Q328 for Channel 2. The circuitry associated with Channel 2 is the same as that for Channel 1 except that it does not have a trigger offset adjustment.

Signals from the Channel 1 Preamplifier are applied to Q302 and Q303. These emitter-follower transistors each drive one input transistor in U310, and the collectors of the U310 input transistors in turn supply emitter current to two current-steering transistors. The compensation and biasing network connected to the emitters of the input transistors in U310 is fixed for Channel 2 but not for Channel 1. Potentiometer R309 adjusts the emitter bias levels of the two input transistors so that dc offsets between channels can be matched.

The base bias voltages of one transistor in each output differential amplifier pair is fixed by the divider network composed of R321 and R322. The other base voltage is controlled by the $\overline{\text{Ch 1 Trig}}$ line from the Trigger Channel Switch. When the $\overline{\text{Ch 1 Trig}}$ signal is HI, the transistors in each output pair with the collectors connected together are biased on and the other transistors are off. The collector signal currents are equal in magnitude but opposite in polarity and signal cancellation occurs. If the $\overline{\text{Ch 1 Trig}}$ signal is LO, the other transistors in each pair will be biased on and an output signal will be developed across R314 and R315 to drive the Internal Trigger Amplifier.

Internal trigger channels are chosen by the A&B INT switch with the A SOURCE switch set to INT. The INT position of S392 reverse biases CR393 and CR399 to prevent external trigger signals or the line trigger signal from reaching the A Trigger Generator. Signals from the Internal Trigger Amplifier are passed to the A Trigger Generator through forward-biased CR372.

CHANNEL 1. For triggering from Channel 1, the A&B INT switch is set to CH 1. The XY line connected to S555 will be at ground potential and one input of U555B will be held LO by CR556. The output of U555B will then also be LO and the Channel 1 signal path through U310 will be enabled. The Channel 2 signal path is disabled by the outputs of both U555C and U555B being HI.

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CHANNEL 2. For triggering from Channel 2, the A&B INT switch is set to CH 2. One input each of U555C and U555D will be LO and force both gate outputs LO. The LO from U555C will enable the Channel 2 signal path through U335 and the HI outputs of U555B and U565C will disable the Channel 1 path.

VERT MODE. When the A&B INT switch is set to VERT MODE, trigger source selection is determined by the two VERTICAL MODE switches. For all VERTICAL MODE switch combinations except BOTH-CHOP, the \overline{V} Mode \overline{T} line is HI. The inputs and outputs of U555B, U555C, and U555D will all be HI, and triggering selection will then be determined by the inputs of U565B and U565C that are controlled by U540A in the Channel Switch circuit.

When Channel 1 is selected (VERTICAL MODE switch set to CH 1), the input to U565C will be HI. The gate output will be LO and the Channel 1 signal will be selected. The LO from the other output of U540A is applied to U565B and causes the $\overline{Ch\ 2\ Trig}$ line to go HI and the Channel 2 Trigger signal is disabled.

When Channel 2 is selected (VERTICAL MODE switch set to CH 2), the outputs of U540A, U565B, and U565C will be the reverse of the states described for Channel 1 selection. The Channel 2 signal will be selected and the Channel 1 Trigger signal disabled.

When selecting ALT VERTICAL MODE, the inputs of U565B and U565C will toggle with each sweep. The outputs of the two gates will also toggle and the Trigger signal source will alternate with the displayed channel.

In the ADD VERTICAL MODE position, both inputs to U565B and U565C will be HI and the gate outputs will be LO. Both Channel 1 and Channel 2 signal paths will be enabled and their output current will be summed at the inputs of the Internal Trigger Amplifier to produce the internal trigger signal.

The CHOP VERTICAL MODE position grounds the \overline{V} Mode \overline{T} line and places a LO on an input of both U555B and U555C. The outputs of these two gates will then be LO and the signal to the Internal Trigger Amplifier will be the same as for the ADD mode.

Internal Trigger Amplifier

The Internal Trigger Amplifier converts the differential trigger signals from the Vertical Preamplifiers into a single-ended signal that drives the X-Axis Amplifier and the A and B Trigger Generators.

Signal current is applied to the emitters of U350D and U350E. The collector current of U350D is converted to a voltage across feedback resistor R357. The opposite-phase collector current of U350E causes a voltage drop across R359 which adds to the voltage at the collector of U350C. This voltage appears at the base of U350A which buffers and level shifts the signal back to 0 V. The emitter signal of U350A drives the X-Axis Amplifier, the B Trigger Generator, and the base of U350B. The emitter signal of U350B in turn drives the A Trigger Generator whenever CR372 is forward biased.

A External Trigger Amplifier

The A External Trigger Amplifier buffers signals applied to the EXT INPUT connector to drive the A Trigger Generator. Input signal coupling is determined by A EXT COUPLING switch S380 which selects AC, DC, or DC \div 10 coupling.

When S380 is in the AC position, the input signal is ac-coupled through C376. In the DC position, the input signal is connected directly to the Amplifier. The DC \div 10 position attenuates the input signal by a factor of 10 through the compensated divider composed of R377, R378, C380, and C381.

The signal is then applied to the gate of Q382A. This source-follower drives emitter-follower transistor Q384 which lowers the Amplifier output impedance. The two FETs are a matched pair, and since the gate and source of Q382B are connected together, Q382B will supply source current for Q382A such that there will be no voltage drop across the gate-source junction of Q382A. Protection-diode CR381 clamps the signal at the gate of Q382A to about -9 V. The Amplifier output will drive the A Trigger Generator through forward-biased CR393 whenever the A SOURCE switch is set to EXT. When the A SOURCE switch is not set to EXT, the base-emitter junction of Q384 will be reverse biased and the Amplifier will be disabled.

Line Trigger Amplifier

The Line Trigger Amplifier supplies a line-frequency trigger signal to the A Trigger Generator when the A SOURCE switch is in the LINE position.

Transformer T390 in the Power Supply provides a line-frequency signal through R397 to Q397. Diode CR399 is forward biased when S392 is in the LINE position, and the emitter signals of Q397 will drive the A Trigger Generator.

A TRIGGER GENERATOR

The A Trigger Generator, shown on Diagram 3, supplies trigger signals to the A Sweep Generator. Included in the A Trigger Generator circuit are the P-P Auto Trigger, Auto Baseline, and TV Triggering circuitry.

A Trigger Level Circuit

The A Trigger Level Circuit establishes voltages at the ends of the A TRIGGER LEVEL potentiometer as a function of the A TRIGGER push button selection and trigger signals selected by the A SOURCE switch.

In the P-P Auto and TV Field modes, Q413 is off and CR414 and CR415 are reverse biased. Trigger signals selected by the A SOURCE switch are applied to peak detectors consisting of Q420-Q422 and Q421-Q423. These peak detectors track dc levels and have a high voltage transfer efficiency. The positive- and negative-peak signal levels stored by C414 and C415 are near the peak levels of the trigger signal. Amplifiers U426A and U426B are configured as voltage followers with transistors Q428 and Q429 in the feedback loops. These transistors thermally compensate for Q420 and Q421 and level shift the amplifier outputs back to the original dc levels of the input trigger signals. The output of U426A will be the positive peak voltage of the input trigger signal and the output of U426B will be the negative peak voltage. Potentiometers R434 and R435 adjust for dc offsets in the trigger circuitry.

In the Norm mode, +8.6 V is applied to the junction of R411 and R414. Diode CR414 is forward biased, turning on Q413 which forward biases CR415. Input transistors Q420 and Q421 are then biased off and no trigger signals will reach the A Trigger Level circuit. The inputs and outputs of U426A and U426B will then be fixed voltages and independent of trigger-signal amplitude.

A Trigger Level Comparator

The A Trigger Level Comparator compares signals selected by the A TRIGGER SOURCE switch to a voltage set by the A TRIGGER LEVEL control. Positive or negative slope triggering is selected by the A TRIGGER SLOPE switch.

Transistors U460B and U460E compare the wiper voltage on the A TRIGGER LEVEL control to the input trigger signal, and the transistor with the higher base voltage will conduct more of the available emitter current. The output collector currents supply emitter current to two transistor pairs which serve as cross-wired switches that are biased on or off by the A TRIGGER SLOPE switch. When S464 is set to the positive slope position, U460C and U460F are

biased on and U460A and U460D are biased off. For the negative slope position, the transistors reverse states to invert the comparator output polarity.

A Schmitt Trigger and TV Trigger Circuit

This circuitry generates a signal that drives the A Trigger Logic as a function of the Trigger Level Comparator output signal and the A TRIGGER Mode switches.

The output signals from the A Trigger Level Comparator drive Q460 and Q463. These transistors are configured as a current mirror that converts the differential output to a single-ended current to drive amplifier U480C. Slope Balance potentiometer R471D corrects for dc offsets between positive and negative slope. Shunt-feedback amplifier U480C converts a current input to a voltage output to drive the input of the Schmitt Trigger, U480D, through R469. Positive feedback for the Schmitt Trigger is provided by potentiometer R479, and C479 reduces trigger jitter by increasing positive feedback at higher frequencies. The setting of R479 determines the circuit hysteresis.

When TV Field is not selected, the TV Trig Enable line connected to R402 and R473 is LO. Transistors Q402 and Q403 are biased off and a LO is placed on one input of U480A by R474. This LO input will cause U480A to invert the output from U480D. With Q403 off, a LO will be placed on one input of U480B by R405 and U480B will also act as an inverter. The A Trigger signal at the output of U480B is therefore the same as the input signal to U480A.

When TV Field is selected, the TV Trig Enable line is HI. The outputs of U480D will determine the conduction states of Q402 and Q403, and the input of U480A connected to R473 will be HI. The output of U480A will be LO and U480B will invert the signal at its other input. Signals at the collector of Q403 are filtered by C408, R405, and C405 to reject TV video information and average the TV horizontal-sync pulses. Setting the trigger-level threshold near the center of the horizontal-sync-pulse swing establishes the untriggered level. When the TV vertical-sync block occurs, the output of the filter applied to U480B pin 7 rises to a level that will cause the Schmitt Trigger circuit to switch. Precise TV field synchronization is obtained as a result of this filtering action. The A Trigger signal output will be the inverse of the filtered signal appearing at U480B pin 7.

A SWEEP GENERATOR AND LOGIC

The A Sweep Generator and Logic circuitry, shown on Diagram 4, produces a linear voltage ramp that is amplified by the Horizontal Amplifier to provide horizontal deflection of the crt beam. The Sweep Generator circuits also produce

signals that are used to generate correct timing of the crt unblanking and intensity levels used for viewing the display. See Figure 3-3 for the block diagram of the A Sweep Generator and Logic circuitry.

The Sweep Logic circuitry controls the holdoff time, starts the sweep upon reception of a trigger signal, and terminates the sweep at the proper sweep level. When using P-P Auto or TV Field triggering, the Sweep Logic circuitry will cause the Sweep Generator to free run, producing a baseline trace if a trigger signal is not received within a pre-determined time period.

A Miller Sweep Generator

The A Miller Sweep Generator produces a linear voltage ramp that drives the Horizontal Amplifier. It produces this ramp by maintaining a constant current through timing capacitors to obtain a linearly increasing voltage.

Field-effect transistors Q704A and Q704B are matched devices with Q704B sourcing current for Q704A. Since the gate and source of Q704B are connected together, the source current of Q704A will be of a magnitude such that there is no voltage drop across its gate-source junction.

When the sweep is not running, Q701 is biased on to hold the timing capacitors in a discharged state. The low impedance of Q701 in the feedback path holds the A Miller Sweep output near ground potential. The voltage across Q701, in addition to the base-emitter voltage of Q706, prevents saturation of the output device.

A sweep ramp is initiated when Q576 is biased off. This will bias off Q701 and the timing capacitors can charge at a rate determined by timing resistors R701 and R702 and the position of A SEC/DIV switch S701. One end of timing resistor R701 is connected to the wiper of R721 and the other end is connected to the input of the Miller integrator. Due to feedback from the circuit output through the timing capacitors, the integrator input voltage remains fixed and establishes a constant voltage across the timing resistors. This constant voltage, which produces a constant current through the timing capacitors, results in a linearly increasing voltage at the output of the A Miller Sweep circuit.

When the output reaches approximately 12 V, the Sweep Logic circuitry will initiate the holdoff period in which Q701 is turned on and the A Sweep Generator is reset. This holdoff period is necessary so that the timing capacitors can be fully discharged before another sweep starts. Capacitors C702 and C703 are always in the charging circuit and are used for high sweep speeds. Capacitor C701A in series with C701B are used for medium sweep speeds, and C701B is used for slow sweep speeds.

The Sec/Div Variable circuitry utilizes an operational amplifier to maintain a constant reference voltage at one end of R721 independent of the circuit load. The voltage applied to the timing resistors varies with the rotational position of R721, the SEC/DIV Variable control. A fixed dc voltage is applied to the noninverting input of the operational amplifier and feedback resistors R717 and R718 establish double that voltage at the anode of VR720.

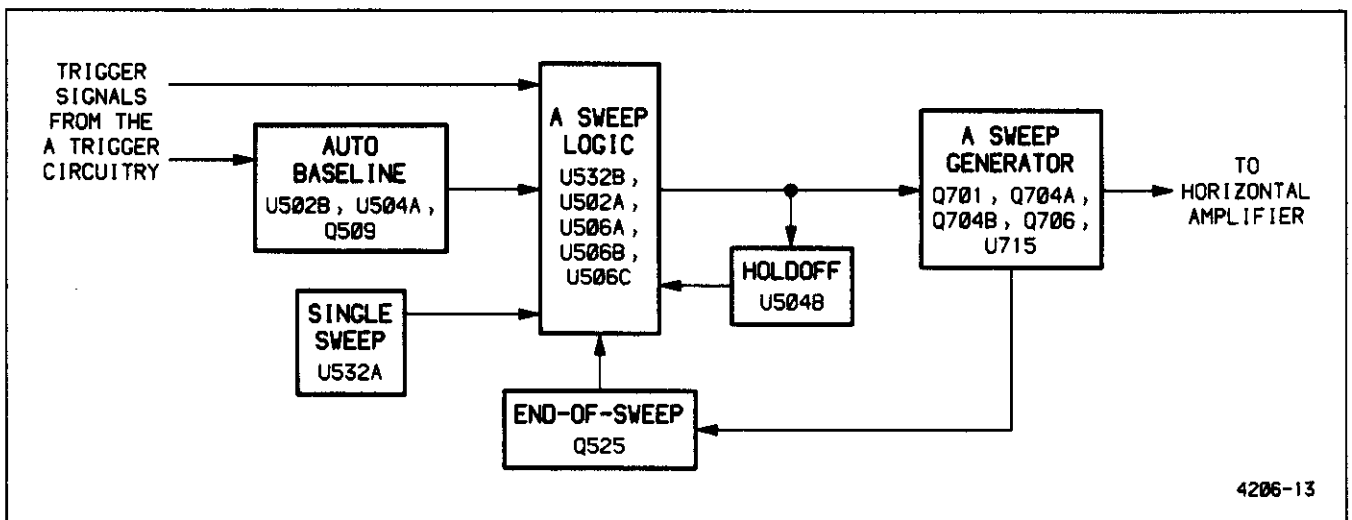


Figure 3-3. Block diagram of the A Sweep Generator and Logic circuitry.

A Sweep Logic

The A Sweep Logic circuitry controls sweep generation, as a function of incoming trigger signals and the A Trigger mode selected.

Incoming trigger signals from the output of U480B will clock U502, a one-shot multivibrator, and cause the Q output to go from LO to HI. If another trigger signal is not received by U502 within a time period determined by the time constant of R503 and C501, the Q output will return LO. Whenever trigger signals are being received, the \bar{Q} output of U502 will bias on Q509 and illuminate TRIG'D LED DS518. The output state of U502 is used in the Auto Baseline circuit as described in the "P-P AUTO and TV FIELD" section.

NORM. When NORM Trigger mode is selected, input pin 12 of U532D is held HI by S401B, causing the gate output to also be HI. The output of U532C will then be LO and U506A will not be held reset. Input pin 4 of U532A is held HI by S401C, causing the output to be LO which places a LO on the D input of U506A. Trigger signals received at the clock input of U506A will then clock this LO to the Q output.

During the previous holdoff period, U506A had been set by U532B so that the \bar{Q} output went LO. This biased on Q576 and the A Miller Sweep was prevented from running. Whenever U506A is clocked following holdoff by a trigger signal, the LO on the D input will be transferred to the Q output and the \bar{Q} output will go HI. This will bias off Q576 and the A Miller Sweep will generate the sweep ramp as described in the "A Miller Sweep Generator" section. When the ramp voltage is about 12 V, Q525 will be biased on. The output of U532B will change from LO to HI, setting U506A and biasing on Q576. With Q576 conducting, holdoff one-shot U504B will be triggered and the A Miller Sweep Generator will be reset to turn off Q525.

With U504B triggered, the \bar{Q} output changes from HI to LO and will stay LO for a time duration determined by the Var Holdoff circuitry and the A SEC/DIV switch position. VAR HOLDOFF potentiometer R9521 determines the amount of charging current available to charge C518, C519 or C520 at pin 15 to the threshold voltage level on pin 14. During the time the \bar{Q} output is LO, the set input of U506A is held HI so that no trigger pulses can initiate a new sweep. When pin 15 of U504B reaches the threshold voltage on pin 14, the \bar{Q} output goes HI to end the holdoff period and release U506A from the set condition. The circuit is then enabled to generate another sweep once a trigger signal is again applied to the clock input of U506A.

P-P AUTO and TV FIELD. When P-P Auto or TV Field is selected, the Auto Baseline configuration is enabled. Pin 12

of U532D is held LO by R569 and the output will follow the signal provided by the Q output of U502. If trigger signals are being received by U502, the output of U532D will be HI and cause the output of U532C to be LO. Flip-flop U506A will respond to trigger signals as described in the "NORM" section. If trigger signals are not being received by U502, the output of U532D will be LO. The output of U532C will then be the inverse of the input signal applied to pin 11 so that U506A will be reset when holdoff ends, causing a sweep to be generated. With no new trigger pulses being applied to the circuitry, U506A will be continuously set and then reset in this manner to generate sweeps.

SGL SWP. In the Sgl Swp mode, both the P-P AUTO and NORM buttons are out. This results in a LO at the output of U532C so that U506A is not held reset. A LO is also on input pin 4 of U532A.

During the previous holdoff period, U532B had reset U506B to cause the Q output to be LO. The D input of U506A will therefore be HI and clock signals to the gate will keep the \bar{Q} output LO and the sweep disabled. When the SGL SWP button is pushed in, the \bar{Q} output of U504A will go LO for a time period determined by the time constant of R504 and C504 and then return HI. This HI will then clock through the HI on the D input of U506B to the Q output. Consequently the output of U532A will go LO and CR514 will be reverse biased to bias on Q511 and light the READY LED. The next trigger pulse applied to the clock input of U506A will then initiate a sweep as described previously. At the end of the sweep, U506B will again be reset, causing the TRIG'D LED to go out and place a HI on the D input of U506A. A new sweep will not be initiated until the SGL SWP button is again pushed.

X-Y. In the X-Y mode of operation, the $\bar{X}\bar{Y}$ line is LO which holds the input of U532B LO through CR518. The output of U532B will hold U506A set and no sweeps can be initiated.

ALTERNATE B SWEEP

The Alternate B Sweep circuitry, shown on Diagram 5, produces a linear voltage ramp that is amplified by the Horizontal Amplifier to provide the B Sweep horizontal deflection on the crt. The Alternate B Sweep circuitry also produces the sweep-switching signals that control the display of the A and B Sweeps, and the gate signals used by the Intensity and Z-Axis circuits to establish the crt unblanking and intensity levels needed for producing both the A Intensified and B Sweep displays.

The B Sweep ramp is enabled by the B Sweep Logic circuit either immediately after the end of the established

delay time (Runs After Delay) or upon receipt of the first trigger signal after the delay time has elapsed. This delay time is a function of the B Delay Time Position Comparator circuit and the A sweep.

B Miller Sweep Generator

The B Miller Sweep Generator is composed of Q709, Q710A, Q710B, Q712, and associated timing components. This circuit produces the B Sweep and functions in the same manner as the A Miller Sweep Generator; see the "A Miller Sweep Generator" section for a description of circuitry operation. The output at the collector of Q712 drives the Horizontal Amplifier and Q643.

B Trigger Level Comparator

The B Trigger Level Comparator is composed of transistor array U605, U625C, Q619, and Q620. This circuit determines both the trigger level and slope at which the B triggering signal is produced. It functions in the same manner as the A Trigger Level Comparator with the exclusion of the TV Trigger and Trigger View circuitry. See the "A Trigger Level Comparator" section for a description of the circuit operation. Buffering of the inverting and noninverting outputs of U625D is provided by U625A and U625B, and Q630 and Q631 level shift the signals to TTL levels. The circuit output at the collector of Q630 supplies trigger signals to clock U670A.

Runs After Delay

The Runs After Delay circuit allows the B Sweep Logic to generate a B Sweep independently of any B Trigger signals. In the Runs After Delay mode, B TRIGGER LEVEL control R602 is rotated fully clockwise. This biases off Q637 and places a LO on the collector. Inverter U660D will then have a HI output with resistor R640 providing positive feedback. The output of U660A will therefore be LO and U670A will be held set with the \bar{Q} output LO.

If the B TRIGGER LEVEL control is not fully clockwise, Q637 is biased on and the B Sweep is in the triggered mode. The output of U660D will be LO, the output of U660A will be HI, and U670A will no longer be held set.

Operation of the B Sweep Logic circuitry under both of these conditions is described in the "B Sweep Logic" discussion.

B Delay Time Position Comparator

The B Delay Time Position Comparator circuit compares the amplitude of the A Sweep sawtooth output voltage to the dc voltage level set by B DELAY TIME POSITION po-

tentiometer R6440. The output of the comparator is used to initiate a B Sweep and to control the B Z-Axis Logic circuit switching.

The inputs to the comparator, U655, are the wiper voltage of R9644 and the A Sweep voltage from the divider network composed of R651, R652, and R653. Input voltage ranges to the comparator are determined by VR645 and R646 for the noninverting input and by R652 for the inverting input. Delay Start potentiometer R646 is adjusted in conjunction with potentiometer R652 to set the B DELAY TIME POSITION dial calibration.

The output of the comparator is enabled or disabled by the strobe signal connected to pin 6. When the \bar{A} Only signal is HI, the comparator is enabled. When \bar{A} Only is LO, the output of the comparator is a high impedance and therefore a HI is present on pin 9 of U680C.

B Sweep Logic

The B Sweep Logic circuitry utilizes signals from the associated B Sweep circuitry to generate control signals for both the B Miller Sweep and the B Z-Axis Switching Logic circuits.

In the Runs After Delay mode, U660A places a LO on the \bar{S} input of U670A. During the previous holdoff period, U680D pin 13 strobed LO. The output of the flip-flop composed of U680C and U680D went HI and the output of U660F went LO. With both the \bar{S} and \bar{R} inputs of U670A LO, the \bar{Q} output is HI to bias on Q709 and prevent the B Miller Sweep from running. Once the A Sweep voltage at U655 pin 3 exceeds the voltage at pin 2, the comparator output will go LO. The flip-flop composed of U680C and U680D will change output states and cause the \bar{R} input of U670A to be HI. The LO on the \bar{S} input will then cause the \bar{Q} output of U670A to go LO. This will shut off Q709 and the B Miller Sweep Generator will produce a linear ramp. If the ramp voltage reaches about 12 V, sweep-end comparator Q643 will turn on and cause the output of U665D to go HI. The B Miller Sweep Generator will continue to run, but the trace will be blanked because the \bar{B} Gate line is HI which reverse biases CR817. Once the ramp is at approximately 13 V, VR712 will conduct and prevent the voltage from increasing further.

The B Sweep Generator will be reset for another sweep by one of two means. If the A Sweep doesn't end before the B Sweep, the Generator will not be reset until the Alt Sync line goes from HI to LO to change the U680C-U680D flip-flop output states. The \bar{R} input of U670A will then be LO, causing the \bar{Q} output to be HI and reset the Generator. Depending on the settings of the A and B SEC/DIV switches, the A Sweep may end before the B Sweep. If this occurs, the Alt

Sync line will go LO at the end of the A Sweep and cause an immediate resetting of the Generator. In either case, a new sweep will be initiated the next time the A Sweep voltage at U655 pin 3 exceeds the voltage at pin 2.

When not in the Runs After Delay mode, the output of U660A is HI and U670A has a HI on both the \bar{S} and D inputs. The circuitry connected to the \bar{R} input of U670A functions as described above. When the output of U660F goes HI, U670A is no longer held reset and the first B trigger signal from the collector of Q630 will clock through the HI on the D input. The \bar{Q} output of U670A will then go LO and a B Sweep will be initiated.

Alternate Display Switching Logic

The Alternate Display Switching Logic circuitry controls both the Horizontal Amplifier sweep switching and the B Z-Axis Logic switching.

HORIZONTAL MODE switch S648 selects the input logic levels that are applied to the circuitry. In the A Horizontal Mode, the \bar{S} input of U670B is LO and the \bar{R} input is HI. This holds U670B set and allows only the A Sweep to be passed to the Horizontal Amplifier. In the B Horizontal mode, the set input of U670B is HI and the reset input is LO to hold U670B reset and allow only the B Sweep to reach the Horizontal Amplifier.

With S648 set to ALT, and for all settings of the VERTICAL MODE switches except BOTH-ALT, the \bar{V}_{alt} signal applied to U660E and the \bar{S} and \bar{R} inputs of U670B are all HI. The LO output of U660E causes the output of U680B to be HI, and whenever the Alt Sync signal applied to pin 1 goes LO, the gate output will change from LO to HI and clock U670B. The outputs of U670B will therefore toggle with each Alt Sync signal transition to alternately enable the A and B Sweeps to reach the Horizontal Amplifier. Whenever the B Sweep is selected for the Horizontal Amplifier, the \bar{Q} output of U670B will be HI. This HI is applied to U665C pin 9, and since pin 10 is also HI, the \bar{S}_{ep} signal from U665C will be LO to enable the A/B Sweep Separation circuitry.

When the CH 1-BOTH-CH 2 VERTICAL MODE switch is set to BOTH, the ADD-ALT-CHOP switch becomes functional. In the ALT VERTICAL MODE position, the \bar{V}_{alt} signal is LO, the Halt signal is HI, and the CH 1 Selected signal is a TTL square wave that switches states at the end of the A Sweep. Input pin 4 of U680B will be HI and the gate output will be the inverse of the CH 1 Selected signal. This output signal is NANDed with the Alt Sync signal by U680A to clock U670B. Whenever the Alt Sync signal goes LO at the end of a sweep and the Ch 1 Selected signal switches from LO to HI, U670B will be clocked. Since only positive transitions on the clock input will cause the flip-flop to change

output states, two A Sweeps are required to cause the flip-flop output levels to switch. With this switching arrangement, the crt will first display the two A Intensified Sweeps and then the two Alternate B Sweeps.

B Z-Axis Logic

The B Z-Axis Logic circuitry switches signal current levels to drive the Z-Axis Amplifier for both the B and the A Intensified Sweep displays. The current supplied is summed with the other signal inputs on the Z-Drive line.

When the HORIZONTAL MODE switch is in the ALT position, pin 5 of U665B is HI. The outputs of U670B and the \bar{B} Gate signal from the output of U665D together with the IN TENSITY controls determine the intensity of the A and B Sweeps.

When the A Sweep is displayed, the Q output of U670B is HI and the \bar{Q} output is LO. These output levels will bias on Q680 and bias off Q685. The emitter voltage of Q680 will reverse bias CR817 to prevent Z-Axis drive current from flowing through the diode. With Q685 off, additional Z-Axis drive current to intensify the A Sweep will be supplied whenever CR685 is biased off. Since input pin 5 of U665B is HI, the gate output and therefore the conduction state of CR685 is determined by U665B pin 4. Whenever the B Sweep is running, the output of U665D will be LO. This will cause the output of U665B to also be LO and CR685 will be biased off. If the B Sweep is not running, the output of U665B will be HI and CR685 will be biased on. This will bias off CR816 and the A Sweep will not be intensified.

If the outputs of U670B are set to display the B Sweep (Q LO and \bar{Q} HI), Q680 will be biased off and Q685 will be biased on. The emitter voltage of Q685 will reverse bias CR816 to prevent Z-Axis drive current from flowing through the diode. With Q680 off, the B Sweep will be displayed if CR680 is reverse biased. Whenever the B Sweep is running, the output of U665D is LO. Diode CR680 will then be reverse biased and Z-Axis drive current will flow through CR817. If the B Sweep is not running, the output of U665D is HI, forward biasing CR680 and therefore reverse biasing CR817. No Z-Axis drive current can then flow through CR817.

HORIZONTAL

The Horizontal Amplifier circuit, shown on Diagram 6, provides the output signals that drive the horizontal crt deflection plates. Signals applied to the Horizontal Pre-amplifier can come from either the A or the B Miller Sweep Generator (for sweep deflection) or from the XY Amplifier (when X-Y display mode is selected). Sweep switching is under control

Theory of Operation—2235 Service

of the Alternate Display Switching Logic circuit. See Figure 3-4 for the block diagram of the Horizontal Amplifier.

The Horizontal POSITION control, X10 Magnifier circuitry, and the horizontal portion of the Beam Find circuitry are also contained in the Horizontal Amplifier circuit.

Horizontal Preamplifier

The Horizontal Preamplifier selects display modes and amplifies input signals for application to the Horizontal Output Amplifier.

The A and B Sweeps, selected by U670B in the Alternate Sweep circuitry, are applied to the emitters of Q742 and Q732 respectively through gain potentiometers R740 and R730. The transistors are biased into the active or cutoff regions by the control voltage applied at the cathodes of CR732 and CR742. Switching between the A and B Sweeps occurs within U760, with a negative input at pin 10 or 9 disconnecting the respective sweep from the rest of the amplifier. The Horizontal POSITION control adjusts the crt trace position through pin 14. Output bias current levels are set by R751 at pin 5 and frequency compensation for X-Axis signals is provided by C751 connected to pin 13.

Horizontal X10 Gain is set by the resistor network connected between pins 3 and 6. When the X10 Magnifier is on, S721 is closed and the timing adjustment is made using R754. Magnifier registration is adjusted by R749 so that there is no horizontal trace shift when switching between the X10 Magnifier on and off positions.

X-Y Amplifier

The X-Y Amplifier amplifies the Channel 1 signal from the Internal Trigger circuitry for application to the Horizontal Preamplifier.

When the X-Y mode is selected, Q737 is biased on to establish a HI on U760 pin 12 so that the A and B Sweeps are disconnected from the Preamplifier outputs. The \overline{XY} signal line will be LO and Q756 will be biased off to enable the X-Axis signal to drive the noninverting input of U758. The output of U758 will then be a function of the X-Axis signal and the Horizontal POSITION control wiper voltage. The X-Axis signal gain is adjusted by R760 and the input voltage from the Horizontal POSITION control at pin 14 is disconnected within U760 so that it does not affect the Preamplifier output. The input signal at pin 11 from U758 will be converted to a differential output signal and applied to the Horizontal Output Amplifier.

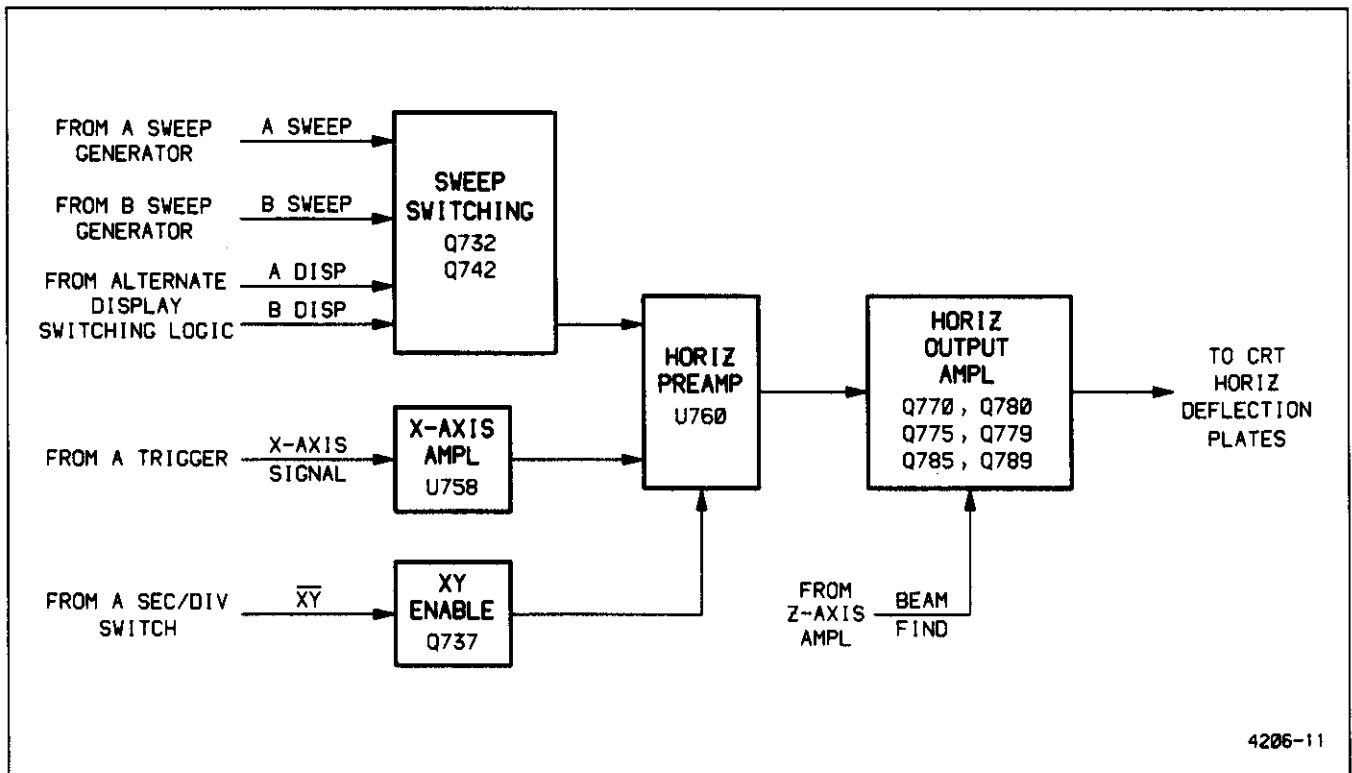


Figure 3-4. Block diagram of the Horizontal Amplifier.

When the X-Y mode is not selected, Q756 is biased on and the X-Axis signal is shunted to ground.

Horizontal Output Amplifier

The Horizontal Output Amplifier provides final amplification of the horizontal signal to drive the horizontal crt deflection plates.

Signals from the (+) and (−) sweep outputs of U760 are used to drive two shunt-feedback amplifiers. Due to the feedback, the input impedance of these amplifiers is low. The base voltages of Q770 and Q780 are at nearly the same dc level due to forward-biased diodes CR765 and CR768 between the two emitters.

Transistors Q770, Q775, and Q779 form a cascode-feedback amplifier for driving the right crt horizontal deflection plate with R775 setting amplifier gain and C775 providing high-frequency compensation. For low-speed signals, Q779 serves as a current source for Q775, and at high sweep rates, the ramp is coupled through C779 to the emitter of Q779. This provides additional pull-up output current to drive the crt at high sweep rates. The amplifier consisting of Q780, Q785, and Q789 drives the left crt horizontal deflection plate in the same manner as described above with zener diode VR782 level shifting the collector signal of Q780.

The BEAM FIND function is implemented when S390 is pushed in to disconnect the cathode of CR764 from the −8.6 V supply. The voltage on the cathode of VR764 goes positive, causing CR780 and CR770 to be forward biased. Current from R764 causes the output common-mode voltage of the two shunt-feedback amplifiers to be shifted negative to reduce the available voltage swing at the crt plates. This prevents the trace from being deflected off-screen horizontally.

Z-AXIS AMPLIFIER

The Z-Axis Amplifier, shown on Diagram 7, controls the crt intensity level via several input-signal sources. The effect of these input signals is either to increase or decrease trace intensity or to completely blank portions of the display. The Z-Drive signal current as determined by the A and B Z-Axis Switching Logic and the input current from the EXT Z AXIS INPUT connector (if in use) are summed at the emitter of common-base amplifier Q825 and thereby determine the collector current of the stage. This transistor provides a low-impedance termination for the input signals and isolates the signal sources from following stages of the Z-Axis Amplifier.

Common-base transistor Q829 establishes a constant current through R832. This current is divided between Q825

and Q829 with the portion through Q829 driving the shunt-feedback output amplifier consisting of Q835, Q840, and Q845. The bias level of Q825 therefore determines the amount of emitter current available to Q829. Feedback-resistor R841 establishes the transresistance gain which converts the input current to output voltage. Emitter-follower Q835 is dc coupled to Q840, and for low-speed signals Q845 acts as a current source. Fast transitions couple through C845, providing additional current gain through Q845 for fast voltage swings at the output of the Amplifier.

External Z-Axis input voltages establish proportional input currents through R822 and R823, and Amplifier sensitivity is determined by the transresistance gain of the shunt-feedback amplifier. Diode CR823 protects the Z-Axis Amplifier if excessive signal levels are applied to the EXT Z AXIS INPUT connector.

The intensity of the crt display in the A, B, and Alt Horizontal modes is determined by the INTENSITY controls and associated circuitry. The A INTENSITY potentiometer controls the base voltage of Q804 to determine the amount of emitter current that will flow through the transistor and therefore the level of the Z-Axis signal. Likewise the B INTENSITY potentiometer will control the base voltage of Q814 and the intensity of the B and Alt Sweep displays.

When only the A Sweep is displayed, Q586 and CR583 are biased off. The current through R818, as set by the A INTENSITY potentiometer, will flow through CR818 and Q825 to fix the voltage level at the Z-Axis Amplifier output. For a B-only display, Q586 is biased on to reverse bias CR818 and prevent A-intensity current from reaching Q825. Current determined by the base voltage of Q814 will flow through CR817 to Q825 and determine the B Sweep intensity. For an alternating A and B display, Q586 will be biased off when the A Sweep is displayed. During the portion of the A Sweep in which the B Sweep runs, current from R816 is allowed to flow through CR816 by the B Z-Axis Logic circuit to provide an intensified zone.

When CHOP VERTICAL MODE is selected, the Chop Blank signal is applied to the collector of Q825 through CR824 during the display-switching time. Signal current is shunted away from CR825, and the forward bias of Q829 increases to the blanking level. When blanked, the output of the Z-Axis Amplifier drops to a level that reduces the crt beam current below viewing intensity during the chop-switching transition.

For an X-Y display, CR818, CR817, and CR816 are reverse biased. The $\bar{X}\bar{Y}$ signal is LO to reverse bias CR551 and allow current in R820 to flow through CR820. The crt intensity is then controlled by the A INTENSITY potentiometer which sets the current in R820 through Q804.

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BEAM FIND switch S390 controls the base bias voltages of Q825 and Q829. When the BEAM FIND button is out, -8.6 V is supplied to a base-biasing network. When the button is pushed in, the -8.6 V supply is removed and the voltage at the anode of VR828 rises to about -5.6 V. This turns off Q829 so that the amplifier output voltage is determined by R835 and the voltage at the BEAM FIND switch, as set by other parts of the Beam Find circuitry. The output voltage of Q835 will then be at a fixed level so that the INTENSITY controls and the Z-Drive signal have no control over the crt intensity. A bright trace or dot will then be displayed.

Dc Restorer

The Dc Restorer circuit produces the crt control-grid bias and couples both dc and ac components of the Z-Axis Amplifier output to the crt control grid. Direct coupling of the Z-Axis Amplifier output to the crt control grid is not employed due to the high potential differences involved. Refer to Figure 3-5 during the following discussion.

Ac drive to the Dc Restorer circuit is obtained from pin 16 of T948. The drive voltage has a peak amplitude of about ± 100 V, a frequency of about 20 kHz, and is coupled into the Dc Restorer circuit through C853 and R853. The cathode of CR851 is biased by the voltage applied from the wiper of Grid Bias potentiometer R851, and the ac-drive

voltage will be clamped whenever the positive peaks reach a level that forward biases CR851.

The Z-Axis Amplifier output voltage, which varies between $+10$ V and $+75$ V, is applied to the Dc Restorer at the anode of CR853. The ac-drive voltage will hold CR853 reverse biased until the voltage falls below the Z-Axis Amplifier output voltage level. At that point, CR853 becomes forward biased and clamps the junction of CR851, CR853, and R854 to the Z-Axis output level. Thus, the ac-drive voltage is clamped at two levels to produce a square-wave signal with a positive dc-offset level.

The Dc Restorer is referenced to the -2 kV crt cathode voltage through R858 and CR854. Initially, both C855 and C854 will charge up to a level determined by the difference between the Z-Axis output voltage and the crt cathode voltage. Capacitor C855 charges from the Z-Axis output through R858, CR854, and CR855, to the crt cathode. Capacitor C854 charges through R858, CR854, R854, and CR853 to the crt cathode.

During the positive transitions of the ac drive, from the lower clamped level toward the higher clamped level, the charge on C854 increases due to the rising voltage. The voltage increase across C854 is equal to the amplitude of the positive transition. The negative transition is coupled

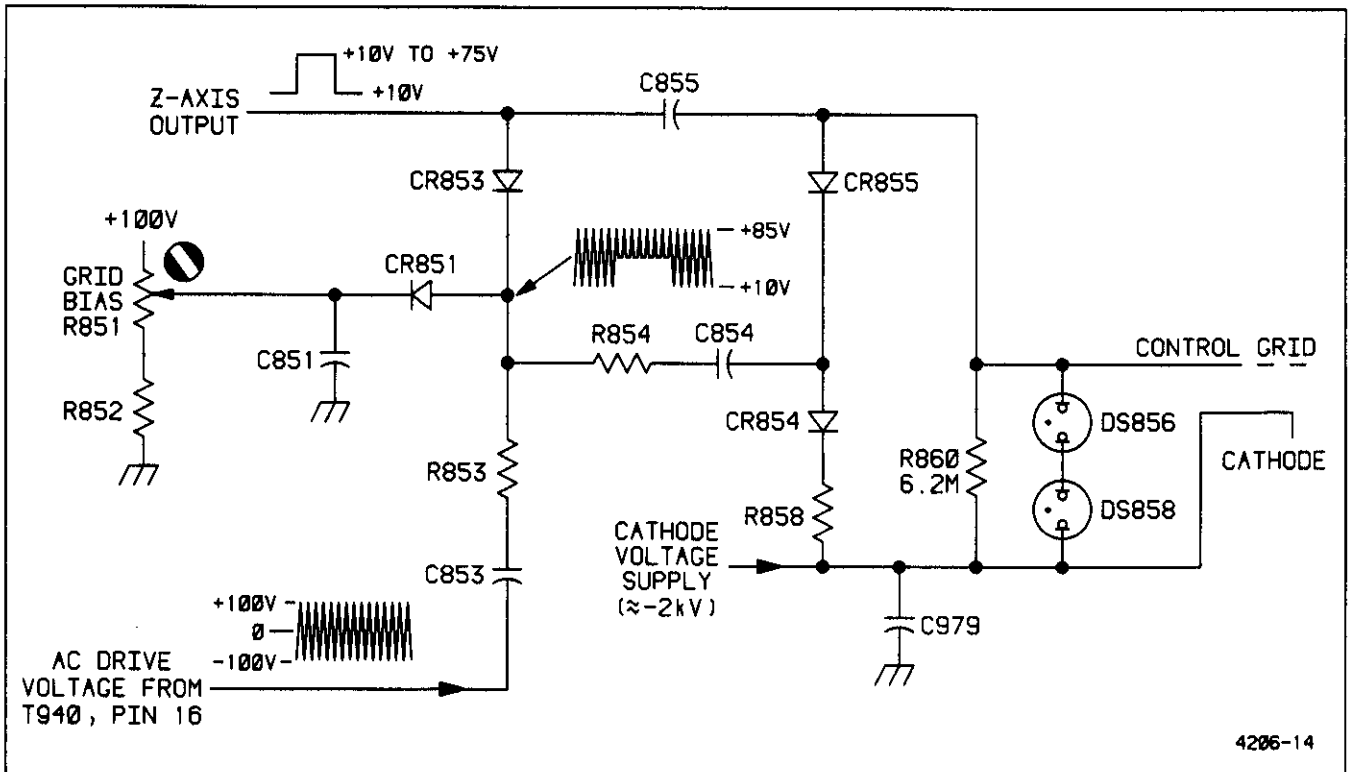


Figure 3-5. Simplified diagram of the Dc Restorer circuit.

through C854 to reverse bias CR854 and to forward bias CR855. The increased charge of C854 is then transferred to C855 as C854 discharges toward the Z-Axis output level. Successive cycles of the ac input to the Dc Restorer will charge C855 to a voltage equal to the initial level plus the amplitude of the clamped square-wave input.

The added charge on C855 determines the control-grid bias voltage. If more charge is added to that already present on C855, the control grid becomes more negative and less crt writing-beam current will flow. Conversely, if less charge is added, the control-grid voltage level will be closer to the cathode-voltage level and more crt writing-beam current flows.

During periods that C854 is charging, the crt control-grid voltage is held constant by the long time-constant discharge path of C855 through R860.

Fast-rise and fast-fall transitions of the Z-Axis output signal are coupled to the crt control grid through C855 to start the crt writing-beam current toward the new intensity level. The Dc Restorer output level then follows the Z-Axis output-voltage level to set the new bias voltage for the crt control grid.

Neon lamps DS858 and DS856 protect the crt from excessive grid-to-cathode voltage if the potential on either the control grid or the cathode is lost for any reason.

POWER SUPPLY AND PROBE ADJUST

The Power Supply circuitry converts the ac power-line voltage into the voltages needed for instrument operation. It consists of the Power Input, Preregulator, and Inverter circuits (which drive the primary of the power transformer) and secondary circuits (which produce the necessary supply voltages for the instrument).

Power Input

The Power Input circuit converts the ac power-line voltage to filtered dc for use by the Preregulator.

POWER switch S901 connects the ac power line through fuse F9001 to the bridge rectifier composed of CR901, CR902, CR903, and CR904. The bridge full-wave rectifies the source voltage, and the output is filtered by C906. Input surge current at the time of instrument power-up is limited by thermistor RT901. The thermistor resistance is moderately high when the power is first turned on, but decreases as the input current warms the device. The instrument is

protected from large voltage transients by suppressor VR901. Conducted interference originating within the power supply is attenuated by common-mode transformer T901, differential-mode transformer T903, line filter FL9001, and capacitors C900, C901, and C902.

Preregulator

The Preregulator provides a regulated dc output voltage for use by the Inverter circuitry.

When the instrument is turned on, the voltage developed across C906 will charge C925 through R926. When the voltage has risen to a level high enough that U930 can reliably drive Q9070, U930 will receive operating supply voltage through Q930. This level is set by zener diode VR925 in the emitter of Q928 and by the voltage divider consisting of R925 and R927. The zener diode will keep Q928 off until the base voltage reaches approximately 6.9 V. Then Q928 will be biased into conduction and the resulting collector current will cause a voltage drop across R929. This voltage drop will bias on Q930, and the positive feedback through R930 will reinforce the turn-on of Q928. Thus Q930 and Q928 will drive each other into saturation very quickly. Once Q930 is on, U930 will begin to function.

Pulse-width modulator U930 controls the output voltage of the Preregulator by regulating the duty cycle of the pulse applied to the gate of Q9070. It utilizes an oscillator with the frequency determined by R919 and C919 (approximately 60 kHz) and with a sawtooth output voltage at pin 5. This sawtooth voltage is compared internally with the output voltage produced by the two error amplifiers. Whenever the sawtooth voltage is greater than the error amplifier output voltage, Q9070 is biased on to supply current to both C940 and the rest of the circuitry. The two error amplifiers maintain a constant output voltage and monitor the output current of the Preregulator. One input of each amplifier is connected through a divider network to the IC internal +5-V reference. The output voltage of the Preregulator is monitored by the voltage divider at pin 2. The voltage drop across R907, produced by the Preregulator output current, is applied to the current limit amplifier at pin 16.

When the instrument is first turned on, the current limit amplifier controls the conduction time of Q9070. While Q9070 is conducting, the output current increases until a sufficiently large voltage drop is developed across R907 to invoke the current-limit mode. The current limit amplifier holds the output current below the current-limit threshold of approximately 1 A. When the voltage across C940 reaches approximately 43 V, the voltage amplifier starts controlling the duty cycle of Q9070 and the Preregulator will not limit current unless there is excessive current demand.

With Q9070 off, C907 charges to the output voltage of the Power Input circuit. When Q9070 turns on, current through the FET will come from the winding connected to pins 1 and 2 of T906 and from C907. Current to C907 is supplied by the winding connected to pins 4 and 5 of T906. When U930 shuts off Q9070, the collapsing magnetic field will raise the voltage at the anode of CR907. This diode then becomes forward biased and passes the currents supplied by C907 and the winding connected to pins 4 and 5 of T906. For this part of the cycle, current to C907 will be supplied by the winding connected to pins 1 and 2 of T906. This process will continue for each period of the oscillator, and the duty cycle controlling the conduction period of Q9070 will be altered as necessary to maintain 43 V across C940. To shut off Q9070 during each oscillator period, Q908 is used to discharge the gate-drain capacitance. Pin 10 of U930 goes LO, reverse biasing CR908 and turning on Q908 to shut off the FET.

Once the supply is running, power to U930 will be supplied from the winding connected to pins 6 and 7 of T906. Diode CR920 half-wave rectifies the voltage across pins 6 and 7 to keep filter capacitor C925 charged and to maintain supply voltage to U930 through Q930.

Instrument protection from excessive output voltage is supplied by silicon-controlled rectifier Q935. Should the Preregulator output voltage exceed 51 V, zener diode VR935 will conduct, causing Q935 to also conduct. The Preregulator output current will then be shunted through Q935, and the output voltage will very quickly go to zero. With the supply voltage of U930 no longer being provided by the winding connected to pins 6 and 7 of T906, the Preregulator will shut down and Q935 will be reset. The supply will then attempt to power up, but may again shut down if the overvoltage condition is again reached. This sequence continues until the overvoltage condition is corrected.

Inverter

The Inverter circuit changes the dc voltage from the Preregulator to ac for use by the supplies that are connected to the secondaries of T948.

The output of the Preregulator circuit is applied to the center tap of T948. Power-switching transistors Q946 and Q947 alternate conducting current from the Preregulator output through the primary windings of T948. The transistor switching action is controlled by T944, a saturating base-drive transformer.

When the instrument is first turned on, one of the switching transistors will start to conduct and its collector voltage will drop toward the common voltage level. This will induce a

positive voltage from the lead of T944 which is connected to the base of the conducting transistor and reinforce conduction. Eventually T944 will saturate, and as the voltage across T944 (and T948) begins to reverse, the conducting transistor will cut off because of the drop in base drive. The other transistor will not start conduction until the voltage on the leads of T944 reverse enough to bias it on. This process will continue, and the saturation time of T944 plus the transistor-switching time will determine the frequency of inverter operation (typically 20 kHz). After the initial inverter start up, the switching transistors do not saturate; they remain in the active region during switching.

Diodes CR946 and CR947 serve as a negative-peak detector to generate a voltage for controlling the output of the error amplifier. Capacitor C943 charges to a voltage equal to the negative peak voltage at the collectors of Q946 and Q947, referenced to the Preregulator input voltage. This voltage level is applied to the divider composed of R937, R938, and R939. The error amplifier, composed of Q938 and Q939, is a differential amplifier that compares the reference voltage of VR943 with the voltage on the wiper of potentiometer R938. The current through Q939 will set the base drive of Q944 and thereby control the voltage on C944. This voltage will bias Q946 and Q947 to a level that will maintain the peak-to-peak input voltage of T948. The amplitude of the voltage across the transformer primary winding, and thus that of the secondary voltages of T948, is set by adjusting -8.6 V Adj potentiometer R938.

At turn on, Q938 is biased off and Q939 is biased on. All the current of the error amplifier will then go through Q939 to bias on Q944. Diode CR945 allows the base of Q944 to go positive enough to initially turn on Q946 or Q947. The current through Q944 controls the base drive for Q946 and Q947. Base current provided by base-drive transformer T944 will charge C944 negative with respect to the inverter circuit floating ground (common) level.

Crt Supply

High-voltage multiplier U975 utilizes the 2-kV winding of T948 to generate 12 kV to drive the crt anode. It also uses an internal half-wave rectifier diode to produce -2 kV for the crt cathode. The -2 kV supply is filtered by a low-pass filter composed of C975, C976, R976, R978, and C979. Neon lamp DS870 protects against excessive voltage between the crt heater and crt cathode by conducting if the voltage exceeds approximately 75 V.

Focus Circuit

Focus voltage is also developed from the -2 kV supply via a voltage divider composed of R894, R892, FOCUS potentiometer R893, R891, R890, R889, R888, and Q885. The focus voltage tracks the A-intensity level through the action

of Q885. The emitter voltage of Q804, set by the A INTENSITY control, is applied to the emitter of Q885 through R885. When the emitter voltage of Q804 changes, the current through Q885 changes proportionally and alters the voltage at one end of FOCUS control R893.

Low-Voltage Supplies

The low-voltage supplies utilize center-tapped secondary windings of T948. The +100 V supply uses CR954 and CR955 for rectification and C954 for filtering. Diodes CR956 and CR957 rectify ac from taps on the 100 V winding, and C956 filters the output to produce +30 V dc. The diode bridge consisting of CR960, CR961, CR962, and CR963 produces the +8.6 V and -8.6 V supplies. Filtering of the +8.6 V is accomplished by C960, C962, and L960; filtering of the -8.6 V is done by C961, C963, and L961. The +5.2

V supply is produced by CR967, CR970, C968, R971, and C970.

Probe Adjust

The Probe Adjust circuitry, shown on diagram 6, utilizes a square-wave generator and a diode switching network to produce a negative-going square-wave signal at PROBE ADJUST connector J9900. Amplifier U985 is configured as a multivibrator with the time constant of R987 and C987 determining the oscillation period. When the output of the multivibrator is at the positive supply voltage, CR988 is forward biased. This reverse biases CR989 and the PROBE ADJUST connector signal is held at ground potential by R990. When the multivibrator output switches states and is at the negative supply voltage, CR988 is reverse biased. Diode CR989 will now be forward biased and the circuit output signal be approximately -0.5 V.