THEORY OF OPERATION

INTRODUCTION

SECTION ORGANIZATION

This section contains a functional description of the 2465 Oscilloscope circuitry. The discussion begins with an overview of the instrument functions and continues with detailed explanations of each major circuit. Reference is made to supporting schematic and block diagrams which will facilitate understanding of the text. These diagrams show interconnections between parts of the circuitry, identify circuit components, list specific component values, and indicate interrelationships with front-panel controls.

The detailed block diagram and the schematic diagrams are located in the tabbed "Diagrams" section at the rear of this manual, while smaller functional diagrams are contained within this section near the associated text. The particular schematic diagram associated with each circuit description is identified in the text, and the diagram number is shown (enclosed within a diamond symbol) on the tab of the appropriate foldout page. For optimum understanding of the circuit being described, refer to both the applicable schematic diagram and the functional block diagram.

HYBRID AND INTEGRATED CIRCUIT DESCRIPTIONS

Digital Logic Conventions

Digital logic circuits perform many functions within this instrument. The operation of these circuits is represented by specific logic symbology and terminology. Most logic-function descriptions contained in this manual use the positive-logic convention. Positive logic is a system of notation whereby the more positive of two levels is the TRUE (or 1) state; the more negative level is the FALSE (or 0) state. In the logic descriptions, the TRUE state is referred to as HI, and the FALSE state is referred to as LO. The specific voltages which constitute a HI or a LO vary between individual devices. For specific device characteristics, refer to the manufacturer's data book.

Hybrids

Some of the circuits in this instrument are implemented in hybrid devices. The hybrids are specialized electronic devices combining thick-film and semiconductor technologies. Passive, thick-film components and active, semiconductor components are interconnected to form the circuit on a ceramic carrier. The end result is a relatively small "building block" with enhanced performance characteristics, all in one package. Hybrid circuits are shown on schematics simply as blocks with inputs and outputs identified. Information about hybrid functioning is contained in the related portion of the Detailed Circuit Description.

Linear Devices

The operation of individual linear integrated circuit devices is described in this section using waveforms or other graphic techniques to illustrate their operation.

BLOCK DIAGRAM

The following discussion is provided as an aid in understanding overall operation of the 2465 Oscilloscope circuitry before the individual circuits are discussed in detail. A simplified block diagram of the 2465 Oscilloscope, showing basic interconnections, is shown in Figure 3-1. The diamond-enclosed numbers in each block refer to the schematic diagram(s) at the rear of this manual in which the related circuitry is located.

BLOCK DESCRIPTION

The Low Voltage Power Supply is a high-efficiency, switching supply with active output regulation that transforms the ac source voltage to the various dc voltages required by the 2465. The High Voltage Power Supply circuit develops the high accelerating potentials required by the crt, using voltage multiplication techniques, and the DC Restorer provides interfacing for the low-potential intensity signals from the Z-Axis Amplifier to the crt control grid.

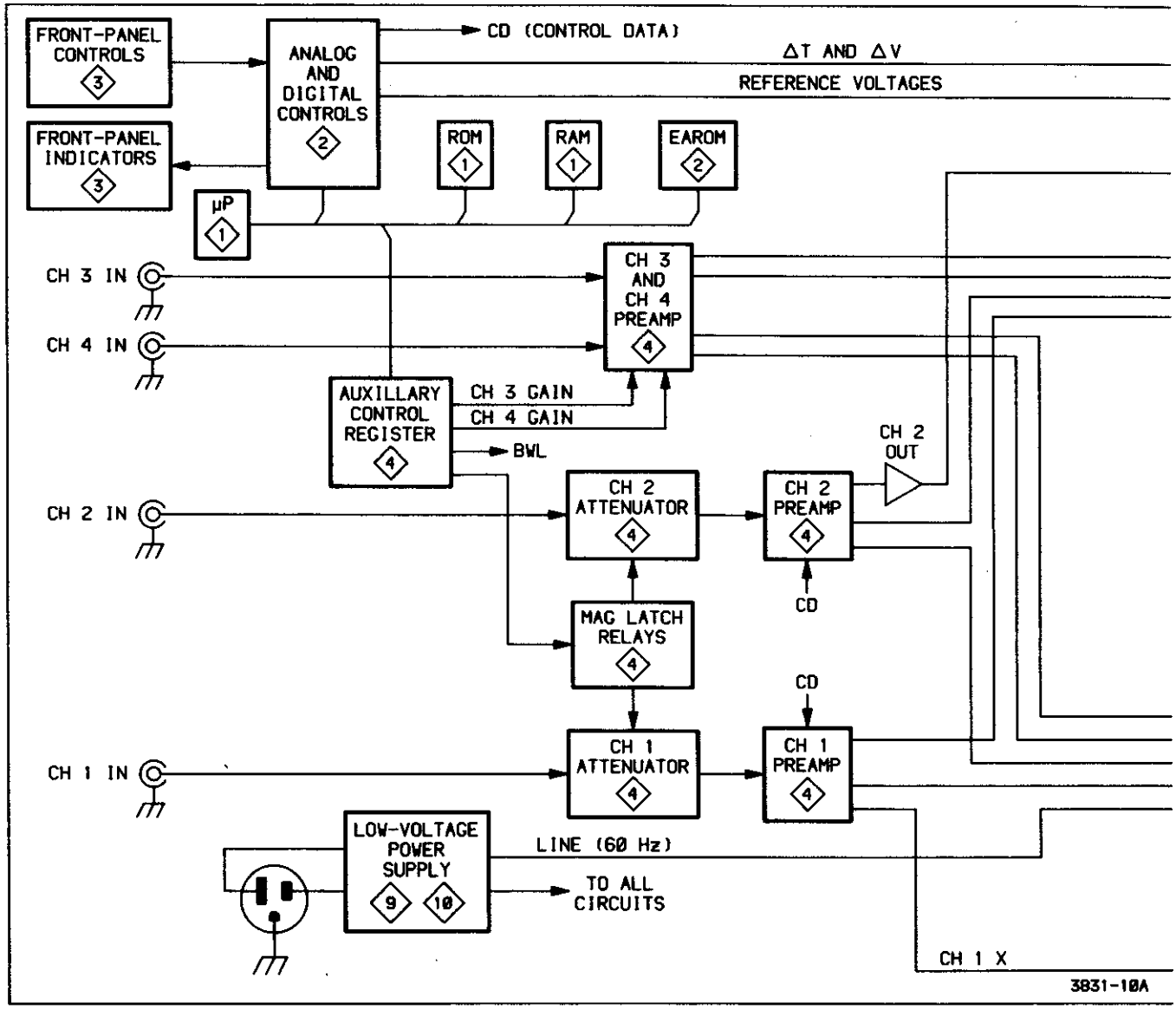

Figure 3-1. Block diagram.

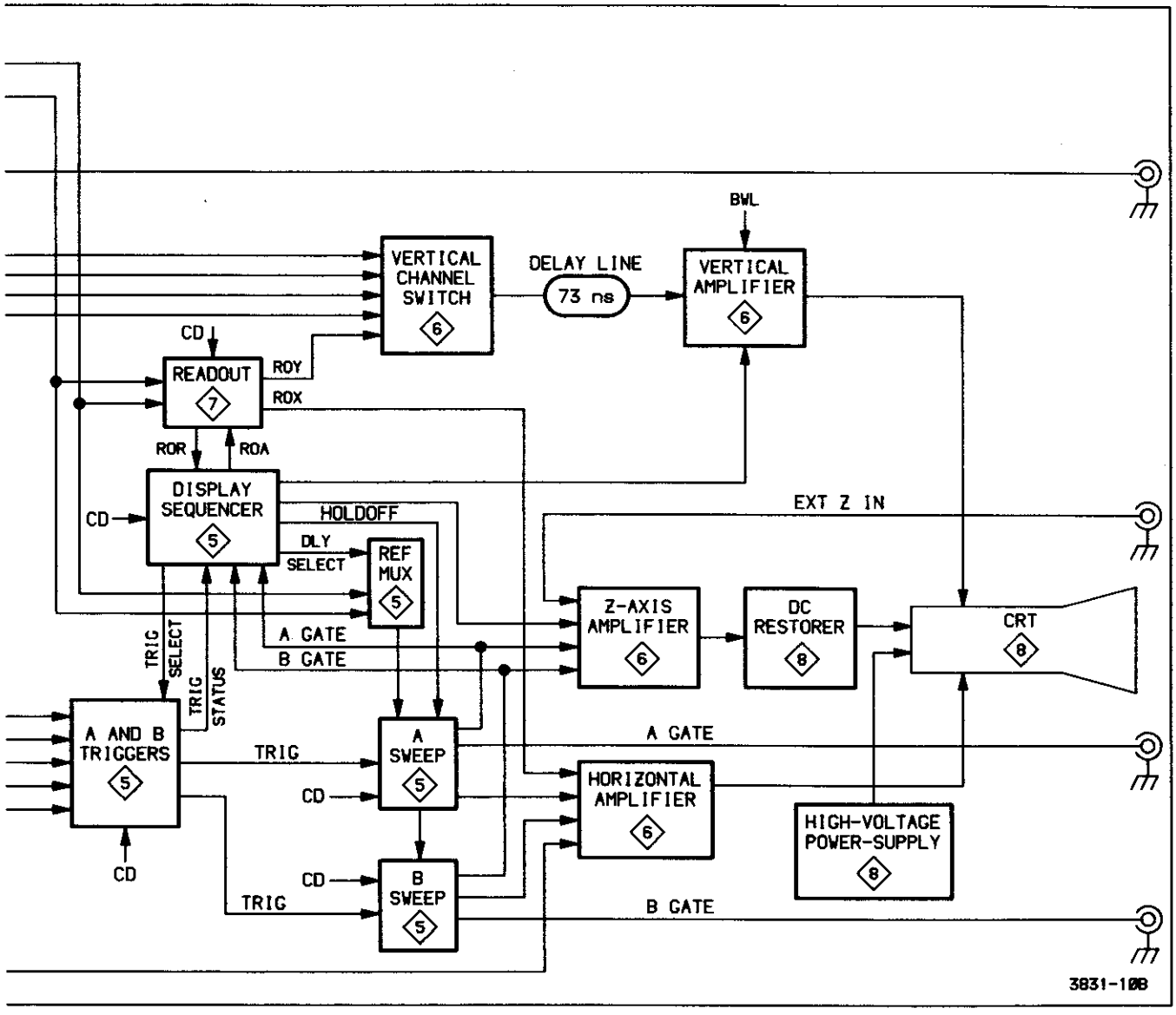

Figure 3-1. Block diagram (cont).

Most of the activities of the 2465 are directed by a Microprocessor. The Microprocessor, under firmware control (firmware is the programmed instructions contained in read-only memory that tells the processor how to operate), monitors instrument functions and sets up the operating modes according to the instructions received.

Various types of data to and from the Microprocessor (program instructions, constants, control data, etc.) are transferred over a group of eight bidirectional signal lines called the Data Bus. The Data Bus is dedicated solely to Microprocessor-related data transfer.

Another group of signal lines, called the Address Bus, are responsible for selecting or "addressing" the memory location or device that the Microprocessor wants to communicate with. Typically, depending on the instruction being executed, the processor places an address on the Address Bus to identify the location the Microprocessor must communicate with. This address, along with some enabling logic, opens up an appropriate data path via the Data Bus; and data is then either read from or written to that location by the processor.

While executing the control program, the Microprocessor retrieves previously stored calibration constants and front-panel settings and, as necessary, places program-generated data in temporary storage for later use. The EAROM (electrically-alterable read-only memory) and RAM (random-access memory) provide these storage functions respectively.

When power is applied to the 2465, a brief initialization sequence is performed, and then the processor begins scanning the front-panel controls. The switch settings detected and the retrieved front-panel data from the EAROM causes the processor to set various control registers and control voltages within the instrument that define the operating mode of the instrument. These register settings and voltage levels control the vertical channel selection and deflection factors, the sweep rate, the triggering parameters, the readout activity, and sequencing of the display. Loading the control data into the various registers throughout the instrument is done using a common serial data line (CD). Individual control clock signals (CC) determine which register is loaded from the common data line.

Coordination of the vertical, horizontal, and Z-Axis (intensity) components of the display most be done in real time. Due to the speed of these display changes and the precise timing relationships that must be maintained between display events, direct sequencing of the display is beyond the capabilities of the processor. Instead, control data from the processor is sent to the Display Sequencer (a specialized integrated circuit) which responds by setting up the various signals that control the stages handling the real-time display signals. The controlled stages are stepped through a predefined sequence that is determined by the control data. Typically, as the sequence is being executed, the Display Sequencer will be changing vertical signal sources, Z-Axis intensity levels, triggering sources, and horizontal sweep signal sources. The specific activities being carried out by the Display Sequencer depend on the display mode called for by the control data.

Vertical deflection for crt displays comes from one or more of the four front-panel vertical inputs and, when displaying readout information, from the Readout circuitry. Signals applied to the front-panel Channel 1 and Channel 2 inputs are connected to their respective Preamplifiers via processor-controlled Attenuator networks. Control data from the Microprocessor defining the attenuation factor selected for each channel is serially loaded into the Auxiliary Control Register and then strobed into the Attenuator Mag-Latch Relays in parallel. The relay switches of each Attenuator network are either opened or closed, depending on the data supplied to the Mag-Latch Relay Drivers. The relays are magnetically latched and remain as set until new control data is strobed in. The Auxiliary Control Register is therefore available, and different mode data is clocked into the register to set up the operating mode of other portions of the instrument.

Attenuated Channel 1 and Channel 2 input signals are amplified by their respective Preamplifiers. The gain factor for the Channel 1 and Channel 2 Preamplifiers is settable by control data from the processor. The Channel 3 and Channel 4 input signals are amplified by their respective Preamplifiers by either of a choice of two gain factors set by control bits from the Auxiliary Control Register. All four of these preamplified signals are applied to the Vertical Channel Switch where they are selected by the Display Sequencer for display when required.

Each of the vertical signals is also applied to the A and B Trigger circuitry via trigger pickoff outputs from the Preamplifier stages. Any one of the signals may be selected as the trigger SOURCE for either the A or the B Trigger circuitry as directed by the Display Sequencer. The line trigger signal provides an added trigger source for A Sweeps only. Control data from the Microprocessor is written to the Trigger circuitry to define the triggering LEVEL, SLOPE, and COUPLING criteria. When the selected trigger signal meets these requirements, a sweep can be initiated. The Trigger circuit initiates both the A Sweep and the B Sweep as required by the display mode selected.

In the case of A Sweeps, the LO state of the trigger holdoff (THO) signal from the Display Sequencer enables the A Sweep circuit and the next A Trigger signal initiates

the sweep. For B Sweeps, and in the case of intensified sweeps, the A Sweep Delay Gate signal ($\overline{DG}$) enables the B Sweep circuit. Depending on the B Trigger mode selected, a B Sweep will be initiated either immediately (RUN AFT DLY) or on the next B Trigger signal (TRIG AFT DLY). The slope of the sweep ramp is dependent on Microprocessor-generated control data loaded into the internal control register of the A and B Sweep circuit hybrids.

Sweep signals generated by each of the Sweep hybrids are applied to the Horizontal Amplifier. The Horizontal Amplifier is directed by the Display Sequencer to select one of the sweep ramps for amplification in sequence. In the case of Readout and X-Y displays, the X-Readout and CH 1 input signals are selected to be amplified, also under direction of the Display Sequencer.

To control the display intensity, the Display Sequencer directs the Z-Axis circuit to unblank the display at the appropriate time for the sweeps and readout displays. When the display is unblanked, the Display Sequencer selects the display intensity for either waveform displays or for readout displays by switching control of the Z-Axis beam current between the front-panel INTENSITY and READOUT INTENSITY potentiometers as appropriate.

During readout displays, the vertical dot-position signal from the Readout circuitry is applied to the Vertical Amplifier via the Vertical Channel Switch. Horizontal dot-position deflection for the readout display is selected by internal switching in the Horizontal Amplifier.

The vertical, horizontal, and Z-Axis signals are applied to their respective amplifiers where they are raised to crt-drive levels. The output signals from the Vertical and Horizontal Amplifiers are applied directly to the crt deflection plates. The Z-Axis Amplifier output signal requires interfacing to the high-potential crt environment before application to the crt control grid. The necessary Z-Axis interfacing is provided by the DC Restorer circuit located on the High-Voltage circuit board. The resulting display may be of waveforms, alphanumeric readout, or a combination of both.

DETAILED CIRCUIT DESCRIPTION

INTRODUCTION

The following discussion provides detailed information concerning the electrical operation and circuit relationships of the 2465 Oscilloscope. Circuitry unique to the 2465 is described in detail, while circuits common in the electronics industry are not. The descriptions are accompanied by supporting illustrations and tables. Diagrams identified in the text, on which associated circuitry is shown, are located at the rear of this manual in the tabbed foldout pages.

PROCESSOR AND DIGITAL CONTROL

The Processor and Digital Control circuitry (diagram 1) directs the operation of most oscilloscope functions by following fimware control instructions stored in memory. These instructions direct the Microprocessor to monitor the front-panel controls and to send control signals that set up the various signal processing circuits accordingly.

Microprocessor

The Microprocessor (U2092) is the center of control activities. It has an eight-bit, bidirectional data bus for data transfer (D0 through D7) and a 16-bit address bus (A0 through A15) for selecting the source or destination of the data. Precise timing of instruction execution, addressing, and data transfer is provided by an external, crystal-controlled clock signal.

The clock signal is developed by the Microprocessor Clock stage and applied to the Microprocessor at pin 39. Using the external clock as a reference, the Microprocessor generates synchronized control output signals [R/$\overline{W}$ (read-write), E (enable), and VMA (valid memory address)] that maintain proper timing relationships throughout the instrument.

Microprocessor Clock

The Microprocessor Clock stage generates a 5-MHz square-wave clock signal to the Microprocessor and a 10-MHz clock signal to portions of the Readout circuitry. Inverter U2556A acts as an oscillator with crystal Y2568 providing feedback at the resonant frequency. The required phase shift for oscillation to occur is produced by C2565, C2566, R2564, and the crystal. The RC network composed of R2571, C2572, R2553, and R2573 biases input pin 1 of U2556A in the active region and establishes approximate

symmetry of the oscillator output. The signal is buffered and inverted by U2556B to provide the 10-MHz clock signal.

Flip-flop U2468A is a divide-by-two circuit that reduces the 10-MHz clock down to a 5-MHz square-wave signal used to clock the Microprocessor and the Display Sequencer. The 10-MHz clock is supplied to the Readout Board for dot timing and is also available for use with option circuitry.

Reset Control

The Reset Control circuitry ensures that, at power-up, the Microprocessor begins program execution from a known point in memory and with all the processor registers in known states. It also allows the processor to reset itself when power is turned off so that the instrument powers down in a known state.

POWER-UP SEQUENCE. Operational amplifier U2435 is configured as a comparator that generates the power-up reset. As power is applied to the instrument, the various power supplies start turning on and pull the noninverting input of U2435C (pin 10) above the inverting input level (pin 9). This action forces output pin 8 HI, and the reference level for the comparator at pin 10 is set to +3.7 volts by the divider network of R2648, R2646, and R2647. The HI from U2435C pin 8 is inverted by U2656A and applied to the processor $\overline{\text{RESET}}$ input (pin 40). When all the power supplies are operating, the PWR UP signal from J251 pin 12 goes HI, and capacitor C2661 begins charging positive through R2652. The time required for C2661 to charge to the comparator switching threshold is approximately 100 ms. When the voltage across C2661 reaches the +3.7-V reference level, the comparator switches states and pin 8 of U2435C goes LO. The $\overline{\text{RESET}}$ signal to the processor then goes HI to enable normal execution to begin, and the processor is directed to the starting address of the power-up routine, which it then performs.

POWER-DOWN SEQUENCE. When the instrument power switch is turned off, the PWR UP signal from J251 pin 12 immediately goes LO. This LO generates the $\overline{\text{NMI}}$ (non-maskable interrupt) request to the processor on pin 6 which causes the processor to branch to the power-down routine. Under direction of that routine, the processor begins shutting down the instrument in an orderly fashion before the power supply outputs can drop below the operating thresholds. This routine also places the EAROM in standby to prevent loss of data from the EAROM and disconnects the CH 1 and CH 2 50-Ω input terminations to protect them from accidental application of excessive voltage during storage or bench handling.

As the operating voltages are falling, the Reset circuitry must not generate a false $\overline{\text{RESET}}$ signal to the processor. Such a restart when the power supply voltages are outside their normal operating range would produce unpredictable processor operation that could possibly alter the contents of the EAROM. When the processor has completed all the other power-down tasks, it finally sets the PWR DOWN signal HI via U2208 (diagram 2). This signal is applied to inverter U2118A at pin 1. Pin 16 of U2118A goes LO and immediately pulls pin 10 of Reset Comparator U2435C LO to prevent a reset to the processor. This LO also forward biases CR2651, and C2661 begins discharging through CR2651 and R2552 to allow the voltage on pin 9 of the comparator to fall to zero. After about 1 ms, C2661 is fully discharged, and the processor sets the PWR DOWN signal to U2118A LO. The output of inverter U2118A then goes HI, and Reset Comparator U2435C immediately switches state to assert the $\overline{\text{RESET}}$ signal to the processor. The $\overline{\text{RESET}}$ signal is held LO until the power supplies have fully discharged.

For diagnostic purposes, the PWR DOWN reset signal can be disabled. Moving jumper P503 to the DIAG (diagnostic) position prevents C2661 from being discharged. The $\overline{\text{RESET}}$ signal is therefore held HI, and the processor can execute a free-running NOP (no operation) loop without interruption if the PWR DOWN bit is set HI while the Address Bus is incrementing.

Data Bus

Tri-state buffer U2194 is used to buffer the data signals to the Microprocessor from other devices on the bus. When not enabled, the device is switched to its high-impedance state to isolate the processor from the buffered Data Bus. Buffer U2194 is enabled via Read-Write Latch U2468B when the processor reads data from another device on the bus.

When the processor writes data onto the bus, Octal Latch U2294 is enabled by Read-Write Latch U2468B. When the E (enable) signal at pin 11 of U2294 is HI, processor data bits are passed asynchronously through the latch to the buffered Data Bus. When the E signal goes LO, data bits meeting setup times are latched into the device. The latched Q outputs provide the required drive current to the various devices on the bus and ensure that data hold times are met for correct data transfer. When the Read-Write Latch places a HI on pin 1 of U2294, the latch is disabled, and the outputs are switched to their high-impedance state.

Data transfer to and from the processor may be interrupted by removing Diag/Norm Jumper P503. This forces a NOP (no operation) condition that is useful for verifying the functionality of the processor (when a data-bus device

is suspected of causing a system failure) or for trouble-shooting the Address Bus and Address Decode circuitry. Removing the jumper removes the operating power from both U2194 and U2294 to disconnect the Microprocessor from the buffered Data Bus. With the Data Bus disconnected, a resistor network pulls the processor Data Bus lines (D0 through D7) to a NOP (no operation) instruction. A NOP causes the Microprocessor to continuously increment through its address field. The Address Decode circuitry may then be checked to determine if it is operating properly.

Address Decode

The Address Decode circuitry generates enabling signals and strobes that allow the Microprocessor to control the various devices and circuit functions. The controlling signals are generated as a result of the Microprocessor placing specific addresses on the Address Bus. Figure 3-2 illustrates the enables and strobes generated by the Address Decode circuitry.

Address decoding is performed by a series of three-line-to-eight-line decoders attached to the Address Bus. The three most significant address bits are decoded by U2480. This device initially separates the total addressable-memory space (64k-bytes) into eight, 8k-byte blocks. Addresses in the top 32k-bytes (address bit A15 HI) select one of four read-only memories (ROM), U2162, U2178, U2362, or U2378. When the VMA (Valid Memory Address) and E (Enable) outputs from the Microprocessor go HI, the

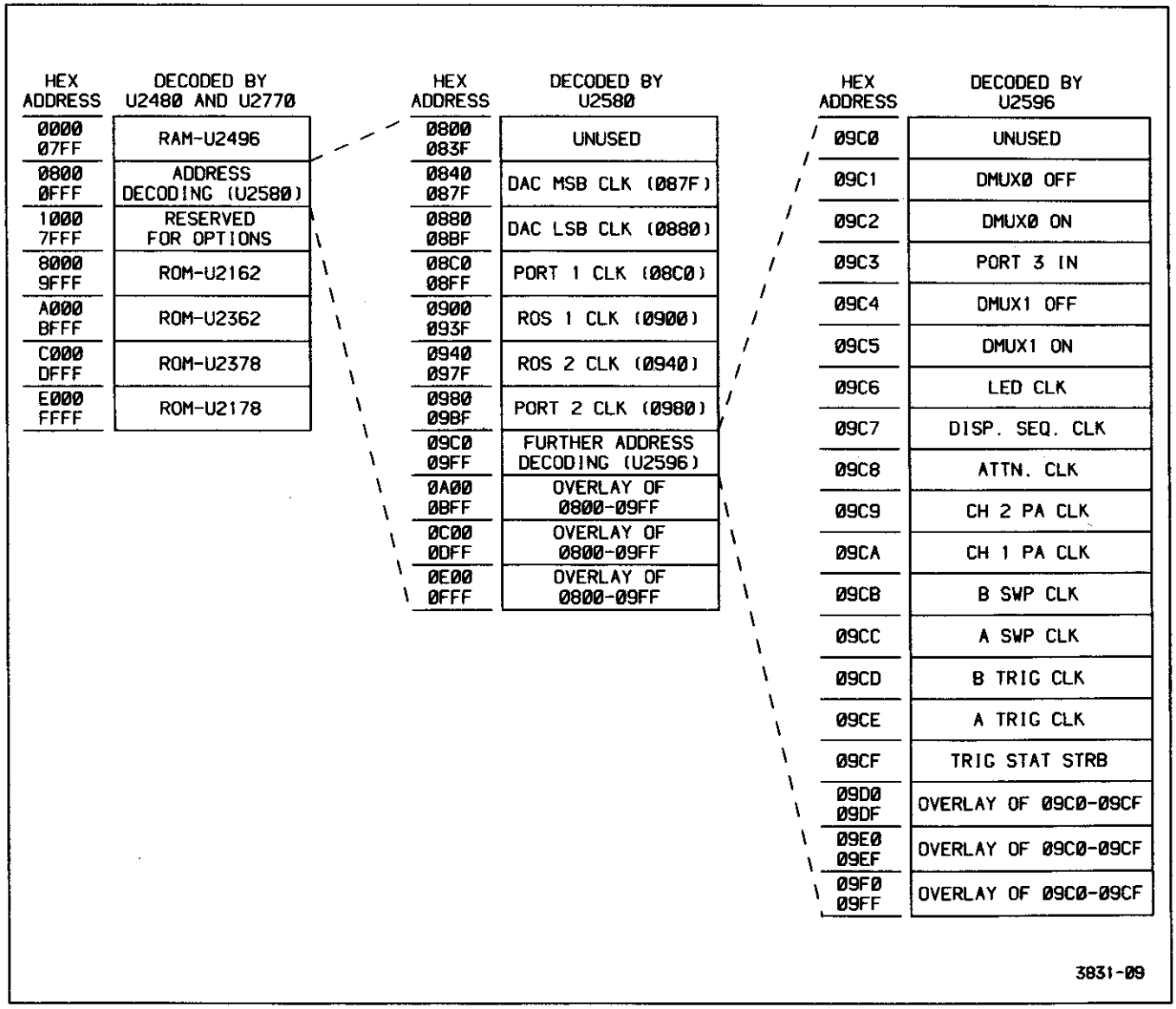

Figure 3-2. Address decoding.

selected ROM is enabled, and data from the selected address location is read out of the ROM.

Of the bottom 32k-bytes of addresses, only the lowest 8k-bytes are further decoded. When addresses in this 8k-byte range are decoded, the Y0 output of U2480 enables decoder U2770. This three-line-to-eight-line decoder separates the lowest 8k-byte address block into 2k-byte blocks. Any address falling into the lowest 2k-byte block of addresses will cause U2770 to generate an enable to the RAM (random-access memory) U2496. Addresses in the next highest 2k-byte block of addresses will enable U2580 to do the next stage of address decoding. The remaining 2k-byte blocks decoded by U2770 are not used.

The level of decoding performed by U2580 uses address bits A6, A7, and A8 to separate the addresses within the 2k-byte block of addresses 0800 to 0FFF into 32 groups of 64 addresses each. Address bits A9 and A10 are not used in the decoding scheme, so each of these 32 blocks is not uniquely identified. This results in four duplicate sections within the address block, each consisting of eight groups of 64 addresses. The upper three sections in the address space are never used; therefore, decoding by U2580 may be more simply thought of as eight groups of 64 address locations. Addresses within these eight groups generate control signals to other portions of the instrument.

The final level of address decoding is done by four-line-to-sixteen-line decoder U2596. When enabled by the Y7 output of U2580, this decoder separates the highest 64-address group decoded by U2580 into 16 individual control signals. In this level of decoding, address bits A4 and A5 are not decoded, so that the 64 possible addresses consist of four overlayed blocks of 16 addresses each.

Each of the control signals generated by the Address Decode circuitry are present only as long as the specific address defining that signal is present on the Address Bus. However, four of the addressable control signals decoded by U2596 are used to either set or reset flip-flops U2656B and U2656D. The control signals are, in effect, latched and remain present to enable multiplexers U2335 (diagram 2) and U170 (diagram 4). When enabled, these multiplexers route analog control signals from DAC (digital-to-analog converter) U2235 (diagram 2) to the various analog control circuits.

Read-only Memory (ROM)

The Read-only Memory consists of four, 8k-byte ROMs that contain the operating instructions (firmware) used to control processor (and thus oscilloscope) operation. Addresses from the Microprocessor that fall within the top 32k-bytes of addressable space cause one of the four read-only memory integrated circuits to be enabled. (See Address Decode description.) Instructions are read out of the enabled ROM (or PROM) IC from the address location present on its 13 address input pins (A0 through A12). The eight-bit data byte from the addressed location is placed onto the buffered Data Bus (BD0 through BD7) to be read by the Microprocessor.

Random-Access Memory (RAM)

The RAM consists of integrated circuit U2496 and provides the Microprocessor with 1k-byte of temporary storage space for data that is developed during the execution of a routine. The RAM is enabled whenever an address in the lowest 2k-byte of addresses is placed on the Address Bus. When writing into the RAM, the write-enable signal ($\overline{WE}$) on pin 21 of U2496 is set LO along with the chip enable ($\overline{CE}$) signal on pin 18. At the same time, the output-enable signal ($\overline{OE}$) on pin 20 is HI to disable the RAM output drivers. Data is then written to the location addressed by the Microprocessor. If data is to be read from the RAM, the $\overline{WE}$ signal is set HI to place the RAM in the read mode, and the $\overline{OE}$ signal is set LO to enable the output drivers. This places the data from the addressed location on the buffered Data Bus where it can be read by the Microprocessor.

Timing Logic

The Timing Logic circuit composed of U2468B, U2556F, U2556C, and U2656C generates time- and mode-dependent signals from control signals output from the Microprocessor. The enable (E) signal output from the Microprocessor is a 1.25-MHz square wave used to synchronize oscilloscope functions to processor timing.

Data applied to the Address Bus, Data Bus, and various control signals are allowed to settle (become valid) before any of the addressed devices are enabled. This is accomplished by switching the E signal HI a short time after each processor cycle begins. The delayed enable signal is inverted by U2556C to provide the active LO signal ($\overline{E}$) that enables the Address Decode circuit after the Address Bus has settled.

Read-Write Latch U2468B is used to delay the read/write signal (R/$\overline{W}$) from the Microprocessor to meet hold-time requirements of the RAM. At the same time, it generates delayed read and write enabling signals of both polarities to meet the requirements of Buffer U2194 and Latch U2294 (in the Microprocessor Data Bus) and various other devices in the Readout circuitry (diagram 7).

When R/$\overline{W}$ goes LO for a write cycle, Read-Write Latch U2468B is reset, and the Q output (pin 9) is held LO. Latch U2294 is in its transparent state at this time, and

data from the Microprocessor is applied asynchronously to the buffered Data Bus. At the end of the write cycle, the R/$\overline{W}$ signal goes HI, and the reset to U2468B is removed. The E signal also goes through a negative transition, and data on the Microprocessor data bus lines is latched into U2294. The next positive transition of the 1.25-MHz E signal (1/2 E cycle after the R/$\overline{W}$ signal goes HI) clocks the HI level at U2468B pin 12 (the D input) to the Q output, and the $\overline{Q}$ output (pin 8) goes LO. The 1/2 E cycle delay between the time R/$\overline{W}$ goes HI and the time that the Q output of U2468B goes HI keeps Latch U2294 outputs on long enough to meet the data hold time for the RAM. At the end of that delay time, pin 1 of U2294 goes HI, and the Latch outputs are switched to the high-impedance state to isolate it from the buffered Data Bus.

A write-enable signal to the RAM is generated by the circuit composed of U2656C and U2556F. The processor R/$\overline{W}$ signal is inverted by U2556F and NANDed with the enable signal (E) by U2656C. The write enable to the RAM at U2656C pin 9 is produced after the address data has settled. This action prevents writing to improper RAM address locations.

READOUT FRAMING AND INTERRUPT TIMING. Binary Counter U2668 is used to generate a readout-framing clock to the Readout circuitry and a real-time interrupt request to the Microprocessor via inverter U2556E. The readout-framing clock is a regular square-wave signal obtained from U2668 pin 14 by dividing the 1.25-MHz $\overline{E}$ signal from U2556C pin 6 by 1024 (2^{10}). This clock tells the readout circuitry to load the next block (subframe) of readout information to be displayed. (See "Readout" description for further information concerning the alphanumeric display.) The real-time interrupt request, which occurs every 3.3 ms, is obtained from pin 2 by dividing the $\overline{E}$ signal by 8192 (2^{13}).

When the real-time interrupt request occurs, $\overline{IRQ}$ (pin 4 of U2092) goes LO, and the processor breaks from execution of its mainline program. The Microprocessor first resets Binary Counter U2668 by setting pin 19 of U2043 (diagram 2) HI (to generate the reset), then it resets pin 19 LO to allow the counter to start again. At this time, the Microprocessor sets analog control voltages and reads trigger status from the Display Sequencer (diagram 11). When this is completed, it reverts back to the mainline program.

In addition to the analog control and trigger status update that occurs with each interrupt, on every fifth interrupt cycle, the Microprocessor also scans the front-panel potentiometers. Every tenth interrupt cycle, scanning the front-panel switches and checking the 50-Ω DC inputs for overloads is added to the previously mentioned tasks.

If all the tasks are not completed at the end of one interrupt cycle, the real-time interrupt request restarts the analog updates, but as soon as those are accomplished, the Microprocessor will pick up with its additional tasks where it was before the interrupt occurred. This continues until all tasks are completed. If any pot or switch changes are detected, the Microprocessor updates the analog control voltages and the control register data to reflect those changes prior to reverting back to the mainline program instructions.

ANALOG CONTROL

The Analog Control circuitry (diagram 2), under Microprocessor control, reads the front-panel controls and sets various analog control voltages to reflect these front-panel settings. The calibration constants determined during instrument calibration and the last "stable" front-panel setup conditions (unchanged for approximately seven seconds) are stored in EAROM (elecrically-alterable read-only memory). At power-on the stored front-panel information is used to return the instrument to its previous operating state.

Status Buffer

Data transfer from the Analog Control circuitry to the Microprocessor is via Status Buffer U2108. Data bits applied to the input pins are buffered onto the Data Bus when enabled by the Address Decode circuitry. Via the Status Buffer, the processor is able to (1) determine the settings of front-panel pot and switches, (2) read the EAROM data, (3) find out if the readout display should be switched on or off, (4) determine if a triggered sweep is in progress, and (5) read the contents of the Readout RAM. When disabled, the buffer outputs are switched to high impedance states to isolate them from the buffered Data Bus.

Front Panel Switch Scanning

The Front Panel Switches are arranged in a matrix of ten rows and five columns. Most of the row-column intersections contain a switch. When a switch is closed, one of the row lines is connected to one of the column lines through a diode. Reading of the switches is accomplished by setting a single row line LO and then checking each of the five column lines sequentially to determine if a LO is present (signifying that a switch is closed). After each of the five columns has been checked, the current row line is reset HI and the next row line is set LO for the next column scan cycle. A complete Front Panel Switch scan consists of setting all ten row lines LO in sequence and performing a five-column scan for each of the rows.

Row lines are set LO when the Microprocessor writes a LO to one of the flip-flops in octal registers U2034 and

U2134. The Row data placed on the buffered Data Bus by the Microprocessor is clocked into the registers as two, eight-bit words by clocks from the Address Decode circuitry (DAC LSB CLK for the lower eight bits and DAC MSB CLK for the upper eight bits). All eight outputs of register U2134 and two outputs of register U2034 drive the ten rows of the front-panel switch matrix (the eleventh line is not used in the matrix). Series resistors in the lines limit current flow and eliminate noise problems associated with excessive current flow.

While each row is selected, the processor will scan each of the five lines in sequence. To scan the columns, the processor increments the three data select bits to U2034 that define the column to be checked. Eight-line data selector U2456 connects the associated column line to Status Buffer U2108. As each line is selected, the Microprocessor reads the Status Buffer to determine if the associated switch is open or closed.

In addition to the front-panel switches, the CAL/NO CAL jumper (P501) is checked to determine whether the instrument should be allowed to execute the calibration routines. The levels on U2456 pins 7 and 9 are read by scanning two additional columns at power-up. If the jumper is pulling the CAL bit LO, the operator will be allowed to use the calibration routines stored in firmware. If the NO CAL bit is pulled LO, the calibration routines may not be performed. If the jumper is removed, and neither bit is pulled LO, the Microprocessor is forced into a special diagnostic mode (CYCLE) used to record certain operating failures during long-term testing of the instrument. (See the "Maintenance" section of this manual for an explanation of the diagnostic modes.) Removing P501 or switching it between the CAL and NO CAL positions will not be recognized by the Microprocessor until the instrument is powered down and then turned back on.

The SI (scope identification) bit is checked at power-up to determine if the instrument is a 2465. Some parts of the firmware are shared with a similar instrument, the 2445, and the check is necessary for the Microprocessor to distinguish between the two instruments. A LO on the SI bit indicates that the instrument is a 2465.

The resistors in series with the input lines to U2456 are current-limiting resistors that protect the CMOS eight-line data selector from static discharges. The resistors connected from the input lines to the +5-V supply are pull-up resistors for the front-panel column lines.

Digital-to-Analog Converter (DAC)

DAC U2234 is used to set the various analog references in the instrument and is used to determine the settings of the front-panel potentiometer. The 12-bit digital values to be converted are written to octal registers U2034 and U2134 for application to the DAC input pins. The DAC then outputs two complementary analog currents that are proportional to the digital input data. (Complementary, in this case, means that the sum of the two output currents is always equal to a fixed value.)

The maximum range of the output currents is established by a voltage-divider network composed of R2127, R2227, R2228, and R2229 connected to the positive and negative reference current inputs of the DAC (pins 14 and 15 respectively). A +10-V reference voltage applied to the DAC through R2228 sets the basic reference current. Resistor R2229 and potentiometer R2127 provide a means to adjust this current over a small range for calibration purposes. The nominal reference current is 1 mA, and the DAC full-scale output current is 4 mA. The output currents flow through series resistors R2324 and R2325, connected to the +1.36-V reference, and proportional voltages result.

Pot Scanning

The Pot Scanning circuitry, in conjunction with the DAC, derives digital values for each of the various front-panel potentiometers. Scanning of the pots is accomplished by data selectors U2408 and U2418. Three bits are written to register U2208 and select the pot to be read. The bits are latched in the register and keep the pot selected until the register is reset. The Microprocessor writes a LO to the inhibit input (pin 6) of either U2408 or U2418 via register U2308 to enable the device. The enabled data selector connects the analog voltage at the wiper of the selected pot to comparator U2214.

Comparator U2214 compares the analog voltage of each pot to the output voltage from the DAC (pin 18). To determine the potentiometer output voltage, the processor performs a binary search routine that changes the output voltage from the DAC in an orderly fashion until it most closely approximates the voltage from the pot.

The conversion algorithm is similar to successive approximation and generates an eight-bit representation of the analog level. When the pot's value is determined, the Microprocessor stores that value in memory. Once all the pots have been read and the initial value of each has been stored, the processor uses a shorter routine to determine if any pot setting changes. To do this the DAC output is set to the last known value of the pot (plus and minus a small drift value), and the status bit is read to see that a HI and LO occurs. If within the limits, the processor assumes that the pot setting has not changed and scans the next pot. When the processor detects that a pot setting has changed, it does another binary search routine to find the new value of that pot.

Analog Control

The operating mode and status of the 2465 requires that various analog voltages (for controlling instrument functions) be set and updated. The digital values of the controlling voltages are generated by the Microprocessor and converted by the DAC. Analog multiplexers U2335 (on diagram 2) and U170 (on diagram 4) route the DAC voltages to sample-and-hold circuits that maintain the control voltages between updates.

The Microprocessor writes three selection bits to register U2034 that directs the DAC output to the appropriate sample-and-hold circuit and charges a capacitor (or capacitors) to the level of the DAC. When the processor disconnects the DAC voltage from the sample-and-hold circuit (by disabling the multiplexer) the capacitor(s) remains charged and holds the control voltage near the level set by the DAC. Due to the extremely high input impedance of the associated operational amplifiers, the charge on the capacitor(s) remains nearly constant between updates.

EAROM

EAROM (electrically-alterable read-only memory) U2008 provides nonvolatile storage for the calibration constants and the power-down front-panel settings. When power is applied to the 2465, the Microprocessor reads the calibration constants and generates control voltages to set up the analog circuitry. The front-panel settings that were present at power-off are recalled to return the instrument to that same operating mode.

The EAROM is a metal-nitride-oxide-semiconductor device (MNOS) and requires a TTL-to-MNOS level shift of the input control and data signals. A MNOS-to-TTL level shift of the output data is also required. Inputs to U2008 are shifted to MNOS levels by U2118B through U2118F and the associated components while output data is shifted back to TTL levels by Q2025, U2118G, and the associated components.

The EAROM data, address, and mode-control bits are written by the Microprocessor to five flip-flops of register U2208. The register outputs drive the level-shifting network in the associated line. Three of thise latched bits define the EAROM mode and will direct data into and out of the device. These three mode control bits are applied to pins 7, 8, and 9 of U2008 and set the mode to either Accept Address, Accept Data, Write Data, Read Data, or Shift-Data-Out.

When writing data into the EAROM, the mode is first set to Accept Address, then the address of the location to be altered is applied to the I/O port (pin 12) as a specially encoded sequence of 20 single bits via U2118C, R2020, and CR2021. This sequence of bits is two, one-of-ten codes where the position of the first LO bit in the sequence represents the most-significant bit of the address (in decimal) and the position of the second LO represents the least-significant digit (see Figure 3-3).

The processor clocks each of the 20 bits into the internal address register by clocking U2008 pin 6 via the clock level shifting network (U2118C and associated components).

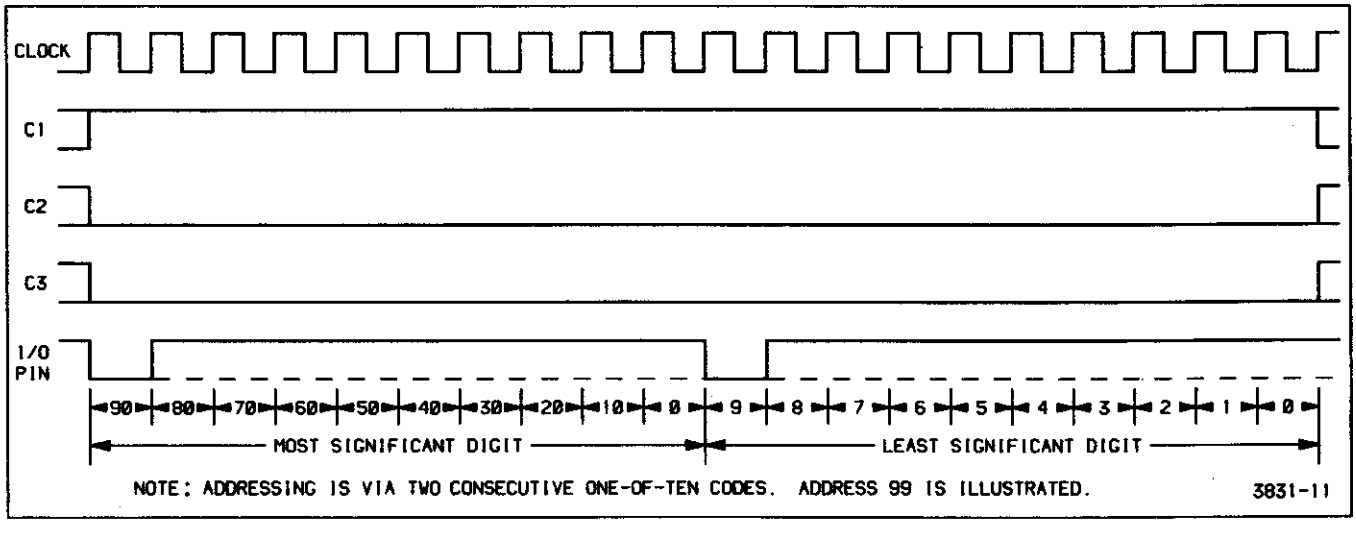

Figure 3-3. Accept address timing.

Internal address decoding within U2008 then enables the selected address location. The three mode-control bits are then set to the Accept Data mode, and the new 14-bit serial data word is applied to the I/O pin. The data bits are clocked into a temporary data-storage register and the mode-control bits are set to the Write mode. A series of clock pulses then writes the data from the temporary data storage register to the addressed location.

When reading from the EAROM, the processor first sets the three-bit mode-control word to Accept Address as in writing, and the 20-bit address is clocked into the EAROM. Now the mode-control word is set to Read Data, and a single clock pulse moves the data from the addressed location to the temporary data-storage register in parallel. The EAROM mode is then set to Shift Data Out, and the 14-bit data word is clocked serially from the temporary storage register to the I/O pin.

The output data is applied to Q2025, U2118G, and the associated components, to shift it to TTL levels. The Status Buffer U2108 applies the data to the Data Bus where the Microprocessor may read it.

FRONT-PANEL CONTROLS

The Front Panel is the operator's interface for controlling the user-selectable oscilloscope functions. Along with the crt, it provides visual feedback to the user about the present operating state of the instrument.

Most of the Front-Panel controls (diagram 3) are "cold" controls; they are not connected directly into the signal path. Therefore, associated circuits are not influenced by the physical parameters (such as capacitance, resistance, and inductance) of the controls. In addition, translating the analog output levels of some of the potentiometers to digital equivalents allows the processor to handle the data in ways that result in a variety of enhanced control features.

To maintain the front-panel operating setup between uses of the instrument, the digitized values of the potentiometers and front-panel switch settings are stored in EAROM at regular intervals (approximately every seven seconds) so that when the instrument power is turned off, these control settings are not lost. Then, when power is next applied, the instrument will power up to the same configuration as when the power was last removed (assuming the settings of the nondigitized pots and switches remain the same).

The Front-Panel controls also allow the user to initiate and direct the diagnostic routines (and when enabled, the calibration routines) programmed into the read-only memory (ROM). These routines are explained in the Maintenance section of this manual.

Front Panel Switches

The Front Panel Switches are arranged in a ten-row-by-five-column matrix, with each switch assigned a unique location within the matrix (see Figure 3-4). A closed switch connects a row and a column together through an isolating diode. To detect a switch closure, the switch matrix is scanned once every 32 ms (every tenth Microprocessor interrupt cycle). When scanning, the Microprocessor sequentially sets each individual row line LO. A closed switch enables the LO to be passed through the associated diode to a column line. When the processor checks each of the five column lines associated with the selected row, the LO column is detected. The intersection of the selected row and the detected column uniquely identifies the switch that is closed. Further information about switch scanning is found in the "Front-Panel Scanning" description located in the "Analog Control" discussion.

As each switch is read, the processor compares the present state of the switch to its last-known state (stored in memory) and, if the same, advances to check the next switch. When a switch is detected as having changed, the processor immediately reconfigures the setup conditions to reflect the mode change and stores the new state of the switch in memory. The detected status of the switch on each of the following scan cycles is then compared against the new stored data to determine if the switch changes again. The 32-ms delay between the time a switch is detected as having changed and the next time it is read effectively eliminates the effects of switching noise (switch bounce) that may occur after the switch is actuated.

Front-Panel Potentiometers

The thirteen Front-Panel Potentiometers are "cold" controls that control the linear functions of the instrument. (SCALE ILLUM, READOUT INTENSITY, INTENSITY, and FOCUS are not considered part of the Front-Panel Control circuitry for the purposes of this description.) Of these, eight are digitized and control their functions indirectly. The remaining five potentiometers (four vertical POSITION pots and the TRACE SEP pot) control their respective circuit functions directly. Data Selectors U2048 and U2148 in the Analog Control circuitry (diagram 2) route the wiper arm voltage of the pot being read to comparator U2214 where it is compared with the output of DAC U2234. The processor changes the DAC output until it most closely matches the output voltage of the pot, then stores the digital value of that "match". See the "Front-Panel Switch Scanning" description in the "Analog Control" discussion for further information on the reading of pot values.

Like the switch matrix scanning, the Front-Panel pot scanning routine is performed every 32 ms. When entered, the routine reads the settings of the last-moved pot and one unmoved pot. Each succeeding scan continues to read the last-moved pot, but a new unmoved pot is read. In this way, each pot is monitored, but most of the scan time is devoted to the pot that is most likely to still be moving (needing continuous updating).

As the initial pot settings are determined, a digital representation of each value is stored in memory. The processor then checks each pot against its last-known value to determine if a pot has moved. If a pot is detected as moving, the processor executes a routine that converts the movement (displacement from last-set value) into a corresponding control voltage.

When producing the actual analog control levels, the processor can manipulate the digital values read for the various pots before sending the output data to the DAC. This allows many of the oscilloscope parameters to vary in an enhanced fashion. The pot data is manipulated by the processor in a manner that produces such features as variable resolution, continuous rotation, fine-resolution backlash, and electrically detented controls.

In the cases of the TRIGGER LEVEL, Horizontal POSITION, VOLTS/DIV VAR, and SEC/DIV VAR controls, the processor reads the magnitude and direction of pot rotation and produces variable-resolution control voltages. If a pot's direction of rotation changes, the magnitude of the change from the last-set position remains small, or if it was not the

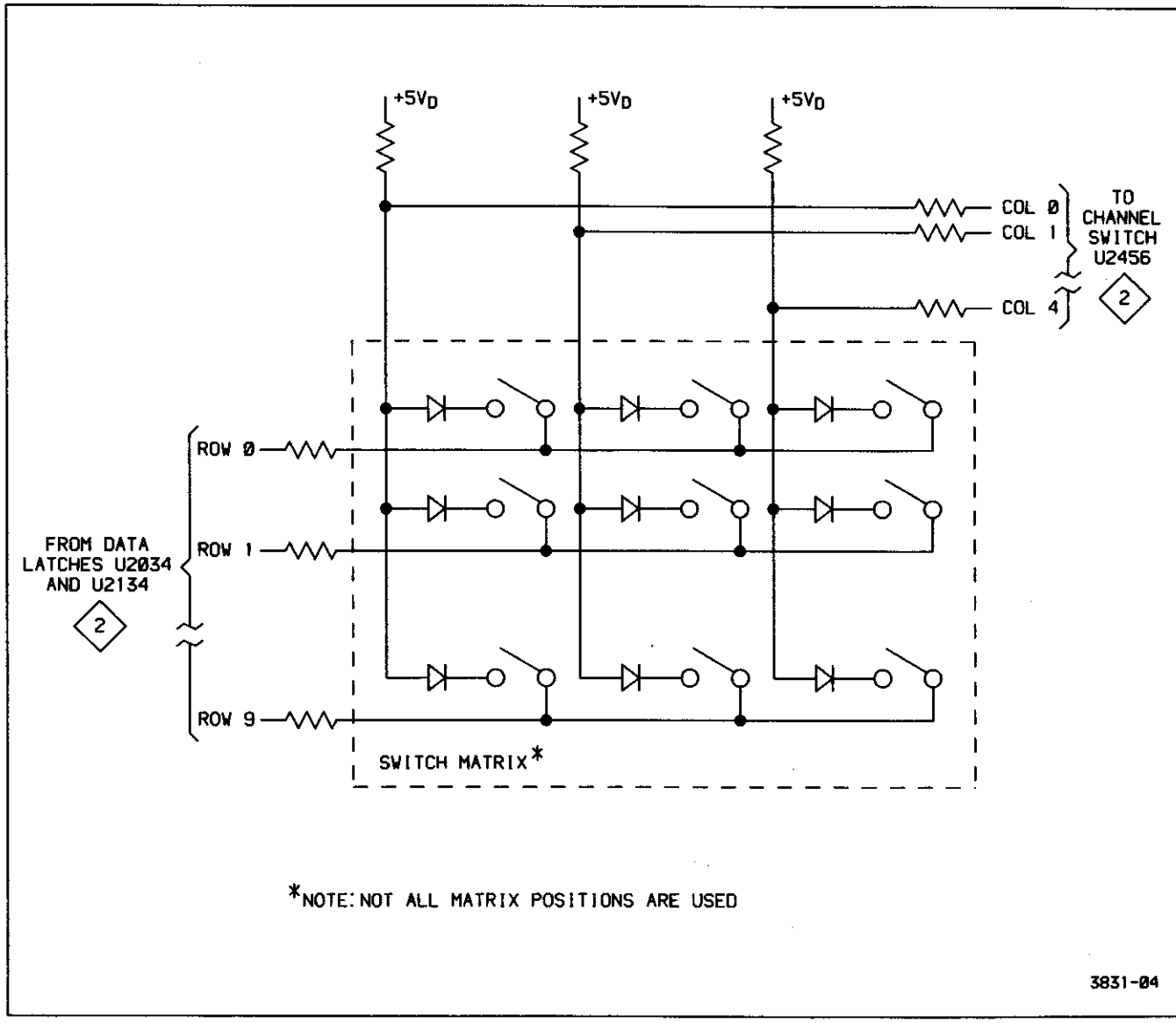

Figure 3-4. Front-Panel Switch matrix.

last pot moved, a fine-resolution control voltage results. In the fine-resolution range, a given rotational displacement will cause a small control voltage change. The same displacement farther away from the last-set reference will cause a proportionally larger control voltage change, producing a coarse-resolution effect. If the changing pot is the last one moved and the direction of rotation remains the same, the algorithm continues from where it left off during the preceding scan; producing control voltage changes with the same increment as it was last using.

The delta reference controls (Δ REF OR DLY POS and Δ) are continuous-rotation potentiometers. They each consist of two pots ganged together with their wiper arms electrically oriented 180° apart. As the wiper of one pot is leaving its resistive element, the wiper of the other pot comes onto its element. The Microprocessor has the ability to watch the output voltage from each wiper and when it detects that the controlling wiper is nearing the end of its range, it will switch control over to the other wiper. The routine the processor uses to watch these pots sets the associated control voltage on the basis of relative voltage changes (ΔV) that occur. Switching between the pots to change control to the opposite wiper arm is based on the specific voltage levels being sensed.

Sensing specific voltage levels is also used when reading the VOLTS/DIV VAR and SEC/DIV VAR controls. These pots have both a mechanical detent and a processor-generated electrical detent. As one of these controls is moved out of the mechanical detent position, the processor watches the analog voltage changes that occur; but the associated control voltage will not change until a specific voltage level (the electrical detent level) is reached. Once the electrical detent value is exceeded, the processor begins to vary the associated control voltage in response to further pot rotation. When returning to the mechanical detent position, the electrical detent level is reached first, and the variable voltage action is stopped before the mechanical detent is entered.

Front-Panel Status LED

Light-emitting diodes (LED) are used to provide visual feedback to the operator about the oscilloscope status and operating mode by backlighting front-panel nomenclature. A 32-bit status word, defining the diodes to be illuminated, is generated by the processor and then serially clocked into the four LED-Status Registers (U3300, U3325, U3350, and U3375). The registers hold the selected diodes on until the next update. Whenever the processor detects that a front-panel control has changed (and a different status display is required), a new status word is generated and applied to pin 1 of U3300. As each of the bits is clocked into the Q_A position of U3300, the preceding bit is shifted to the next register position. After 32 bits have been clocked into (and 24 bits through) U3300, all four LED-Status registers are full and contain the LED illumination pattern to be displayed to the user. A LO at any Q output of the registers illuminates the corresponding front-panel LED.

The TRIG'D LED is not driven by the LED-Status Register. It is driven by the Analog Control circuitry and illuminated whenever a triggered sweep is in progress.

ATTENUATORS AND PREAMPLIFIERS

The Attenuators and Preamplifiers circuitry (diagram 4) allows the operator to select the vertical deflection factors. The Microprocessor reads the Channel VOLTS/DIV switches and VOLTS/DIV VAR controls and then digitally switches the attenuators and sets the preamplifier gains accordingly.

Channel 1 and Channel 2 Attenuators

The Channel 1 and Channel 2 Attenuators are identical in operation, with corresponding circuitry in each channel performing the same function. Therefore, only the Channel 1 circuitry is described.

Input signals from the Channel 1 input connector are routed through an attenuator network by four pairs of magnetic-latch relay contacts. The position of the relays is set by Microprocessor data placed into Auxiliary Control Register U140. Relay buffer U110 provides the necessary drive current to the relays.

Four input coupling modes (1 MΩ AC, GND, 1 MΩ DC, and 50 Ω DC) and three attenuation factors (1X, ÷10, and ÷100) may be selected by closing different combinations of relay contacts. The three attenuation factors, along with the variable gain factors of the Vertical Preamplifier, are used to obtain the crt deflection factors. The relays are magnetically latched and once set, remain in position until new attenuator-relay-setting data and strobes are generated. (See the "Auxiliary Control Register" description for a discussion of the relay-latching procedure.)

The 50 Ω termination resistor has a thermal sensor associated with it that produces a dc voltage (CH 1 OVL) proportional to the input power. Should the input power exceed the normal safe-operating level for the 50 Ω DC input, the termination resistor temperature will exceed the normal operating limit and will change the output voltage of the thermal sensor. The amplitude of this dc level is periodically checked via comparator U2214 and DAC U2234 (on diagram 2) and allows the Microprocessor to detect when an overload condition is present. When an overload occurs, the processor switches the input coupling to the 1 MΩ position to prevent damage to the attenuator and displays **50 Ω OVERLOAD** on the crt.

Compensating capacitor C105 is adjusted at the time of calibration to normalize input capacitance of the preamplifier to the attenuator.

A probe-coding ring around the BNC input connector passes probe-coding information (a resistance value to ground) to the Analog Control circuitry for detection of probe attenuation factors. The readout scale factors are set to reflect the detected attenuation factor of the attached probe.

Auxiliary Control Register

The Auxiliary Control Register allows the Microprocessor to control various mode and range dependent functions of the 2465. Included in these functions are: attenuation factors, Channel 3 and Channel 4 gains, vertical-bandwidth limiting, and the X-Y display mode.

When the Microprocessor sets the input coupling mode and attenuation factors for Channel 1 and Channel 2, a series of eight, 16-bit control words are serially clocked into shift registers U140 and U150 (eight bits in each register). Each control word is used to set the position of one of the eight attenuator and coupling relays (four relays are in each attenuator assembly). Each control word will have only the bit corresponding to the specific relay contact to be closed set HI. Relay buffers U110 and U130A (for Channel 1) and U120 and U130B (for Channel 2) are Darlington configurations that invert the polarities of all bits. This results in a LO being applied to only the coil lead associated with the contact to be closed; all other coil leads are held HI.

To set a relay once the control word is loaded, the Microprocessor generates a ATTN STRB (attenuator strobe) to U130G pin 7 via R129 and C130. The strobe pulses the output of U130G LO for a short time. This output pulse attempts to turn on both Q130 and Q131 (relay drivers) via their identical base-bias networks. Due to the lower level from the turned on Darlington relay buffer (coupled through the associated coil diode and either CR130 or CR131 to one of the bias networks), one transistor will turn on harder as the ATTN STRB pulse begins to forward bias the transistors. The more positive collector voltage of the transistor turning on harder is fed through the bias diode (again either CR130 or CR131) to further turn off the opposite transistor. This action results in one transistor being fully on and the other one being fully off. The saturated transistor sources current through the two stacked relay coils to the LO output of either U140 or U150 (current sink) to close the selected contacts. Once set, the magnetic-latch feature will hold the relay set to this position until opposing data is clocked into the Auxiliary Control Register and strobed into the relay. All coil leads for the remaining relays are set HI, and only the selected relay will be set.

To set the seven remaining Attenuator and coupling relays, the sequence just described is repeated seven more times. Whenever the Microprocessor determines that the attenuation factor or input coupling has changed, the entire relay-setting procedure is repeated for all eight relays.

After the coupling and attenuator relays have been latched into position, the Auxiliary Control Register is free to be used for further circuit-controlling tasks. Eight more bits of control data are then clocked into U140 either to enable or disable the following functions: vertical bandwidth limiting (BWL), triggered X-Y mode (TXY), the A and B Sweep Delay Comparators (BDCA and BDCB), and slow-speed intensity limit (SIL); or to alter the Channel 3 and Channel 4 gain factors (GA3 and GA4). Two other bits are clocked into register U150: one to produce the CTC signal and the other to control the scale illumination circuit during SGL SEQ display mode. The CTC control bit is used to enable a sweep-start linearity circuit in the A Sweep circuitry (diagram 5) on the 2 ns and 20 ns per division sweeps.

Analog Control Multiplexer

When enabled by the Address Decode circuitry, Analog Control Multiplexer U170 directs the analog levels applied to pin 3 from DAC U2234 (diagram 2) to one of six sample-and-hold circuits. In the Preamplifier circuitry, the sample-and-hold circuits maintain the VAR gain and DC Bal control-voltage levels applied to both the Channel 1 and Channel 2 Preamplifiers U100 and U300 between updates. Two of the Multiplexer outputs direct analog levels to the Holdoff and Channel 2 Delay Offset sample-and-hold circuits (diagram 5). Routing is determined by the three-bit address from register U2034 (diagram 2) applied to Multiplexer U170 on pins 9, 10, and 11.

Channel 1 Preamplifier

Channel 1 Preamplifier U100 converts the single-ended input signal from the Channel 1 Attenuator to a differential output signal used to drive the Vertical Channel Switch. The device produces either amplification or attenuation in predefined increments, depending on the control data written to it from the Microprocessor. The Preamp also has provisions for VAR gain, vertical positioning, and a trigger signal pickoff.

The Channel 1 vertical input signal is applied to pin A of Channel 1 Preamp U100. Control data from the processor is clocked into the internal control register of the device via pin 22 (CD) by the clock signal applied to pin 23 ($\overline{CC}$). The data sets the device to have an input-to-output gain ratio of either 2.5 or 1 or to have an attenuation factor of 2, 4, or 10, depending on the VOLTS/DIV control setting.

Two analog control voltages set by the DAC and the Channel 1 vertical position dc level modify the differential output signal at pins 9 and 10. The front-panel Channel 1 POSITION control supplies a dc level to U100 pin 17 that vertically positions the Channel 1 display on the crt. A DC Bal signal is applied to pin 2 of U100 from the DAC via the sample-and-hold circuit composed of U160A and C177. This DC Bal signal is a dc offset-null level that is determined during the automatic DC Bal procedure. The offset value is stored as a calibration constant in the EAROM and is recalled at regular intervals to set the DC Bal level, holding the Preamp in a dc balanced condition.

The Channel 1 VOLTS/DIV VAR control is monitored by the Microprocessor during the front-panel scanning routine. When the processor has determined where the VOLTS/DIV VAR control is positioned, it causes DAC U2234 (diagram 2) to produce a corresponding control level and routes it to the VAR gain sample-and-hold circuit composed of U160D, C179, and associated components. The control voltage at the output of U160D (pin 14) sets the variable gain of the Preamp.

A pickoff amplifier internal to U100 conditions the trigger signal and provides the proper signal level at pin 15 to drive the A/B Trigger Generator (U500, diagram 5). The pickoff point for the trigger signal is prior to the addition of the vertical position offset, so the position of the signal on the crt has no effect on the trigger operation. However, the pickoff point is after the DC Bal and Variable gain signals have been added to the signal so both of these functions will affect trigger operation.

Common-mode signals are rejected from the trigger signal by the circuitry composed of operational amplifier U450A and associated components. The inverting input of U450A (pin 6) is connected to the common-mode point between APO+ (pin 12) and TPO− (pin 15) of U100. Any common-mode signals present are inverted and applied to a common-mode point between R451 and R453 to cancel the signals from the differential output. A filter network composed of LR180 and the built-in circuit board capacitor (5.6 pF) reduces trigger noise susceptibility. Trigger signals for options are obtained by removing P100A and connecting the appropriate connector.

The Channel 1 input signal used to provide the horizontal deflection for the X-Y displays is obtained from U100 pin 11. The components between pin 11 and the Horizontal Output Amplifier provide phase compensation of the signal. During instrument calibration, the delay produced by C115, C116, L115, R115, and variable capacitor C118 is matched to the 78-ns delay of the vertical delay line (DL100, diagram 6).

Channel 2 Preamplifier

Operation of Channel 2 Preamplifier U200 is nearly identical to that of the Channel 1 Preamplifier just described. The exceptions are that the output polarity of the Channel 2 signal may be either normal or inverted and that the signal obtained from the BPO+ output (pin 11) is conditioned differently for a different purpose than in the Channel 1 Preamplifier circuitry.

Inverting the Channel 2 signal for the CH 2 INVERT feature is accomplished by biasing on different amplifiers. The control data clocked into the internal control register from pin 22 sets up the necessary switching.

The Channel 2 BPO+ signal at U200 pin 11 provides an accurate representation of the Channel 2 signal at the rear-panel CH 2 OUT connector. The BPO+ output signal is reduced by divider R460 and R461 and is applied to the emitter of Q460B. Transistor Q460B, configured as a diode, provides thermal compensation for the bias voltage of Q460A and reduces dc level shifts with varying temperature. Emitter-follower Q460A provides the drive and impedance matching to the CH 2 OUT connector and removes the diode drop added by Q460B. Clamp diodes CR460 and CR461 protect Q460B should a drive signal be accidentally applied to the CH 2 OUT connector.

Channel 3 and Channel 4 Preamplifier

The functions provided by the Channel 3 and Channel Preamplifier are similar to those provided by the Channel 1 and Channel 2 Preamplifiers. The single-ended CH 3 and CH 4 input signals are converted to differential signals, and vertical gain and vertical positioning information is added to the output signals. Trigger pickoff signals are generated for both channels and are routed to the Trigger hybrid.

Channel 3 and Channel 4 gains may be either 0.1 volt per division or 0.5 volt per division. The logic levels of control bits applied to U300 pin 30 (GA3) and pin 31 (GA4) from Auxiliary Control Register U140 sets the gain of the Channel 3 and Channel 4 Preamplifiers respectively. Vertical positioning of the Channel 3 and Channel 4 signals on the crt is controlled by the variable voltage levels applied to pin 29 (POS3) and pin 30 (POS4) from the front-panel CH 3 and CH 4 POSITION potentiometers.

Dc offsets in the output signal due to any tracking differences between the +5-V and the −5-V supply to U300 are reduced by the tracking regulator circuit composed of U165A, Q190, and associated components. Operational amplifier U165A and Q190 is configured so that the output of voltage at the emitter of Q190 follows the −5-V supply applied to R198. This tracking arrangement ensures that the supply voltages are of equal magnitudes to minimize dc offsets in the output signals.

Scale Illumination

The Scale Illumination circuit consists of U130C, U130D, U130E, U130F, and associated components. The circuit enables the operator to adjust the illumination level of the graticule marks on the crt face plate using the SCALE ILLUM control.

Components U130C through U130F, depicted on diagram 4 as inverters, are actually Darlington transistor pairs. Figure 3-5 is a simplified illustration of the Scale Illumination circuitry, redrawn to show U130C through F as Darlington transistor pairs for the purpose of the following description.

Darlington transistors U130D and U130E control the current flow to scale-illumination lamps DS100, DS101, and DS102. Base drive current for U130D and U130E via R133 is set by the front-panel SCALE ILLUM pot R134. Voltage at the more negative end of the pot is set by the self-biasing configuration of U130F and R135. The voltage level established by these two components is two diode drops above ground (≈ 1.2 V) so that, at full counter-clockwise rotation, the wiper voltage of the SCALE ILLUM pot will just match the turn-off point of U130D and U130E. The voltage at the other end of the pot is set by the collectors of U130D and U130E. As the SCALE ILLUM pot is advanced, the base drive to U130D and U130E increases, and the voltage on their collectors moves closer to ground potential. This increases the current through the scale-illumination lamps to make them brighter and produces some negative feedback to the base circuit through the SCALE ILLUM pot. Negative feedback stabilizes the base drive to U130D and U130E to hold the illumination level constant at the selected setting of the SCALE ILLUM control.

During SGL SEQ display mode, the graticule is illuminated only once during the sequence for photographic purposes. In this mode, a HI is initially written to Auxiliary Control Register U150 (bit Q_H). This turns on U130C and shunts the base drive current of U130D and U130E to ground. At the point in the sequence when the graticule should be illuminated, the processor writes a LO to bit Q_H, and U130C is turned off. This enables U130D and U130E to turn on the lamps to the illumination level set by the SCALE ILLUM pot.

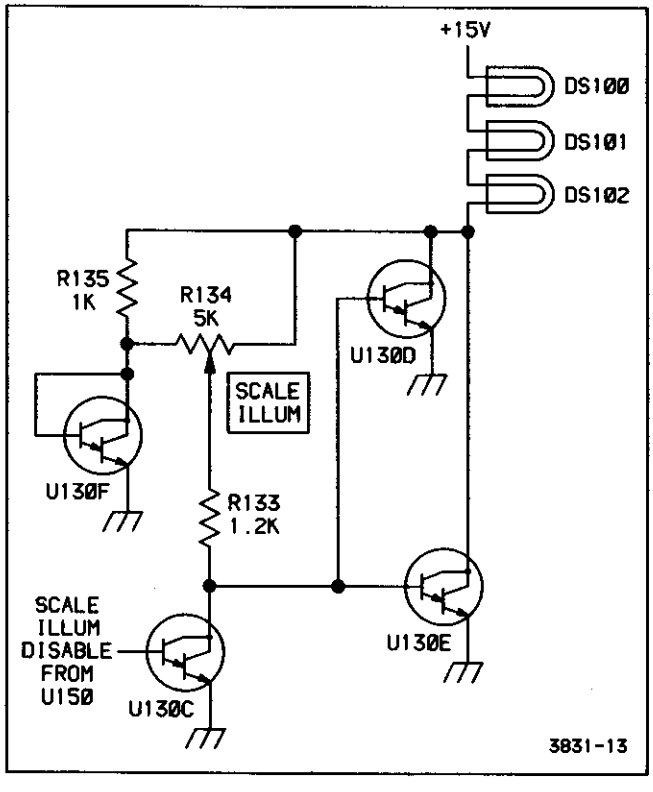

Figure 3-5. Scale Illumination circuit.

DISPLAY SEQUENCER, TRIGGERS, AND SWEEPS

The Display Sequencer circuitry (diagram 5) controls and sequences the "analog-type" oscilloscope functions in real time, dependent on control data it receives from the Microprocessor. The A/B Trigger circuitry, under control of the Display Sequencer, detects when triggering requirements are met and initiates the appropriate sweep. The A Sweep and B Sweep circuits generate sweep ramps under control of the Display Sequencer when triggered by the A/B Trigger circuitry.

Display Sequencer

The Display Sequencer stage consists primarily of integrated circuit U650. This IC accepts analog and digital control signals from various parts of the instrument and, depending on the control data string clocked into its internal control register from the Microprocessor, will change control signals that it sends to other, signal-handling circuits.

Fifty-five bits of serial data from the processor defining the instrument's operating sequence are applied to the Display Sequencer data input, pin 25. The data string is clocked into U650 to the internal control register by the processor-generated control clock applied to pin 24. The data string is organized in several fields, with each field defining the operating mode of one specific instrument function.

Display Sequencer U650 controls the various functions defined by the data fields by setting the levels of the associated control lines. The functions and controlling signal lines for each function are as follows:

Vertical Display Selection

CH 1, CH 2, CH 3, CH 4, ADD, and Readout Y signals are selected by the $\overline{VS1}$, $\overline{VS2}$, $\overline{VS3}$, and $\overline{VS4}$ control signals. See the Vertical Channel Switch description for further information.

Horizontal Display Selection

A Sweep, B Sweep, CH 1 (for X-Y displays) and Readout X are selected by the $\overline{HSA}$ and $\overline{HSB}$ control signals See the Horizontal Output Amplifier description for further information.

Trigger Source Selection

CH 1, CH 2, CH 3, CH 4, ADD, Line, and a sample of the vertical output signal (for calibration purposes only) are selectable as the Trigger SOURCE by the $\overline{SR0A}$, $\overline{SR1A}$, $\overline{SR2A}$, $\overline{SR0B}$, $\overline{SR1B}$, and $\overline{SR2B}$ control lines (pins 28, 27, 29, 32, 31, and 30 respectively). See the A/B Trigger description for further information.

Trigger Holdoff

Sweep recovery time and the circuit initialization time required when front-panel controls are changed are controlled by the THO (trigger holdoff) signal.

Delta Time (Δt) Delay Selection

DLY REF 0 or DLY REF 1 is selected by the DS (delay select) signal.

Trigger and Sweep Activity (Status)

The activity of the Trigger and Sweep circuits, as indicated by the $\overline{SGA}$, $\overline{SGB}$, $\overline{TSA}$, and $\overline{TSB}$ lines, is reported to the Microprocessor via the TSO (trigger status output) line when clocked by the TSS (trigger status strobe) signal.

Intensity Control

The readout intensity, display intensity, and display intensity compensation are controlled by the BRIGHT output level.

Display Blanking

Display blanking for CHOP VERTICAL MODE, Readout transitions, and front-panel control changes is controlled by the BLANK output.

Readout Control

The vertical selection, horizontal selection, and intensity controls are all set to their readout modes either at the end of an A Sweep ($\overline{SGA}$ goes HI) or in response to a readout request ($\overline{ROR}$) from the Readout circuitry (diagram 7). While in the readout mode, the BLANK control signal is driven by the readout blank ($\overline{ROB}$) input signal on pin 5 (also from the Readout circuitry). The readout active line ($\overline{ROA}$, pin 6), when set LO, tells the Readout circuitry that readout dots may be displayed if necessary. The $\overline{ROA}$ signal is always set LO at the start of the trigger holdoff time following sweeps, and it is held there until the holdoff time is almost over. This allows the majority of holdoff time to be used for displaying readout dots. The Display Sequencer will switch the $\overline{ROA}$ signal back to HI before the end of holdoff so that the readout display does not interfere with display of the vertical signal at the triggering event.

Trace Separation

Vertical separation between the A Sweep trace and the B Sweep traces (for alternate horizontal sweep displays), and between the reference B Sweep trace and the delta B Sweep trace (when delta time is selected in B Sweep only mode), is enabled by the TS1 + TS2 output.

X10 Horizontal Magnification

Horizontal X10 magnification is controlled by the $\overline{MAG}$ output.

Calibrator Timing

The 5-Hz to 5-MHz drive signal to the Calibrator circuitry is provided by the CT output.

In the course of developing waveform displays, the Display Sequencer selects one or more vertical channel, sets the trigger source, and selects the horizontal display mode. In most cases, the trigger selection does not change after it has been set unless a front-panel trigger control is changed. An exception is that in VERT TRIGGER MODE, the trigger source tracks the sequencing of the vertical channels (unless AUTO LVL MODE, or CHOP VERTICAL MODE is also selected). Trigger source selection lines are changed only during trigger holdoff time between sweeps.

HOLDOFF RAMP. The holdoff ramp circuit, used to delay the start of a sweep until all circuits have recovered from the previous sweep, is made up of U165C, Q154, Q155, and associated components. Operational Amplifier U165C and capacitor C180 form a sample-and-hold buffer

used to set the charging current for holdoff-ramp integrating capacitor C660. A control voltage from digital-to-analog converter (DAC) U2234 (diagram 2) via multiplexer U170 (diagram 4) is stored on C180. The stored voltage level sets the base voltage for both Q154 and Q155 via amplifier U165C. Transistors Q154 and Q155 form a current-mirror with nearly equal collector currents. Transistor Q154 is a current-to-voltage converter that provides negative feedback to U165C, setting loop gain. Transistor Q155 acts as a constantcurrent source that charges integrating capacitor C660, producing a linear holdoff ramp.

A comparator circuit in U650 detects when the ramp crosses a predefined threshold voltage (approximately +3 V). When the threshold is reached, pin 10 of U650 (HRR) goes LO and the integrating capacitor is discharged. At that same time, an internal counter that keeps track of the holdoff ramp cycles is incremented. The ramps continue to be generated and reset until the holdoff ramp counter has counted the number of ramp cycles defined by the sweep-rate-dependent holdoff data field stored in the Display Sequencer control register. At all sweep speeds except 5 ns per division, the count is at least two holdoff ramp cycles. The front-panel variable HOLDOFF control affects holdoff time by varying the HOLDOFF control voltage to U165C (from the DAC), changing the charging rate of integrating capacitor C660.

When holdoff time requirements are met (determined by the number of ramps counted), the Display Sequencer sets the THO (trigger holdoff) signal LO. This enables both the A Sweep hybrid (U700) and the A Trigger circuitry in U500. The Trigger circuit begins monitoring the selected trigger source line and, when a triggering event is detected that meets the triggering requirements defined by the stored control data, initiates the A Sweep and sets the $\overline{\text{TSA}}$ (trigger status, A Sweep) line to Display Sequencer U650 LO (indicating that the A Sweep has been triggered).

As the A Sweep circuit (U700) responds to the trigger, it sets the $\overline{\text{SGA}}$ (sweep gate A) line LO (via U980A) indicating that an A Sweep is in progress. After the sweep has run to completion, U700 sets the $\overline{\text{SGA}}$ line HI signaling the end of sweep. The Display Sequencer then sets the THO line HI, resetting the A/B Trigger hybrid U500 and A Sweep hybrid U700 in preparation for the next sweep.

DELAY GATE OPERATION. Analog Switches U850B and U850C select the delay references for each sweep. Depending on the display mode and point in the display sequence, the $\overline{\text{DS}}$ control signal (U650 pin 40) routes one of the two analog delay references through U850B and U850C to the two sweep hybrids. The selected reference level is compared against the changing sweep ramp voltages to generate the delay gates that control each sweep's functions.

After an A Sweep has been initiated by a trigger, a delay gate circuit within U700 compares the A Sweep ramp voltage to the selected delay reference. When the sweep ramp reaches the delay reference level, the $\overline{\text{DG}}$ (delay gate) output goes LO, enabling the B trigger portion of U500 and B Sweep hybrid U900. Then, when B triggering occurs (for TRIG AFT DLY mode), the A/B Trigger hybrid sets the $\overline{\text{TGB}}$ (trigger gate B) signal LO, initiating the B Sweep. In RUN AFT DLY mode, however, the $\overline{\text{TGB}}$ signal to U900 is held LO, and the B Sweep is initiated at the end of the A Sweep delay time when the A Sweep delay gate goes LO.

STATUS MONITORING. As the Display Sequencer controls the display system in real time, it continually monitors the trigger and sweep operations and updates the internal trigger status register accordingly. The Microprocessor checks the contents of this register every 3.3 ms to determine the current status of the trigger and sweep circuitry. The Microprocessor reads the trigger status register by generating a series of trigger status strobe (TSS) pulses (U650 pin 19) to serially clock the contents of the register out to the TSO (trigger status output) line and onto the Data Bus (via Status Buffer U2108 on diagram 2). The system status information obtained by this check is used for AUTO LVL triggering, AUTO free-run triggering, detecting the completion of all the sweeps in a SGL SEQ display, and during instrument calibration.

INTENSITY CONTROL. The Display Sequencer controls the intensity for both sweep and readout displays. The analog levels at pins 22 and 23 (set by the front-panel INTENSITY and READOUT INTENSITY controls) determine the basic intensity level of the displays. Two internally generated DAC currents (developed by multiplying the IREF current at pin 20 by two processor-generated numbers stored internally) are added to the basic intensity level currents to produce the display intensity seen on the crt (see Table 3-1). The two DAC currents added to the INTENSITY current are dependent on sweep speed, number of channels being displayed, and whether or not the X10 MAG feature is in use. These added currents increase crt beam current and hold the display intensity somewhat constant under the varying display conditions. The resulting current is applied to Z-Axis Amplifier U950 (diagram 6) from the BRIGHT output of the Display Sequencer (pin 21).

To produce the intensified zone on the A Sweep trace for A intensified by B Sweep displays, an additional current is added to the crt drive signal by the Z-Axis Amplifier during the concurrence of the $\overline{\text{SGAZ}}$ and $\overline{\text{SGBZ}}$ (sweep gate A and B z-axis) signals.

Table 3-1

Intensity Control

Type of Display	Horizontal Selects		Resulting Current at BRIGHT Output
	$\overline{HSA}$	$\overline{HSB}$	
X/Y	LO	LO	DI (display intensity) only
A Sweep	LO	HI	DI + A Swp DAC current
B Sweep	HI	LO	DI + B Swp DAC current
Readout	HI	HI	ROI (readout intensity) only

The readout intensity (ROI) level, controlled from the front-panel READOUT INTENSITY pot, is conditioned by U350A and associated components. Operational Amplifier U350A, configured as a full-wave rectifier, increases readout intensity when the pot is rotated either direction from center. Resistor R360 sets the minimum readout intensity current that occurs at the midpoint of the READOUT INTENSITY pot rotation.

Readout On-Off Comparator U350B detects to which side of center the READOUT INTENSITY control is set. The Microprocessor reads the output of omparator U350B via Status Buffer U2108 (diagram 2) at regular intervals. Depending on the status received, the processor sets up the Readout circuitry (diagram 7) to display either all of the readout information or just the "delta type" readouts.

Blanking of the crt display during CHOP VERTICAL MODE displays or when switching between dot positions in the readout displays is controlled by the Display Sequencer's BLANK output (pin 3). When the signal is LO, the crt z-axis is turned on to the selected intensity level; when HI, the crt display is blanked.

READOUT CONTROL. Readout displays are controlled by the readout request ($\overline{ROR}$) signal, the readout active ($\overline{ROA}$) signal, and the readout blank ($\overline{ROB}$) signal. During the first part of the holdoff time, up until one or two holdoff ramps before holdoff time ends (dependent on the sweep rate), the Display Sequencer sets the $\overline{ROA}$ signal line LO. While the $\overline{ROA}$ line is LO, the Readout circuitry may display readout character dots if necessary. During readout displays, the horizontal and vertical select signals ($\overline{HSA}$, $\overline{HSB}$, $\overline{VS1}$, $\overline{VS2}$, $\overline{VS3}$, and $\overline{VS4}$) are all set HI. This deselects the waveform-related sweep and deflection signals and gives display control to the Readout circuitry. While readout information or cursors are being displayed, the BLANK output signal (pin 3) is controlled by the readout blank ($\overline{ROB}$) signal from the Readout circuitry, and the readout intensity (ROI) signal (pin 23) controls the BRIGHT output level.

During holdoff, the Display Sequencer always sets the readout active ($\overline{ROA}$) line LO. As previously described, setting the $\overline{ROA}$ signal LO allows the Readout circuitry to display readout dots. In some settings of the SEC/DIV switch, with adequate trigger rates, holdoff time is provided for the Readout circuitry to display all the readout information without causing noticeable display flicker.

In those cases where the holdoff time is insufficient to prevent flicker, a portion of the Readout circuitry will request display control by setting the readout request ($\overline{ROR}$) signal LO. The Display Sequencer recognizes all readout requests immediately and switches the horizontal and vertical select lines to the readout display mode. The Readout circuitry displays one readout dot and then resets the readout request HI to switch back to the display of waveforms. Readout requests occur as required during sweep times to keep the readout display caught up. (See "Readout" description for further information).

TRACE SEPARATION. The TRACE SEP feature is used to position the alternate B Delayed Sweep trace downward from the A Sweep when Alternate Horizontal Display Mode (TURN-ALT) is active. It is also used when either the Δt or $1/\Delta t$ measurement function is used with B Sweep only displays. In the latter case, the TRACE SEP control vertically positions the trace(s) associated with the Δ control.

When the Display Sequencer determines that trace separation should be active, the LO TSIN level at pin 7 is routed to pins 9 and 8, the TS1 and TS2 outputs (connected together). This LO output turns off transistor Q600 (diagram 6), thereby enabling the trace separation voltage from the front-panel TRACE SEP pot to be applied to pin 42 of Vertical Output Amplifier U600. To disable the trace separation function, the Display Sequencer sets the TS1 + TS2 control line HI, turning on Q600 and shunting the trace separation signal to ground.

X10 MAG SELECT. The MAG (sweep magnifier) output (pin 39) drives the magnifier control input (pin 14) of Horizontal Output hybrid U800 and the select input (pin 9) of analog switch U860C (diagram 6). Analog switch U860C routes a magnifier gain-control voltage to the Horizontal Amplifier to set the horizontal gain for the X10 magnified displays.

CH 2 DELAY OFFSET. The $\overline{VS2}$ (vertical select, channel 2) output applied to analog switch U860B at pin 10 routes a calibrated offset voltage from sample-and-hold buffer U165D to both sweep hybrids when the Channel 2 vertical signal is being displayed. The offset voltage is used to eliminate the apparent propagation delay between the Channel 2 and the Channel 1 (or CH 2 and either one of the other channels). A step in the calibration procedure allows use of the front-panel Channel 2 Delay Offset feature to be either enabled or disabled. When enabled, the Channel 2 offset may be adjusted up to ±500 ps (with respect to Channel 1) using the Δ control.

CALIBRATOR TIMING. The Calibrator timing signal (CT) from the Display Sequencer is generated by an internal counter. The counter divides the 5-MHz clock input at pin TC (timing clock) by a value that is a function of sweep speed. The resulting square-wave output signal drives the Calibrator circuit. For ease of sweep rate verification, the Calibrator signal provides a display of five complete cycles on the crt at sweep speeds from 100 ms per division to 0.1 μs per division. Below 100 ms per division, the Calibrator output frequency remains at 5 Hz; and above 0.1 μs per division, the Calibrator frequency remains at 5 MHz.

When chopping between vertical channels, the Display Sequencer adds a 200-ns skew at the end of some sweeps to desynchronize the chop frequency from the sweep speed (to prevent the sweep from locking onto the chop frequency). Due to this, the Calibrator signal has an irregular pulse repetition characteristic between sweeps. This will not be apparent when observing the Calibrator signal on the crt of the 2465 since the skew is synchronized to the sweep, but may be observed when the Calibrator output signal is used with other instrumentation. The skew can be eliminated by setting the 2465 to SGL SEQ Mode (to shut off the sweeps).

A/B Trigger

The A/B Trigger hybrid (U500) and associated circuitry select the triggering signal source for each horizontal sweep as directed by the Display Sequencer. When the proper triggering criteria to initiate a sweep are detected, a triggering gate signal is produced to start the selected sweep.

Control data from the processor defining trigger mode, coupling, and slope parameters for each trigger is clocked into two storage registers internal to U500 for the A TRIG CLK signal on pin 23 ($\overline{CCA}$) and the B TRIG CLK signal on pin 47 ($\overline{CCB}$). The Display Sequencer selects the A trigger source with the $\overline{SR0A}$, $\overline{SR1A}$, and $\overline{SR2A}$ signal lines; the B trigger source is selected using the $\overline{SR0B}$, $\overline{SR1B}$, and $\overline{SR2B}$ signal lines. Table 3-2 illustrates trigger source selection.

Table 3-2

Trigger Source Selection

Select Inputs			Trigger Source
$\overline{SR2A(B)}$	$\overline{SR1A(B)}$	$\overline{SR0A(B)}$	
H	H	L	CH 1
H	L	H	CH 2
H	L	L	ADD
L	H	L	CH 3
L	L	H	CH 4
H	H	H	LINE (or BWLB[a])

[a]During calibration routines from the Diagnostic Monitor.

To initiate the A Sweep, the trigger hybrid compares the selected signal to the analog trigger level input at pin 13, TLA (trigger level A). B trigger signals are compared to the TLG (trigger level B) signal at pin 37 when triggered B Sweeps are required. When the proper trigger signal is detected, U500 outputs a trigger gate ($\overline{TGA}$ or $\overline{TGB}$) to the appropriate sweep circuit to initiate that sweep.

When an A Sweep is initiated, the trigger-status line ($\overline{TSA}$) (trigger status A, U500 pin 20) goes LO to signal the Display sequencer that a trigger has occurred. Until the sweep is completed, the $\overline{TGA}$ signal on pin 18 (or $\overline{TGB}$ signal on pin 42 for B Sweeps) remains LO. After the A Sweep is completed, the A Sweep Gate ($\overline{SGA}$) from A Sweep hybrid U700 (via U980A) will go HI, causing the Display Sequencer to set its THO (trigger holdoff) line (pin 13) HI. This resets the sweep hybrid and the trigger hybrid in preparation for the next trigger event.

The B Trigger Holdoff input (THOB, U500 pin 39) is held HI (keeping the B Trigger reset) until the A Sweep Delay Gate ($\overline{DG}$, U700 pin 41) goes LO (see the following A Sweep description). When $\overline{DG}$ goes LO, the B Trigger portion of U500 is enabled. The B Sweep Trigger functions in a manner similar to that of the A Sweep Trigger just described.

A Sweep

When properly triggered, the A Sweep circuit generates linear sweep ramps of selectable slopes. When amplified, these ramp signals horizontally sweep the crt beam across the face of the crt. The A Sweep circuitry consists of U700,

Q709, Q741, U860A, U910B, U980A, and associated components.

The A Sweep ramp signal is derived by charging one of several selectable capacitors from a programmable constant-current source. Capacitor selection depends on the sweep-rate-dependent control data (CD) on pin 29 that is clocked into A Sweep hybrid U700 by the A SWP CLK on pin 28 ($\overline{CC}$). This sweep-rate data causes some internal logic to select either hybrid-mounted capacitors CT0 or CT1 or capacitor C708 at the CT2 (timing capacitor two) pin. An additional capacitor, C709, may be selected (via Q709) if the control data asserts the TCS (timing capacitor select) signal on pin 9. TCS will be HI for A Sweep speeds slower than 1 ms per division. Capacitor C707 and associated circuitry form a linearity compensation circuit.

The constant current to charge the selected capacitor is derived from the DAC-controlled voltage, A TIM REF (A timing reference), generated on the Control Board. The ITREF input (U700 pin 24) is held at zero volts by an internal programmable current-mirror circuit at that input (see Figure 3-6). The A TIM REF voltage is applied to the current mirror via series resistors R723 and R724 to establish the input reference current (ITREF). The output of this current mirror is related to the input reference current by a multiple "M" that is set by a control data field stored in the internal control register of U700. The derived output current (M x ITREF) is connected to another programmable current-mirror circuit, U910B, external to the hybrid. The output of U910B provides the actual charging current and is a control-data-selected multiple of the M x ITREF current.

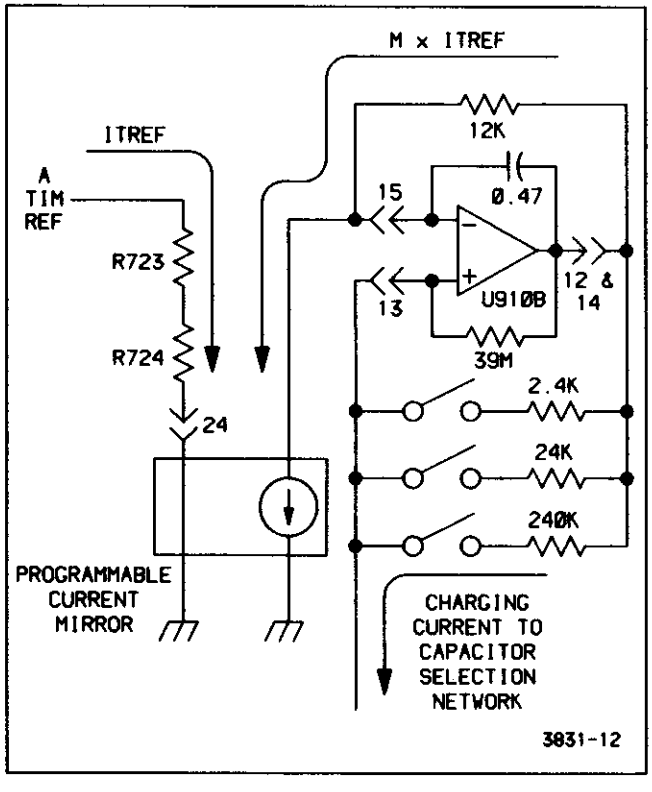

Figure 3-6. Sweep generator.

At the time of calibration, the processor will vary the ITREF input current until the slope of the output ramp for specific current-mirror/timing capacitor combinations is precisely set. The values of A TIM REF at these settings allow the processor to precisely calculate the characteristics of the current-mirror circuits at their various multiplication factors and the charging characteristics of the timing capacitors. These values are stored as calibration constants in nonvolatile memory (EAROM U2008, diagram 2).

Once the calibration constants are set, any setting of the SEC/DIV switch causes the Microprocessor to recall the associated calibration constants from the EAROM. The processor then calculates the proper value of A TIM REF based on the selected timing capacitor and the current-mirror multiplication factors.

If the SEC/DIV VAR control is out of the calibrated detent position, the processor will decrease the A TIM REF voltage from the maximum, in-detent value by an amount proportional to the position setting of the VAR control. At the maximum, fully counterclockwise setting of the VAR control, the ITREF current is one-third that of the normal, in-detent current.

For A Sweep hybrid U700 to initiate a sweep at the selected rate, the $\overline{AUXTRIG}$ (auxiliary trigger) input (pin 3), the THO (trigger holdoff) line from the Display Sequencer (on pin 1), and the $\overline{TRIG}$ (trigger) line from the trigger hybrid (on pin 2) must all be LO. With these three inputs LO, the A SWEEP ramp begins, and the sweep gate ($\overline{SG}$) output (pin 45) goes LO. The buffered sweep gate signal ($\overline{SGA}$) at the output of U980A returns to the Display Sequencer through R981 to indicate that the A Sweep is active. The sweep gate signal is used by various other circuits for their timing activities and is held LO until the A SWEEP ramp ends. The buffered (negative) sweep gate is inverted and routed to the rear-panel A GATE output connector via U975B.

Analog switch U860A and associated components form a switchable charging network that permits delaying the timing of end-of-A-Sweep gate signal ($\overline{SGAZ}$) for B Sweep displays. For normal A Sweep operation with the $\overline{HSA}$ signal LO, the $\overline{SGAZ}$ signal will end quickly, since the capacitance associated with Z-Axis hybrid U950 input

(diagram 6) will be charged positively through both R753 and R754. For B Sweep operation ($\overline{HSA}$ is HI), the end of the $\overline{SGAZ}$ gate signal will be delayed slightly (with respect to the normal sweep gate) since charging of the Z-Axis input capacitance will be at a slower rate through R754 only. This allows more of the B Sweep to be displayed than would otherwise be possible.

The A Sweep Delay Gate ($\overline{DG}$) signal acts as the trigger holdoff (THO) signal for the B Sweep and the B Trigger circuitry. It is generated by comparing the A SWEEP ramp voltage to the selected delay reference (DR) level from analog switch U850C. As the ramp voltage crosses the delay reference level, the delay gate ($\overline{DG}$) output signal goes LO, removing the HI THO level to the B Sweep. This enables the B Sweep to run immediately in RUN AFT DLY B Trigger Mode or, when in TRIG AFT DLY B Trigger Mode, enables the B Sweep to run when a triggering event occurs.

The BDCA (A Sweep bypass-delay comparator) input (pin 39) is a data bit from Auxiliary Control Register U140 (diagram 4) that, when HI, sets the A Sweep $\overline{DG}$ output LO at the beginning of the A Sweep. This enables the B Sweep to run immediately at the start of the A Sweep and is used for calibration purposes and for options.

The capacitive load (part of the etched-circuit board) at the RDA (retrace delay adjust) input (pin 4) is used to delay the retrace of the sweep until the Z-Axis drive is fully turned off in response to the $\overline{SGAZ}$ gate going HI. This delay prevents any part of the retrace from being seen.

B Sweep

Operation of B Sweep hybrid U900 is similar to that just described for the A Sweep with the following exceptions: The THO input (and thus sweep enabling) is controlled by the A Sweep hybrid and not the Display Sequencer (see the preceding A Sweep description). The timing capacitor select output, TCS, is not used, and only three timing capacitors are selectable (two on the B Sweep hybrid at CT0 and CT1 and one externally at CT2). Unlike the A Sweep, the delay reference (DR) input (pin 37) and the B Sweep bypass-delay comparator signal (BDCB) input (at pin 39) are used only for factory calibration.

Calibrator

The Calibrator circuit, composed of Q550, U165B, U550A, B, C, and D, and associated components, generates a square-wave output of precise amplitude and frequency characteristics. The CALIBRATOR signal provided at the front-panel output connector is useful for adjusting probe compensation and verifying VOLTS/DIV, SEC/DIV, and Δt (delta time) calibration. Output frequency is controlled by the Display Sequencer and is set to display five cycles across the ten crt graticule divisions at sweep speed settings from 100 ns per division to 100 ms per division. This feature allows quick and easy verification of the sweep rates. The Calibrator circuitry is essentially a voltage regulator that is alternately switched on and off, producing the square-wave output signal.

When the timing signal (CAL) from the Display Sequencer to the base of U550D is LO, U550C (configured as a diode) is forward biased, shunting bias current away from Q550, keeping it turned off. When transistor Q550 is off, the front-panel CAL OUT connector is pulled to ground potential through R558, setting the lower limit of the CALIBRATOR output signal.

As the CAL signal goes from LO to HI, the emitter of U550D is pulled HI to reverse bias U550C. Bias current for Q550 is established, and the transistor is turned on. The voltage at the emitter of Q550 rises to a level of +2.4 volts, determined by the voltage regulator composed of U165B, U550A, U550B, and associated components. This regulated level is applied to the front-panel CALIBRATOR connector through a voltage-divider network composed of R557 and R558. This produces an output voltage of 400 mV with an effective output impedance of 50 Ω.

Since the frequency of the CALIBRATOR signal is controlled by the same divider chain that controls operation of the vertical chopping rate, the intentional 200-ns shift added to the chop signal at the end of some sweeps (to desynchronize the chopping rate from the sweep rate) shows up on the CALIBRATOR signal as an irregular-width pulse. This shift is not apparent when viewing the CALIBRATOR signal on the instrument providing the signal (since the skew occurs during sweep-retrace time), but it should be taken into account when using the 2465 CALIBRATOR signal with other instrumentation. The skew can be eliminated from the signal by setting the 2465 TRIGGER MODE to SGL SEQ (to shut off the sweeps).

VERTICAL CHANNEL SWITCH AND OUTPUT AMPLIFIERS

The Vertical Channel Switch (diagram 6) selects the signal source for vertical deflection of the crt beam. The Vertical, Horizontal, and Z-Axis output amplifiers provide the signal amplification necessary to drive the crt.

Vertical Channel Switch

The Vertical Channel Switch circuitry consists of hybrid Channel Switch U400, that selects one of the vertical signals for application to the Vertical Output Amplifier,

and a combined switch/amplifier circuit that converts the single-ended readout vertical signal into a differential signal for application to the Channel Switch.

Channel selection is controlled by the Display Sequencer $\overline{VS1}$ through $\overline{VS4}$ signals applied to the vertical channel selection pins (pin 24, pin 25, pin 13, and pin 14 respectively). (See Table 3-3 for the Vertical Display Selection.) When a vertical select line is LO, the associated input signal pins are connected to the differential output (+OUT, pin 1 and −OUT, pin 3). The CH 5 input signal (Readout Vertical) is added to the output whenever both the $\overline{VS3}$ and $\overline{VS4}$ select signals are HI but will only contain readout information when the readout select logic (U970C and U975A) detects that the Display Sequencer has set both the Horizontal Select signals ($\overline{HSA}$ and $\overline{HSB}$) HI (readout selected).

Table 3-3

Vertical Display Selection

Select Inputs				Vertical Display
$\overline{VS1}$	$\overline{VS2}$	$\overline{VS3}$	$\overline{VS4}$	
L	H	H	H	CH 1
H	L	H	H	CH 2
L	L	H	H	ADD
H	H	L	L	CH 3
H	H	H	L	CH 4
H	H	H	H	Readout (Y)

READOUT SWITCH/AMPLIFIER. Transistors U485A, U485B, U485C, U485D, and U475C, along with their associated components, make up an analog switch circuit that routes either the readout vertical signal at the base of U485A or the ground reference at the base of U485C to the output at the emitter of U475C. The signal selected depends on the complementary voltages applied to the emitter junctions of the two emitter-coupled transistor pairs, U485A and B and U485C and D. The selection voltages are developed by voltage-divider networks on the complementary logic outputs of U975C and U975A.

When readout information is to be displayed, the horizontal select inputs to U980B and U980C go HI and the output of NAND-gate U975C goes LO. The LO applied to the divider network of R498, R484, and R471 pulls the anode of CR484 low enough to reverse bias it. This forward biases the emitter-coupled pair U485A and B via R483. NAND-gate U975A inverts the LO and applies a HI to the junction of R497 and R485. The HI forward biases CR485, and the emitters of U485C and D are pulled to a level in excess of +2 V, reverse biasing the transistor pair. With U485C and D reverse biased, the ground reference level at the base of U485C is isolated from the output, while the readout vertical information is allowed to pass through the forward-biased transistor pair.

When readout information is not being displayed, a HI is present at the output of NAND-gate U975C. The HI forward biases CR484 and, when inverted by U975A, reverse biases CR485. With the biasing conditions reversed, the transistor pair of U485C and D becomes forward biased and U485A and B become reverse biased. The ground reference level present at the base of U485C is coupled to the output, while the readout vertical signal is isolated.

The output signal (either the readout vertical signal or the ground reference level) is applied to the CH5+ input of Channel Switch U400 via R495 and R412. The inverting amplifier circuit composed of U475A, U475B, U475D, and associated components inverts the readout vertical signal for application to the CH5− input. The amplifier is an inverting unity-gain configuration with transistors U475A and U475B connected as an emitter-coupled pair. The base of U475A is referenced to ground through R482. The base of U475B is pulled to the same level by the negative feedback from emitter-follower U475D through R478. The noninverted signal applied is to the base of U475B through R492 and will attempt to increase or decrease the current to the base of U475B, depending on the amplitude and polarity of the signal. However, the negative feedback from the collector of U475B (via U475D and R478) will hold the base of U475B at the ground reference level. The feedback current through R478 develops a voltage drop across R478 that is equal in amplitude but opposite in polarity to the noninverted vertical readout signal. The inverted readout signal is applied to the Channel Switch on pin 2 (CH5−) via R476 and R402.

The RLC networks connected between the output pins of U400 are adjusted during calibration to obtain the correct overall high-frequency response of the vertical deflection system. The HF ADJ (high-frequency adjust) pot R417 and resistor R416 (connected to pin 16) trim the high-frequency response of the Channel Switch hybrid.

Delay Line

Vertical deflection signals from the Vertical Channel Switch are delayed approximately 78 ns by Delay Line DL100. This delay allows the Sweep and Z-Axis circuits to turn on before the triggering event begins vertical deflection of the crt beam, thereby permitting the operator to view the triggering event. The bridged-T network, composed of

inductors and capacitors built into the circuit board, corrects phase-distortion introduced by the delay line.

Vertical Output Amplifier

Vertical Output Amplifier U600 is a hybrid device that provides the final amplification of the selected vertical signal, raising it to the level required to drive the crt deflection plates. The vertical signal from the Delay Line is applied to pins 10 and 3 of U600. The RL network connected between pins 8 and 5 (COMPA and COMPB) of U600 compensates the signal for the skin-effect losses associated with the delay line.

Amplifier gain and vertical centering are adjusted by R638 and R639 respectively, primarily to match the amplifier hybrid to the crt installed in the instrument. An intensity-dependent correction current is sinked away from the vertical centering input at pin 39 by the Dynamic Centering circuit. The correction signal holds the vertical centering stable over a wide range of varying display intensity. Readout jitter adjustment pot R618 is used to minimize thermal distortion in the output amplifier to reduce jitter in the display readout.

The vertical output signal at pins 28 and 33 of U600 (OUT A and OUT B) is applied to the vertical deflection plates of the crt (diagram 8) via L628 and L633. The deflection plates form a distributed-deflection structure that is terminated by a hybrid resistor network. One element of the terminating network is an adjustment potentiometer used to match the network impedance to that of the crt.

BANDWIDTH LIMITING. Bandwidth-limiting coils L644 and L619, along with capacitors built into U600, form a three-pole filter used to roll off high-frequency response of the Vertical Output amplifier above 20 MHz. To limit the vertical bandwidth, the BWL (bandwidth limit) input to U600 (pin 16) is pulled LO. It may be set LO either by the BWL control data bit from Auxiliary Control Register U140 (diagram 4) when the operator selects the Bandwidth Limit feature or automatically by the output of NAND-gate U975A in the Vertical Channel Switch circuitry (via CR616) when the readout is being displayed.

TRACE SEPARATION. The voltage applied to the TS (trace separation) input of U600 (pin 42) is used to offset the output levels of the hybrid to vertically shift the position of trace on the crt. During normal sweep displays, the TS1 + TS2 signal applied to the base of Q600 by the Display Sequencer (diagram 5) is HI, and the transistor is turned on. The TRACE SEP level at the junction of R642 and CR600 is shunted to ground, and no offsetting of the output signal will occur. For those displays in which trace separation should occur, the Display Sequencer switches the base of Q600 to ground level to turn off the transistor. The trace separation level set by front-panel TRACE SEP control R3190 is now applied to the TS input of U600, and a corresponding offset of the displayed trace will occur.

BEAM FIND. As an aid in locating off-screen or overscanned displays, the 2465 is provided with a beam-finding feature. When the front-panel BEAM FIND button is pushed, the beam-find input pin (BF, pin 15) of U600 will be pulled HI. While BF is HI, the dynamic range of Vertical Output Amplifier U600 is reduced, and all deflected traces will be held to within the vertical limits of the crt graticule.

OUTPUT PROTECTION CIRCUIT. A current-limit circuit composed of transistors Q623 and Q624 protects the Vertical Output Amplifier from a short-circuited output or a bias-loss condition. Either of these fault conditions will cause excessive current to flow into pins 30 and 31 of U600. Current in FET Q624 is limited to the IDSS current, so the voltage at pins 24, 30, and 31 will drop. This decreases the forward bias on pass-transistor Q623 and lowers the voltage at pin 23 of U600 enough and provides some degree of protection for the device.

Horizontal Amplifier

The Horizontal Amplifier circuitry consists of Horizontal Output Amplifier U800, a unity-gain buffer amplifier made up of the five transistors in U735, and associated components.

UNITY-GAIN BUFFER AMPLIFIER. The amplifier circuit composed of U735A, B, C, D, and E along with their associated components, form a unity-gain amplifier that buffers the ramp signal from A Sweep Generator U700 to the Horizontal Output Amplifier. Transistors U735C and D form a differential pair with the negative excursion of their emitters limited to −5 V (clamped by U735E). Negative feedback from the collector of U735C to its base is via emitter-followers U735A and B (in parallel) which drive to the A Sweep input (pin 18, A+) to Horizontal Output Amplifier U800.

HORIZONTAL OUTPUT AMPLIFIER. Integrated circuit U800 provides the final amplification of the selected horizontal-deflection signal required to drive the crt. One of the single-ended input signals applied to the four input pins is converted to a differential-output signal at the output pins of the amplifier. The four deflection signals to U800 are: the A Sweep (pin 18, A+), the B Sweep (pin 16, B+), the Readout Horizontal signal (pin 17, RO), and the Channel 1 signal (used for horizontal deflection of the X-Y displays) at pin 20, the X+ input pin. Signal selection is done by an internal channel switch and is controlled by the $\overline{\text{HSA}}$ (horizontal select A) and $\overline{\text{HSB}}$ (horizontal select B) signals from the Display Sequencer (see Table 3-4).

Table 3-4

Horizontal Display Selection

Control Level		Selected Signal
$\overline{HSA}$	$\overline{HSB}$	
H	H	Readout (X)
H	L	B Sweep Ramp
L	H	A Sweep Ramp
L	L	X Input (from CH 1)

Switching between unmagnified (X1) gain and magnified (X10 gain) is also controlled by signals from the Display Sequencer. For normal horizontal deflection, the $\overline{MAG}$ signal on pin 14 of U800 is HI, and the gain of the output amplifier produces normal sweep deflection. Precise X1 deflection gain is set by adjusting X1 Gain pot R860. When the X10 MAG feature is selected, amplifier gain for the magnified sweeps is increased by a factor of 10. The $\overline{MAG}$ signal from the Display Sequencer goes LO when magnified sweep is to be displayed. This switches the amplifier gain and switches analog switch U860C from the X1 position to the X10 position. Amplifier gain in the magnified mode is adjusted by adding or subtracting a small bias current using X10 Gain control R850. Dc offsets in the amplifier and crt are compensated for, using Horiz Centering pot R801 to precisely center the display. An intensity-dependent position correction signal, used to hold the horizontal centering stable over a wide range of varying display intensities, is added at this point by the Dynamic Centering circuitry.

Timing and linearity of the sweep is affected by the amplifier transient response; and Trans Resp pot R802, connected to pin 2, is adjusted during calibration for optimum accuracy of the high-speed sweeps.

As with the Vertical Output Amplifier, the Beam Find feature reduces the dynamic range of the Horizontal Output Amplifier. While the front-panel BEAM FIND button is pressed in, a HI is placed on U800 pin 15 via pull-up resistor R615, and the horizontal deflection is reduced, moving horizontally off-screen displays to within the graticule viewing area.

Z-Axis Amplifier

Z-Axis Amplifier U950 turns the crt beam off and on at the desired intensity levels as the oscilloscope goes through its display sequence. The BRIGHT (brightness) signal applied to U950 pin 44 from the Display Sequencer U650 (diagram 5) is amplified to the level required to drive the crt control grid (via the DC Restorer circuitry) and sets the crt beam intensity. The BLANK input signal applied to U950 pin 5, also from the Display Sequencer, blanks the trace during sweep retrace, chop switching, and readout blanking by reducing the VZOUT signal to a blanked level. Sweep gate z-axis signals ($\overline{SGAZ}$ and $\overline{SGBZ}$) from the A Sweep and B Sweep hybrids (U700 and U900 respectively, diagram 5) are applied to the Z-Axis Amplifier on pins 4 and 5. These signals turn the beam current on and off for the related displays and, when used in conjunction with the BLANK signal on pin 5, enable the sweeps to be blanked while still allowing the Readout circuitry to blank and unblank the crt for the readout displays.

Control signals applied to U950 pin 48, pin 2, and pin 1 ($\overline{HSA}$, $\overline{HSB}$, and TXY respectively) switch some internal logic circuitry to enable or disable different input signals for the various types of displays. Table 3-5 illustrates the effects of the various input signals on the output signal for different combinations of $\overline{HSA}$, $\overline{HSB}$, and TXY.

The Z-Axis hybrid has an internal limiter circuit that prevents the crt from being damaged during high-intensity, high-repetition-rate displays. For high-rep-rate displays, capacitor C956 is shunted to ground via U850A. A signal representative of the intensity setting and the sweep repetition rate is integrated on C957 and results in a control level at pin 7 of U950 used to limit intensity of the crt beam. For the slower repetition rate displays, the SIL bit (slow intensity limit) from Auxiliary Control Register U140 (diagram 4) opens CMOS switch U850A, gently reducing the effective capacitance at pin 7. In this slow-sweep mode, limiting depends primarily on the intensity setting.

Focus tracking for intensity (VZOUT) level changes is provided by the VQOUT (quadrapole output voltage) signal at pin 22 of U950. The VQOUT signal varies the focusing voltages (and thus the focusing strenth) of two quadrapole lenses in the crt (diagram 8). The VQOUT signal is related to the VZOUT level exponentially and provides the greatest auto-focus control at high-intensity levels. Gain of the VQOUT signal is set by the High-Drive Focus adjustment, R1842. The VQOUT signal also drives the Dynamic Centering circuit and holds the display position stable during wide-range intensity level changes.

Transient response of the Z-Axis Amplifier is adjusted by potentiometer R1834, connected to U950 at pin 13.

Dynamic Centering

The circuit composed of U3401, U3402, and associated components generates compensating signals to offset positioning effects that occur in the crt when the intensity

Table 3-5

Blanking and Intensity Control Selection

Control Inputs			Intensity Affected By	Blanking Affected By	Typical Display
TXY	$\overline{HSA}$	$\overline{HSB}$			
X[a]	H	H	BRIGHT (RO level)	BLANK	Readout
X	H	L	BRIGHT, Z EXT	BLANK, $\overline{SGAZ}$, $\overline{SGBZ}$	Delayed Sweep
X	L	H	BRIGHT, $\overline{SGBZ}$, Z EXT	BLANK, $\overline{SGAZ}$	Main Sweep
L	L	L	BRIGHT, $\overline{SGBZ}$, Z EXT	BLANK	X-Y
H	L	L	BRIGHT, $\overline{SGBZ}$, Z EXT	BLANK, $\overline{SGAZ}$	X-Y

[a]X = State doesn't matter.

is varied over a wide range. The VQOUT signal from Z-Axis Amplifier U950 is exponentially proportional to the display intensity and dynamically controls the intensity-dependent offsets.

Dynamic Centering adjustment pots R3401 and R3407 set the gain and polarity of the signals at their related outputs by varying the current in the emitter circuit of one of two emitter-coupled pairs of transistors. Adjusting the bias level at pin 4 above ≅ −10.6 volts (determined by R3410 and R3411 at the complementary input, pin 1) will generate an inverted signal, while adjusting the bias level below −10.6 volts will cause a noninverted signal. Amplitude of the resulting signal is dependent on how far from the −10.6-volt reference the bias is set. The output signal is added or subtracted from the position voltage applied to the Vertical and Horizontal Output Amplifiers. Both pots are adjusted so that position shifts due to display intensity variations are minimized.

READOUT

The Readout circuitry (diagram 7) is responsible for displaying the alphanumeric readout characters on the crt. An eight-bit character code specifying each character (or cursor segment) to be displayed is written from the Microprocessor to a corresponding location in the Character RAM U2920 (a 128-x-8-bit, random-access memory integrated circuit). Each of the lower 64 locations in the RAM corresponds to one of the 64 possible character locations in the crt readout display (see Figure 3-7); 32 locations in the upper graticule row and 32 in the lower graticule row. The upper 64 RAM locations are used to store cursor segment information for the display of the ΔV and Δt measurement cursors. The eight-bit character code written to each location in RAM points to a block of addresses in Character ROM U2930. This block in the ROM contains the dot-position information for the specific character to be displayed at the associated crt position.

Each character is made up of zero (for a space character) or more dots displayed in an eight-wide by sixteen-high dot matrix. Specific blocks of ROM addresses contain all the X-Y offset coordinates for the dots in a particular character in the readout. The coordinates are referenced to the lower-left corner of the character dot matrix. Each individual data byte in the block of ROM addresses contains both the X and the Y coordinates for one dot of the associated character.

To display a character, a combination of the character position on the crt (the RAM address) and the byte of X-Y position data from Character ROM U2930 (relative to that character position) is appled to Horizontal and Vertical DAC (digital-to-analog converters) circuits, U2910 and U2905 respectively. In these circuits, the X-Y position data is converted to analog deflection signals used to position each dot in the crt readout display. Each of the position bytes are read from the block of ROM defining the character under control of the readout timing and sequencing circuitry. The resulting dots, when displayed in sequence, form the character at the proper location on the crt.

Readout I/O

The Readout I/O circuitry, composed of U2860, U2865, U2960, and associated components, provides the interface between the Microprocessor and the Readout board. Two types of data, Readout mode data and character data, are written to the Readout board serially via data bus line BD0.

STORING A CHARACTER. Displaying a character starts with serially clocking 15 of the 16 character data bits into a 16-bit shift register formed by registers U2960 and U2860. The $\overline{ROS1}$ strobe (readout strobe one) from the Address Decode circuitry (diagram 1) is the clocking signal. The first eight bits of the loaded data indicate the character to be displayed, while the last seven bits select the location on the crt that the character is to be displayed.

On positive-going transitions of the $\overline{ROS1}$ strobe, the data bit present on the BD0 data line is shifted into the first latch of character address register U2960. The following negative-going edges of the $\overline{ROS1}$ strobe are inverted by U2965A to produce a positive transition that shifts the data bit present at U2960 pin 9 (Q_{SH}) into U2860. After 15 $\overline{ROS1}$ strobes have occurred, seven bits of character data are latched into U2860, and the eighth character bit and seven of the character address bits are latched into character address register U2960 (though they have not been shifted into their correct positions for addressing the RAM).

At this point, the last character bit remains to be shifted into the registers, but the operating mode must be set up first to ensure correct operation upon shifting the final bit. The eight bits of mode data are shifted into the mode control register U2865 by the $\overline{ROS2}$ strobe. Bit Q_4 ($\overline{WRITE}$), along with the $\overline{ROS2}$ and the R/$\overline{W}$ Dlyd signal

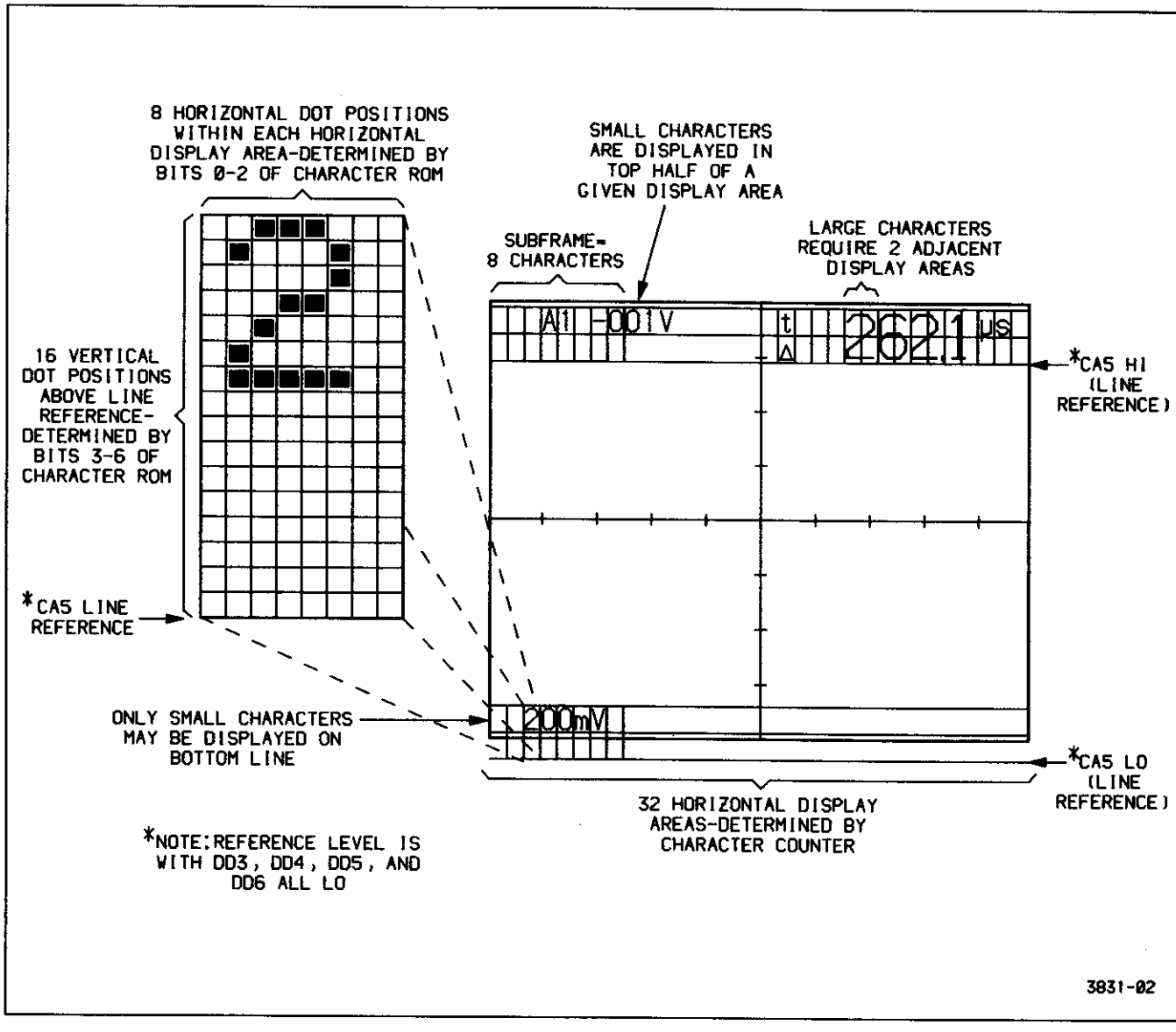

Figure 3-7. Developing the readout display.

are applied to the RAM enabling circuitry and determine when new character information will be written into the Character RAM. With U2865 loaded with the mode data, a final $\overline{ROS1}$ strobe clocks the eighth bit of character data from U2960 to U2860 on the negative edge, and the positive edge of the strobe clocks the eighth character address bit (an unused bit) into U2960.

With control bit Q_4 from U2865 LO, the outputs of U2860 are enabled and the eight bits of character data (CD0 through CD7) are written in parallel into the Character RAM at the location selected by the seven-bit address from U2960. Register U2960 is enabled only when the Readout is not displaying characters (the REST signal at pin 15 of U2960 is HI).

The character data register U2860 also provides a means for the Microprocessor to read data from the Character RAM for partial verification of Readout circuit operation (during the power-up tests). The eight bits of parallel data from the Character RAM location selected by character address register U2960 are loaded into U2860 by setting bit Q_3 of mode control register U2865 LO. Inverter U2965C converts the LO to a HI and applies it to character register U2860 at pin 1. The HI on pin 1, in combination with the fixed HI on pin 19 of U2860, switches the character register to the Load mode. The next positive transition of the $\overline{ROS1}$ strobe loads the eight data bits placed on the CD0 through CD7 bus lines into the register in parallel. Bit Q_3 is then returned HI, and the next positive transition of the $\overline{ROS1}$ strobe shifts the Q_A bit to pin 8 (Q_A'), the RO DO (readout data out) line. Seven more $\overline{ROS1}$ strobes shift the remaining seven bits of character data out onto the RO DO line to Status Buffer U2108 (diagram 2) to be read, one at a time, by the processor.

Character RAM

Character RAM U2920 provides temporary storage of the readout character selection data. This character data is organized as 128 eight-bit words that define the character that should be displayed at any given readout position on the crt. Cursor information is also stored in U2920 when cursors are to be displayed.

RAM locations may be addressed either from the Readout I/O stage by character address register U2960, as previously described, or by the Character Counter stage. The lower 64 address locations in RAM each correspond to a specific readout location on the crt, while the upper 64 address locations store cursor information. The eight bits of data written to one of these locations from the Readout I/O stage is a code that identifies the specific character (or cursor segment) that should be displayed at the associated crt location. After the display data is written into the RAM, the Character Counter is allowed to address the RAM, incrementing through the RAM address field. The eight-bit character codes for each display location are output to Character ROM U2930 in sequence.

Character Counter

The Character Counter stage consists of two four-bit counters (U2940A and B) cascaded together to form an eight-bit counter (only seven of which are used) and tri-state buffer U2935 which drives the RAM address lines.

As the Character Counter addresses each RAM location, a sequence of "dot display cycles" is performed in which the individual dots that make up the character are positioned on the crt and turned on. The $\overline{EOCH}$ (end of character) signal applied to U2885A prevents the counter from incrementing until all dots of the character have been displayed. As the last dot of a character is addressed, the $\overline{EOCH}$ bit at pin 2 of U2855A goes LO. The next $\overline{GETDOT}$ pulse increments U2940B, and the next RAM location is addressed to start the display of the next character. Space characters have the $\overline{EOCH}$ bit set LO for the first "dot" of the character and merely advance the Counter to the next character address without displaying any dots. See the Character ROM description for further explanation of the $\overline{EOCH}$ bit.

Character ROM

Character ROM U2930 contains the horizontal and vertical dot-position information for all of the possible characters (or cursor segments) that may be displayed. The eight bits of character data from the Character RAM are applied to the eight most-significant address inputs (A4 through A11) of the Character ROM and select a block of dot-positioning data unique to the character to be displayed. The Dot Counter increments the four least-significant address lines (A0 through A3), causing the ROM to output a sequence of eight-bit words, each defining dot position for the selected character.

The three least-significant bits of a ROM dot-data word (DD0 through DD2) select one of eight horizontal positions for the dot within an eight-by-sixteen character matrix (see Figure 3-7). The next four bits (DD3 through DD6) define the vertical position of the dot within the matrix. These dot-data bits are applied to the Horizontal and Vertical Character DACs, where they are converted to the analog voltages used to position the dot on the crt.

The last dot-data bit DD7 is the $\overline{EOCH}$ (end of character) bit and, when LO, indicates that the last dot of the character is addressed. It is used to reset the Dot Counter (via U2855B) and enables the Character Counter to be incremented (via U2855A) after the last dot of a character has been displayed.

Two servicing jumpers, J401 and J402, have been provided to disable the Character ROM and force the DD7 bit ($\overline{EOCH}$) LO. In certain instances, these two conditions may be useful when troubleshooting the Readout circuitry. To prevent damage to the ROM output circuitry, J402 should only be installed after J401 is installed (to disable the ROM).

Dot Counter

The Dot Counter consists of two four-bit counters (U2870A and B), OR-gate U2835A, inverter U2980D, and inverting input AND-gate U2855B. It sequences through a block of addresses containing dot-position data for a selected character. The Dot Counter is incremented when a dot is finished (via Inverter U2980D) by the $\overline{GETDOT}$ signal from the Dot Cycle Generator.

The counter increments through the block of dot-position data until the last byte of the block is encountered (last dot). This last data byte has the $\overline{EOCH}$ (end of character) bit (DD7) set LO. The dot is positioned and displayed in the normal manner, but when the $\overline{GETDOT}$ signal occurs for the next dot display cycle, the $\overline{EOCH}$ bit is latched into U2905 and generates the $\overline{EOCH1}$ (end of character, delayed one dot) signal at U2905 pin 19. With $\overline{EOCH}$ and $\overline{EOCH1}$ both LO, the HI reset pulse produced at pin 4 of NOR-gate U2855B resets the counter and, except for space characters, the $\overline{EOCH}$ bit returns HI. As the reset is removed from the Dot Counter, it is reenabled for display of the next character. For space characters, the $\overline{EOCH}$ bit will be detected as a LO when the first dot is read from the Character ROM, and the Character Counter will advance to the next character on the next rising edge of $\overline{GETDOT}$.

Counter U2870A and OR-gate U2835A enable characters of more than 16 dots to be displayed. Since most of the readout characters are small, using 16 dots or less, efficient data storage is achieved by storing the dot-position data as 16 consecutive bytes. For displaying these smaller characters, the four bits from U2870B are sufficient to address the 16 possible dot-position bytes.

When larger characters (up to 32 dots) are to be displayed, an additional bit of counter data must be used to address the ROM. This fifth bit comes from U2870A pin 3 and is ORed by U2835A with bit CD0 from the Character RAM. The block address for these larger characters always has bit CD0 set LO, so the counter bit from U2870A pin 3 is in control of the ROM address line at pin 4 of U2930. When displaying these larger characters, the dot count goes beyond 16 dots before the $\overline{EOCH}$ bit is set LO. On the seventeenth character, the fifth counter bit (pin 3 of U2870A) will go HI to address the next 16-byte block of character data in ROM U2930. The lower four bits of the Dot Counter then sequence through this additional block in the normal manner until the $\overline{EOCH}$ bit is encountered, resetting the counter.

Horizontal DAC

The Horizontal DAC generates the voltages used to horizontally position dots of the readout display on the crt. Five data bits (CA0 through CA4) from the Character Counter stage position a character to the correct column in the display (32 possible columns across the crt), while three data bits from Character ROM U2930 (DD0 through DD2) horizontally position the dots within the eight-by-sixteen character matrix (see Figure 3-7).

The eight bits of position data are written to the permanently enabled DAC each time a new dot is requested by the Dot Cycle Generator. The $\overline{GETDOT}$ signal applied to pin 11 (Chip Select) enables the DAC to be written into, and the falling edge of the 5-MHz clock applied to pin 12 (Write) writes the data at the eight DAC input pins into an internal latch. The voltage at the DAC output pin changes to reflect the data present in the latch.

Vertical Character DAC

The function of Vertical Character DAC U2905 is similar to that of the Horizontal DAC just described. It is responsible for vertically positioning each character dot on the crt. The Vertical DAC circuit is made up of five, D-type flip-flops (contained within U2905) and an accompanying resistor weighting network. The outputs of the flip-flop source different amounts of current to a summing node through a resistor weighting network.

The five data bits are latched into U2905 on the rising edge of the $\overline{GETDOT}$ signal. One bit of character address data (CA5) from the Character Counter switches the vertical display position between the upper and lower readout display lines. When the display is to be in the bottom line, bit CA5 is set LO. With CA5 LO, zener diode VR2925 is biased off and a small current is sourced to the summing node via R2925. Vertical position above this reference is determined by dot data bits DD3 through DD6. When the top line is to be displayed, the CA5 bit is set HI, biasing VR2925 on. A larger current is now sourced into the summing node via R2925 and enough voltage is developed across R2926 to move the display to the top row of the crt. As before, the individual dots are then positioned above this reference level by dot data bits DD3 through DD6.

Mode Select Logic

The Mode Select Logic circuitry is composed of analog switches U2800 and U2805, buffers U2820A and B, gates U2810A, B, C, and D, U2900B and C, and part of U2905. It controls the readout display mode by selecting which deflection signals should drive the Horizontal and Vertical Deflection Amplifiers during a readout display. Five display modes are decoded by the Mode Select Logic: character display, vertical cursor 0, vertical cursor 1, horizontal cursor 0, and horizontal cursor 1.

For normal character displays, cursor select bit CA6 on U2800 pin 1 is LO. This LO signal passes through analog switch U2800 and is latched into U2905 when the $\overline{\text{GETDOT}}$ request from the Dot Cycle Generator goes HI. This latched LO selects the character display mode by forcing the outputs of U2900B and C and U2810A and B HI. The HI outputs of U2900B and C applied to the select input pins of analog switch U2805 cause the Horizontal DAC output signal applied to U2805 pin 11 to be routed to the Horizontal Amplifier (diagram 6) via buffer U2820B. The same HI logic levels cause NOR-gates U2810C and D to produce a LO at their outputs. This causes analog switch U2800 to route the Vertical DAC output signal applied to pin 12 to the Vertical Output Amplifier (also diagram 6) via buffer U2820A.

For cursor displays, cursor select bit CA6 goes HI. This HI is routed through analog switch U2800 and latched into U2905 when $\overline{\text{GETDOT}}$ next goes HI. This produces a HI at U2905 pin 5, enabling the Mode Select Logic to decode output bits DD3, DD4, and DD5 (from U2905) to determine which of the four possible cursor modes is selected (see Table 3-6). Once one of the cursor modes is entered, analog switch U2800 routes a fixed HI from pin 5, pin 2, or pin 4 to U2905 to keep the Mode Select Logic enabled. Character display mode is reentered only when return-to-character-mode data is decoded (DD4 and DD5 both LO). When that occurs, U2800 routes the CA6 bit to U2905 and, if the bit is LO, the cursor display mode is halted.

CURSOR DEVELOPMENT. Cursors are displayed in short sections, alternating between both vertical positions (for the delta voltage cursors) or both horizontal positions (for the delta time cursors). When displaying delta voltage cursors, the DLY REF 0 level is routed to the Vertical Amplifier by analog switch U2800. This level determines the vertical position of one of the voltage cursors. Horizontal-positioning voltages for one segment of the cursor are routed from Horizontal DAC through analog switch U2805 and buffer U2820B to horizontally position each of the dots making up the cursor segment. DLY REF 1 is then used to vertically position the second cursor, and the Horizontal DAC positions each of the dots for that cursor segment. The cycle is repeated until all segments of both cursors are displayed.

Delta time cursor displays are similar in that the DLY REF 0 and DLY REF 1 signals are used to position the cursors. In this case, however, analog switch U2805 selects the DLY REF 0 and DLY REF 1 signals alternately to position the cursors horizontally, and the Horizontal DAC output is routed via analog switch U2800 and buffer U2820A to vertically position the dots within each cursor segment.

Table 3-6

Readout Display Mode Selection

Control Bits				Mode Selected	Horizontal Signal	Vertical Signal
CA6 (Cursor Select)	DD5	DD4	DD3			
L	X[a]	X	X	Character Display	Horiz DAC	Vert DAC
H	L	H	L	Vert Cursor 1	Horiz DAC	DLY REF 1
H	L	H	H	Horiz Cursor 1	DLY REF 1	Horiz DAC
H	H	L	L	Vert Cursor 0	Horiz DAC	DLY REF 0
H	H	L	H	Horiz Cursor 0	DLY REF 0	Horiz DAC
H	L	L	X	Return to Character Display Mode		

[a]X = State doesn't matter.

Refresh Prioritizer

The Refresh Prioritizer circuitry consists of U2850A and B, U2950A, U2990A, and U2985. It keeps track of how well the Readout circuitry is doing in displaying all the required readout information and maintains the overall refresh rate. Since the readout display must remain flicker-free and at a constant intensity over the entire sweep rate range, various modes of displaying readout information are provided. The Refresh Prioritizer keeps track of the display status and enables the various readout-display modes as required to produce minimal interference with the displayed waveform trace(s).

Ideally, readout information should be displayed only when the oscilloscope is not trying to display waveform traces. These times occur before a trace commences, after a trace is completed, or between consecutive traces. Displaying in this mode corresponds to "priority one" in Figure 3-8 and causes no interference with the displayed waveforms. If the Readout circuitry is able to display all the required readout dots during the holdoff time between sweeps, the prioritizer U2985 will turn off the Dot Start Governor until the next subframe of readout information is to be displayed. When the sweep times are either too fast to finish a readout display during holdoff (at 5 ns per division no identifiable holdoff time exists) or too slow to allow flicker-free readout, readout display modes other than priority one are initiated.

The next most desirable time for dots to be displayed is during "triggerable" time; that time between sweeps when the oscilloscope is waiting for a sweep trigger event to occur. This is designated priority two and may cause slight interference on the leading edge of the displayed trace if a dot is being displayed when the actual trigger occurs.

Finally, the least desirable dot display time is during a waveform trace display. This display time is designated either priority three or priority four. (Priority four indicates a higher demand of display time.) In priorities three and four, dot displays occur during the main portion of the waveform display. However, the waveform blanking associated with these displays is relatively random in nature and is usually not noticeable.

To start a readout display, the ROSFRAME (readout subframe) request from the Timing Logic (diagram 1) clocks the Q output of flip-flop U2850A HI. ROSFRAME is a periodic clocking signal used to hold the overall refresh rate constant and occurs at regular intervals, regardless of the state of the display.

As the Dot Cycle Generator runs, it resets U2830B in the Dot Timer at somewhat irregular intervals with the STARTDOT signal (via inverter U2890A). The Dot Timer then starts a timing sequence, and the rising edge of the REFRESH signal from U2830A pin 4 clocks the latched ROSFRAME request from U2850A pin 5 to the Q output (pin 9) of flip-flop U2850B. This HI, applied to the S1 input (pin 10) of prioritizer U2985, sets it up to increment with the next REFRESH clock applied to its clock input (pin 11). The LO $\overline{Q}$ output of U2850B (pin 8) applied to the reset input of U2850A resets the latched ROSFRAME request. See Figure 3-9 for an illustration of the timing sequence involved.

The next REFRESH clock increments the display priority to one by clocking a HI to the Q_D output (pin 12) of prioritizer shift register U2985. (Table 3-7 illustrates the operation of U2985. The same clock latches the now LO ROSFRAME request at U2850B pin 12 to the Q output (pin 9), where it is applied to the S1 input (pin 10) of prioritizer U2985. The LO on the S1 input of the prioritizer will remain until another ROSFRAME request from the Timing Logic occurs, and the encoded priority at the output pins of U2985 will remain as it is presently set.

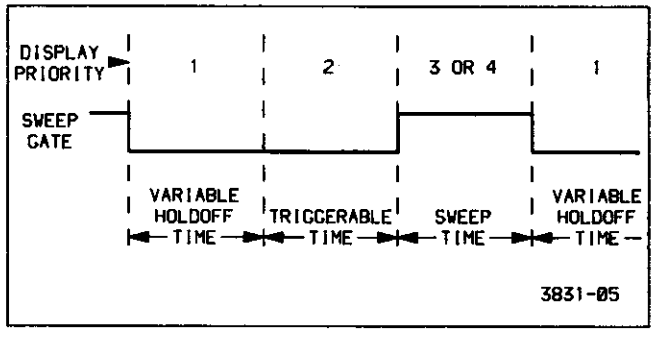

Figure 3-8. Readout display priorities.

Table 3-7

Operation of Prioritizer Shift Register

Select Inputs		Mode
S0	S1	
H	H	Parallel Load
H	L	L → Q_A (decrease priority)
L	H	H → Q_D (increase priority)
L	L	Hold Data

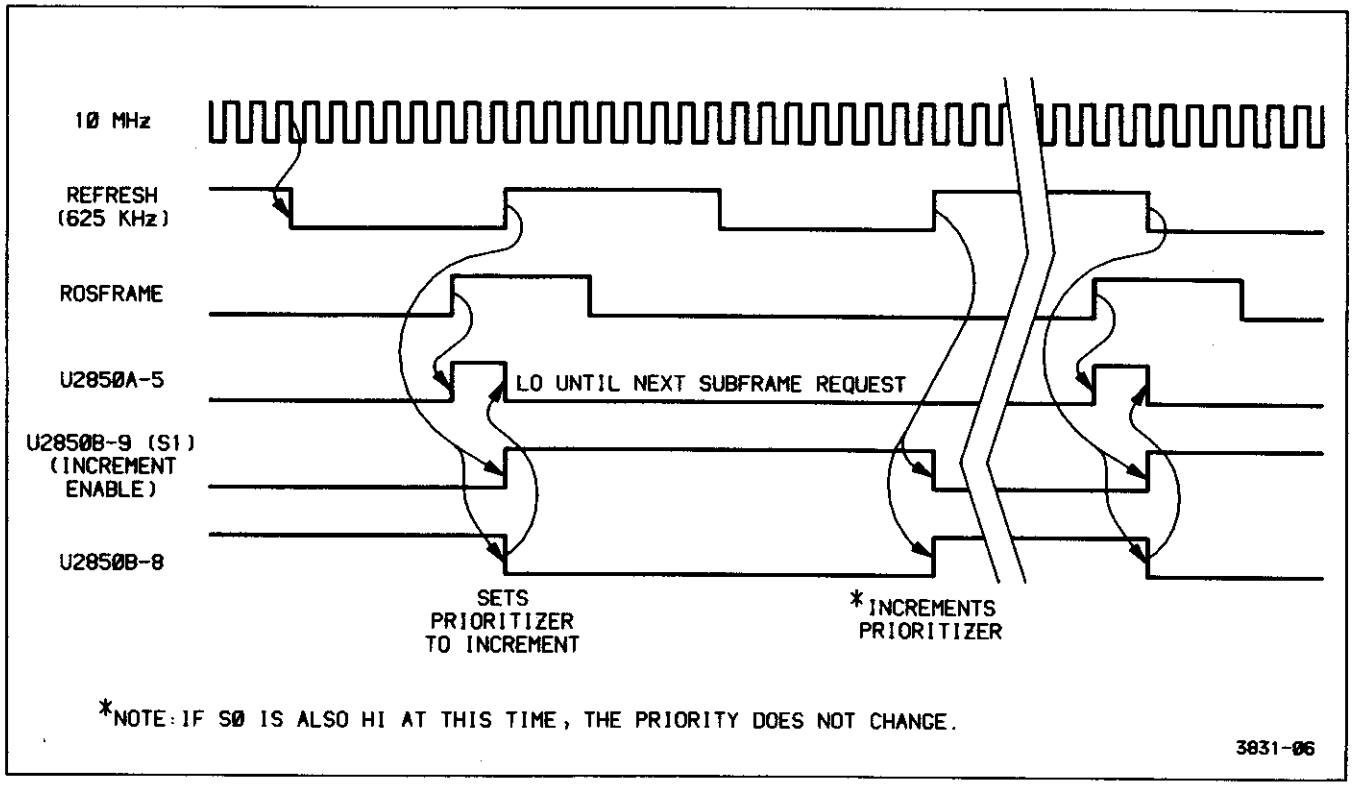

Figure 3-9. Timing of Refresh Prioritizer.

As each of the consecutive dots of the readout frame are displayed, the Dot and Character Counters increment until all dots of the subframe have been displayed (eight characters). As the Character Counter increments to address the next character of the display (first character of the next frame), the fourth bit of counter U2940B goes HI and sets the S0 input (pin 9) of prioritizer U2985 HI via exclusive-OR-gate U2990A. The Dot Timer then clocks the prioritizer with a REFRESH clock on pin 11 of U2985, and the priority is decremented back to zero (indicating that the subframe is completed). The next ROSFRAME request starts the process over again to display the next subframe of readout display. The sequence just described is the priority one display mode and is used when holdoff time between sweeps allows all dots of the subframe to be displayed before the next ROSFRAME request occurs.

If a second ROSFRAME request occurs before the Character Counter indicates the end of the subframe (to decrement the prioritizer back to zero), input S1 of U2985 will be set HI (while the S0 input pin remains LO) and the Prioritizer will increment to priority two (outputs Q_C and Q_D go HI) on the next STARTDOT cycle. If this display priority still is inadequate to complete the subframe display before the next ROSFRAME request occurs, priority two will be incremented up to priority three, or even to priority four should the condition persist. Priority four is operationally the same as priority three, but it is used to keep the readout circuitry continuously displaying readout data on through the next subframe, thus allowing the display to catch up. If priority four is in effect, the next decrement that occurs at the end of a subframe only returns the prioritizer to priority three, not to priority two.

The circuit composed of flip-flop U2950A and exclusive-OR-gate U2990A enables either edge of the CA3 bit to decrement the priority of the display when a subframe is completed. Either a negative or positive transition on pin 2 of U2990A will cause the output at pin 3 to go HI since the Q output of U2950A is still at the opposite level. The HI from U2990A indicates that the end of the present subframe has occurred, and it sets up the prioritizer to decrement with the next REFRESH clock. At the same time that the prioritizer decrements, the changed level of the CA3 bit is clocked through U2950A and causes the output of exclusive-OR-gate U2990A to return LO until the next subframe is completed.

If the subframe is completed (S0 on U2985 goes HI) when a ROSFRAME request is also pending (S1 is also HI), U2985 does a parallel load, reloading the present priority back into the prioritizer. Since, in this case, the subframe display was completed at the same rate as the ROSFRAME request occurred, the readout display priority is not changed.

Dot Start Governor

The Dot Start Governor detects the display priority from the Refresh Prioritizer and initiates dot-display cycles as the appropriate conditions are met. The conditions tested include display priority, sweep gate completion, dot completion, readout control status, and the readout active enable from the Display Sequencer.

When the readout board status line (ACTIVE/$\overline{\text{ADDRESSABLE}}$) is HI (signifying display) and the REST line goes HI to indicate that the dot cycle is complete, AND-gate U2970C generates a HI at pin 8 (DOTOK) to signal that a new dot display is allowed. The HI from U2970C enables most of the gating in the Dot Start Governor. If the Refresh Prioritizer has encoded a display priority of either one or two, the output of exclusive-OR-gate U2990B is HI. When DOTOK from U2970C goes HI to enable a dot display, the LO reset from pin 6 of U2970B to pin 1 of flip-flop U2880A is removed. Now, when the A Sweep gate ($\overline{\text{SGA}}$) goes HI (beginning of Holdoff), the HI at the D input of U2880A is clocked to the Q output and the $\overline{\text{Q}}$ output at pin 6 will go LO, requesting display of a priority one or two dot. This LO dot request is propagated through U2885B, U2890D, U2890B, and U2890C and sets the STARTDOT signal LO. STARTDOT going LO resets Dot Cycle Generator shift register U2995 and counter U2830B of the Dot Timer. Resetting the Dot Cycle Generator shift register causes the REST signal from U2995 pin 13 to go to a LO, removing the HI DOTOK signal at U2970C pin 8. As DOTOK goes LO, STARTDOT at pin 8 of U2890C goes HI to start the Dot Cycle Generator. At the same time the reset to U2880A is asserted via U2970B and the dot request is removed. Both the Dot Timer and the Dot Cycle Generator are now enabled and start the first dot-display cycle during holdoff time.

After the Display Sequencer U650 (diagram 5) has time to respond to the end of the sweep gate, it sets the readout active signal ($\overline{\text{ROA}}$) to pin 4 of U2880A LO. This sets pin 5 of U2855B LO, and the signal is propagated through U2855B, U2890D, U2890B, and U2890C, as before, resetting the Dot Timer and the Dot Cycle Generator. REST then goes LO as before and starts the Dot Cycle Generator and Dot Timer. This cycle continues, displaying one dot per cycle (except for the first nondisplayed dot of a character which is automatically initiated by $\overline{\text{EOCH2}}$), until the Display Sequencer determines that the readout time is over (sets $\overline{\text{ROA}}$ HI) or until the display priority is decremented to zero.

When a display priority of three or four exists, the output of U2990B will be LO, and U2970B, U2880A, and the associated logic gates following it will not be able to initiate a dot cycle. In either of these display priorities, U2970D, U2835C, U2980A, U2965B, and flip-flop U2950B detect the higher priority and generate a readout request signal ($\overline{\text{ROR}}$) to the Display Sequencer. The LO from U2950B pin 8 propagates through U2890B and U2890C to initiate a STARTDOT cycle. When the Display Sequencer recognizes that the readout request signal is LO, it will perform the mode-dependent setup functions necessary to give display control to the Readout Board and will then set the $\overline{\text{ROA}}$ (readout active) line LO. The LO will be clocked into U2880B, and the Dot Cycle Generator will generate a $\overline{\text{GETDOT}}$ signal, resetting the readout request from flip-flop U2950B. Only one dot is displayed for each readout request.

A similar readout display request will be generated when priority-two-or-higher displays are required when sweep gates are not present (dot display during triggerable time after holdoff). This condition is detected by NAND-gate U2885A. AND-gate U2970D allows a readout request to be generated when in the interfere mode. This mode is invoked only during a single-sequence waveform display and ensures that all of the selected sweep combinations are displayed once, followed by a complete readout frame (for the purpose of crt photography).

Dot Cycle Generator

The Dot Cycle Generator, composed of shift register U2995, flip-flop U2880B, and associated gating circuitry, generates time-related signals for the following purposes: unblanking the crt to display a dot; requesting the next byte of dot data in preparation for displaying the next dot; and reenabling itself to repeat the tasks, via the Dot Start Governor (dependent on the display priority).

The timing relationships of the Dot Cycle Generator output signals are controlled by shift register U2995. When the Dot Start Governor initiates a STARTDOT cycle as previously described, the STARTDOT signal initially goes LO, resetting all the Q outputs of U2995 LO and setting the Q output of flip-flop U2880B to a HI. The STARTDOT signal is then returned HI, and Dot Timer counter U2830A and shift register U2995 are enabled. The shift register begins to consecutively shift HI logic levels to its Q output pins with each 5-MHz clock from Dot Timer. After approximately 400 ns, pin 5 (Q_C) of the shift register will go HI. The HI at Q_C propagates through exclusive-OR-gate U2990D and AND-gate U2970A to unblank the crt by setting the readout blanking signal ($\overline{\text{ROB}}$) HI.

When the Q_F output of U2995 goes HI (1 μs after STARTDOT), the output of U2990D goes LO and the output of U2990C goes HI. The LO from U2990D propagates through U2970A to blank the crt ($\overline{\text{ROB}}$ goes LO) and to clock flip-flop U2880B via inverter U2890C. The $\overline{\text{ROA}}$

(readout active) level from the Display Sequencer (diagram 5) is clocked from the D input (pin 12) of U2880B to the Q output; and, if LO (indicating that the readout circuitry had control of the crt when unblanking occurred; thus the dot was displayed), the output of U2980B is set HI. With three HI levels applied to NAND-gate U2885C, a $\overline{\text{GETDOT}}$ request is generated to get the next byte of dot-position data for display. The next 5-MHz clock sets the Q_G output of U2995 HI, and the output of U2990C goes LO, removing the LO $\overline{\text{GETDOT}}$ signal.

At 1.4 μs after STARTDOT goes HI, U2995 pin 13 (Q_H) goes HI to produce the REST signal, indicating that the current dot cycle is complete and the Dot Cycle Generator is at REST. If the readout ACTIVE/$\overline{\text{ADDRESSABLE}}$ mode bit at U2970C pin 10 is still HI, the REST signal going HI produces a HI DOTOK signal (next dot is allowed) at pin 8. This HI applied to pin 10 of U2890C, along with any of the possible dot requests from the Dot Start Governor, will initiate another STARTDOT cycle for the next dot of the display. As long as the Display Sequencer holds the readout active line ($\overline{\text{ROA}}$) LO, U2885B, U2890D, and U2890B of the Dot Start Governor will automatically initiate dot cycles as soon as the previous one ends (REST goes HI), until the Refresh Prioritizer is decremented to zero.

When the last dot of the character is called from the Character ROM, the $\overline{\text{EOCH}}$ bit (DD7) applied to latch U2905 at pin 8 (in the Mode Select Logic circuitry) is LO. At the end of that dot display cycle, the $\overline{\text{GETDOT}}$ signal clocks the LO $\overline{\text{EOCH}}$ bit into latch U2905. The latched bit becomes the $\overline{\text{EOCH1}}$ signal (end of character, delayed one dot request) and is applied to U2855B, along with the already LO $\overline{\text{EOCH}}$ bit, to reset Dot Counters U2870A and B. The least-significant bits to the Character ROM address pins (A0 through A4) are then zeros, and the first dot of the next character is addressed. The Horizontal and Vertical DACs don't write this first dot position data into their registers until the end of the next $\overline{\text{GETDOT}}$ signal. That same $\overline{\text{GETDOT}}$ signal also clocks $\overline{\text{EOCH1}}$ into U2905 which becomes $\overline{\text{EOCH2}}$ at pin 6 (end of character, delayed by two dot requests). $\overline{\text{EOCH2}}$ is applied to AND-gate U2970A and disables the gate prior to the time the Dot Cycle Generator attempts to unblank the crt for the first dot display; thus the first dot of a character is never displayed.

Disabling the unblanking path for the first dot of each character in the manner just described allows the more radical voltage changes between characters to settle before the actual display of the next character begins. When the dot data for one of these undisplayed dots also has the $\overline{\text{EOCH}}$ bit set LO, it is a space character, and the display is advanced to the next character.

Dot Timer

The Dot Timer, composed of U2890A and U2830A and B, generates three, time-related signals used to synchronize the display and maintain the proper sequencing of the individual character dots.

The two least-significant bits of the Dot Timer, from U2830B pins 11 and 10, are reset at the beginning of a dot cycle by a LO STARTDOT signal applied to the reset input of the counter via U2890A. As the dot-display cycle begins, the STARTDOT signal returns HI and the Dot Timer begins counting in a binary fashion. The 10-MHz clock applied to pin 13 is divided by two to produce the 5-MHz clocking signal at output pin 11. The 5-MHz clock sequences the Dot Cycle Generator through the various phases of the dot-display cycle. The REFRESH output signal from U2830A pin 4 updates the Refresh Prioritizer as each subframe is displayed.

A third clock, from U2830A pin 6, occurs at approximately 8-μs intervals and allows any pending dot requests to generate a $\overline{\text{ROR}}$ signal to the Display Sequencer via flip-flop U2950B. (Readout request generation is described in the Dot Start Governor discussion.)

HIGH VOLTAGE POWER SUPPLY AND CRT

The High Voltage Power Supply and CRT circuit (diagram 8) provides the voltage levels and control circuitry for operation of the cathode-ray tube (crt). The circuitry consists of the High Voltage Oscillator, the High Voltage Regulator, the Cathode Supply, the Anode Multiplier, the DC Restorer, Focus Amplifiers, the CRT, and the various CRT Control circuits.

High Voltage Oscillator

The High Voltage Oscillator transforms power obtained from the −15 V unregulated supply into the various ac levels necessary for the operation of the crt circuitry. The circuit consists primarily of transformer T1970 and switching transistor Q1981 connected in a power oscillator configuration. The low-voltage oscillations set up in the primary winding of T1970 are raised by transformer action to high-voltage levels in the secondary windings. These ac secondary voltages are applied to the DC Restorer, the Cathode Supply, and the Anode Multiplier circuits that provide the necessary crt operating potentials.

Oscillation occurs due to the positive feedback from the primary winding (pin 4 to pin 5) to the smaller base-drive winding (pin 3 to pin 6) that provides base drive to switching transistor Q1981. The frequency of oscillation is

approximately 50 kHz and is determined primarily by the resonant frequency of the transformer.

OSCILLATION START-UP. Initially, when power is applied, the High Voltage Regulator circuit detects that the crt cathode voltage is too positive and pulls pin 6 of transformer T1970 negative. The negative level is applied to switching transistor Q1981 through the transformer winding and forward biases it. Current begins to flow in the primary winding through the transistor collector circuit and induces a magnetic field around the transformer primary winding. The increasing magnetic field induces a current in the base-drive winding that further increases the base drive to the transistor. This inphase feedback causes Q1981 to quickly saturate, at which point the current in the primary winding reaches its maximum value. As the rate of change in the primary current peaks and then reverses, the induced magnetic field begins to decay. This decreases the base-drive current and begins to turn Q1981 off.

As Q1981 turns off, the magnetic field around the primary winding continues to collapse, and a voltage of opposite polarity is induced in the base-drive winding. This turns the switching transistor completely off. Once again, as the magnetic field builds and then reverses, the current induced in the base-drive winding changes direction, forward biasing Q1981. At that point, the primary-winding current starts increasing again, and the switching transistor is again driven into saturation by the feedback supplied to the base-drive winding. This sequence of events occurs repetitively as the circuit continues to oscillate.

The oscillating magnetic field couples power from the primary winding into the secondary windings of the transformer. The amplitudes of the voltages induced in the secondary windings are functions of the turns ratios of the transformer windings.

High Voltage Regulator

The High Voltage Regulator consists of U1956A and B and associated components. It monitors the crt Cathode Supply voltage and varies the bias point of the switching transistor in the High Voltage Oscillator to hold the Cathode Supply voltage at the nominal level. Since the output voltages at the other secondary winding taps are related by turns ratios to the Cathode Supply voltage, all voltages are held in regulation.

When the Cathode Supply voltage is at the proper level (−1900 V), the current through R1945 and the 19-MΩ resistor internal to High Voltage Module U1830 holds the voltage developed across C1932 at zero volts. This is the balanced condition and sets base drive in Q1981 via integrator U1956A and voltage-follower U1956B. Varying base drive to Q1981 holds the secondary voltages in regulation.

If the Cathode Supply voltage level tends too positive, a slightly positive voltage will develop across C1932. This voltage causes the outputs of integrator U1956A and voltage-follower U1956B to move negative. The negative shift charges capacitor C1951 to a different level, around which the induced feedback voltage at the base-drive winding will swing. The added negative bias causes Q1981 to turn on earlier in the oscillation cycle, and a stronger current pulse is induced in the secondary windings. The increased power in the secondary windings increases the secondary voltages until the Cathode Supply voltage returns to the balanced condition (zero volts across C1932). Opposite action occurs should the Cathode Supply voltage tend too negative.

Cathode Supply

The Cathode Supply circuit is composed of a voltage doubler and an RC filter network contained within High Voltage Module U1830. This supply produces the −1900-V accelerating potential applied to the CRT cathode and the −900-V slot lens voltage. The −1900-V supply is monitored by the High Voltage Regulator to maintain the regulation of all voltages from the High Voltage Oscillator.

The alternating voltage from pin 10 of transformer T1970 (950 V peak) is applied to a conventional voltage-doubler circuit at pin 7 of the High Voltage Module. On the positive half cycle, the input capacitor of the voltage doubler (0.006 μf) is charged to −950 V through the forward-biased diode connected to ground at pin 9 of the module (charging path is through the diode, so stored charge is negative). The following negative half cycle adds its ac component (−950 V peak) to this stored dc value and produces a total peak voltage of −1900 V across the capacitor. This charges the 0.006-μf storage capacitor (connected across the two doubler diodes) through the second diode (now the forward-biased diode) to −1900 V. Two RC filters follow the voltage doubler to smooth out the ac ripple. A resistive voltage divider across the output of the filter network provides the −900-V slot lens potential.

Anode Multiplier

The Anode Multiplier circuit (also contained in High Voltage Module U1830) uses voltage multiplication to produce the +14-kV CRT anode potential. Circuit operation is similar to that of the voltage-doubler circuit of the Cathode Supply.

The first negative half cycle charges the 0.001-μf input capacitor (connected to pin 8 of the High Voltage Module) to a positive peak value of +2.33 kV. The following positive half cycle adds its positive peak amplitude to the voltage stored on the input capacitor and boosts the charge on the second capacitor of the multiplier (and those following) to +4.66 kV. Following cycles continue to boost up succeeding capacitors to values 2.33 kV higher than the preceding capacitor until all six capacitors are fully charged. This places the output of the last capacitor in the multiplier at +14 kV above ground potential. Once the multiplier reaches operating potential, succeeding cycles replenish current drawn from the Anode Multiplier by the crt beam. The 1-MΩ resistor in series with the output protects the multiplier by limiting the anode current to a safe value.

Focus Amplifier

The Focus Amplifier, in conjunction with the auto-focus circuitry of Z-Axis hybrid U950 (diagram 6), provides optimum focus of the crt beam for all settings of the front-panel INTENSITY control. The Focus Amplifier itself consists of two shunt-feedback amplifiers composed of Q1851, Q1852, and associated components. The outputs of these amplifiers set the operating points of a horizontally converging quadrapole lens and a vertically converging quadrapole lens within the crt. The convergence strength of each lens is dependent on the electric field set up between the lens elements.

Since the bases of Q1851 and Q1852 are held at constant voltages (set by their emitter potentials), changing the position of the wiper arms of the ASTIG and FOCUS pots changes the amount of current sourced to the base junctions through R1856 and R1857 respectively. This changes the base-drive currents and produces different output levels from the Focus Amplifiers; that, in turn, changes the convergence characteristics of the quadrapole lenses.

Initially, at the time of adjustment, the FOCUS and ASTIG potentiometers are set for optimum focus of the crt beam at low intensity. After that initial adjustment, the ASTIG pot normally remains as set, and the FOCUS control is positioned by the user as required when viewing the displays. When using the FOCUS control, transistor Q1852 is controlled as described above; however, an additional current is also supplied to the base node of Q1851 from the FOCUS pot through R1855. This additional current varies the base-drive current to Q1851 and provides tracking between the two lenses as the FOCUS control is adjusted during use of the instrument.

The convergence strengths of the quadrapole lenses also dynamically track changes in the display intensity. The VQOUT signal, applied to the crt at pins 5 and 6, is exponentially related to the VZOUT (intensity) signal driving the crt control grid and increases the strength of the lenses more at higher crt beam currents. (A higher beam current requires a stronger lens to cause an equal convergence of the beam.)

DC Restorer

The DC Restorer provides crt control-grid bias and couples both the dc and the low-frequency components of the Z-Axis drive signal to the crt control grid. This circuit allows the Z-Axis Amplifier to control the display intensity by coupling the low-voltage Z-Axis drive signal (VZOUT) to the elevated crt control-grid potential (about −1.9 kV).

The DC Restorer circuit (Figure 3-10) operates by impressing the crt grid bias setting and the Z-Axis drive signal on an ac voltage waveform. The shaped ac waveform is then coupled to the crt control grid through a coupling capacitor that restores the dc components of the signal.

GRID BIAS LEVEL. An ac drive voltage of approximately 300 V peak-to-peak is applied to the DC Restorer circuit from pin 7 of transformer T1970. The negative half cycle of the sinusoidal waveform is clipped by CR1953, and the positive half cycle (150 V peak) is applied to the junction of CR1930, CR1951, and R1941 via R1950 and R1953. Transistor Q1980, operational amplifier U1890A, and associated components form a voltage clamp circuit that limits the positive swing of the ac waveform at the junction.

Transistor Q1980 is configured as a shunt-feedback amplifier, with C1991 and R1994 as the feedback elements. The feedback current through R1994 develops a voltage across the resistor that is positive with respect to the +42.6 V on the base of the transistor. The value of this additive voltage plus the two diode drops across CR1950 and CR1951 sets the upper clamping threshold. Grid Bias potentiometer R1878 sinks varying amounts of current away from the base node of the transistor and thus sets the feedback current through R1994. The adjustment range of the pot can set the nominal clamping level between +71 V and +133 V.

When the amplitude of the ac waveform is below the clamping threshold, series diodes CR1950 and CR1951 will be reverse biased and the ac waveform is not clamped. During the time the diodes are reverse biased, transistor Q1980 is kept biased in the active region by the charge retained on C1971 from the previous cycle. As the amplitude of the ac waveform at the junction of CR1930 and CR1950 exceeds the voltage at the collector of Q1980, the two series diodes (CR1950 and CR1951) become forward biased, and the ac waveform is clamped at that

level. Any current greater than that required to maintain the clamp voltage will be shunted to the +42-V supply by transistor Q1980.

Operational amplifier U1890A sinks a time-dependent variable current away from the base node of Q1980 that modifies the crt control-grid bias during the first few minutes of instrument operation. The circuit compensates for the changing drive characteristics of the crt as it warms up.

At power-up, capacitor C1990 begins charging through R1991 toward the +15-V supply. The output of U1890A follows the rising voltage on pin 3; and after about ten minutes (for all practical purposes), it reaches +15 V. As the output voltage slowly increases, the charging current through R1992 causes the Grid Bias voltage to gradually lower about ten volts from its power-on level. The charge on C1990 dissipates slowly; therefore, if instrument power is turned off and then immediately back on again, the output of U1890A will still be near the +15-V limit rather than starting at zero volts as when the crt was cold.

Z-AXIS DRIVE LEVEL. The variable-level Z-Axis signal (VZOUT) establishes the lower clamping level of the ac waveform applied to the High Voltage Module. When the amplitude of the waveform drops below the Z-Axis signal level, CR1930 becomes forward biased, and the ac waveform is clamped to the Z-Axis signal level. The VZOUT

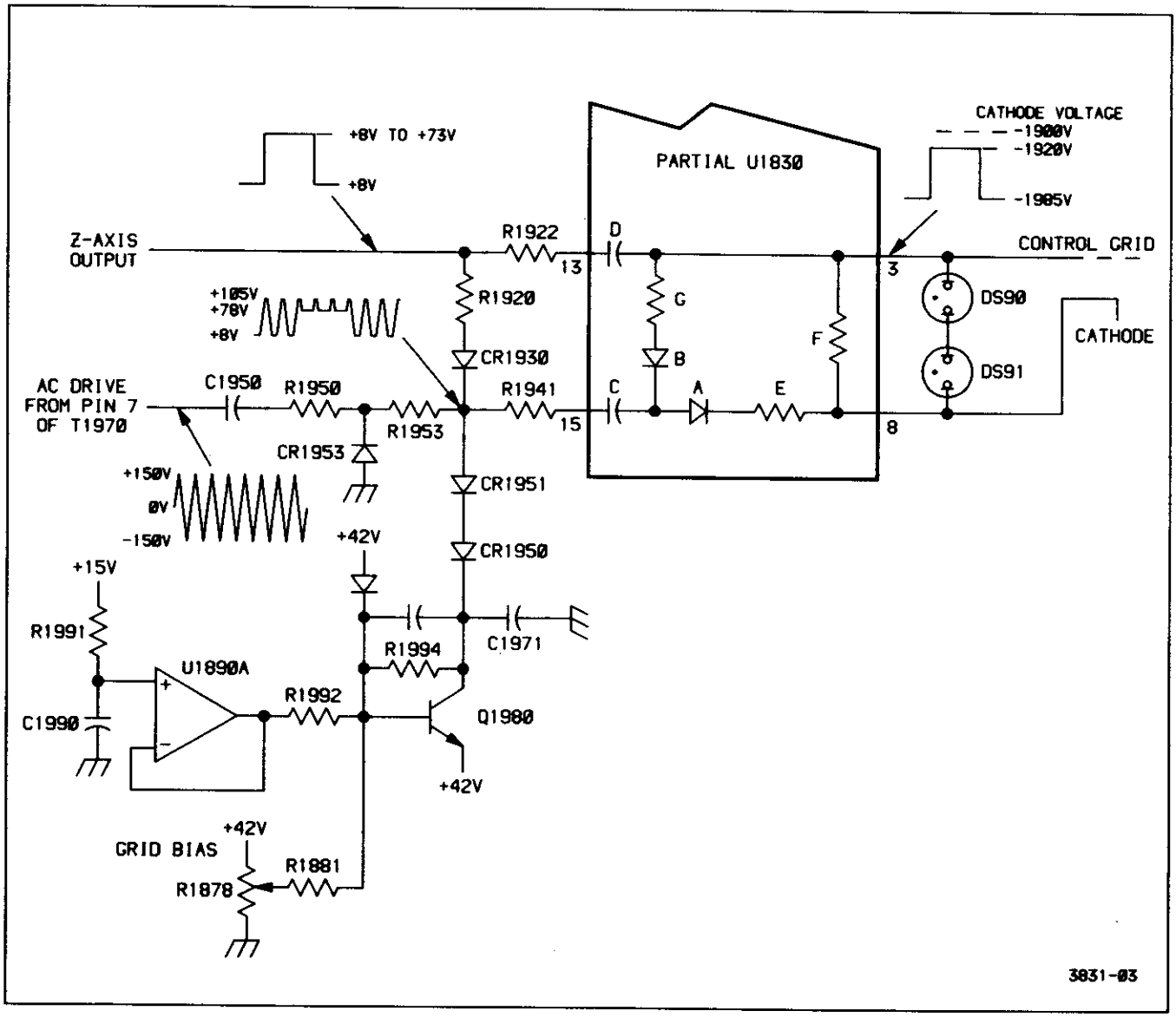

Figure 3-10. Dc Restorer circuit.

level may vary between +8 V and +75 V, depending on the setting of the front-panel INTENSITY and READOUT INTENSITY controls.

The ac waveform, now carrying both the grid-bias information and the Z-Axis drive information, is applied to a DC Restorer circuit in the High Voltage Module where it is raised to the high-voltage levels of the crt control grid.

DC RESTORATION. The DC Restorer circuit in the High Voltage Module is referenced to the crt cathode voltage via a connection within U1830. Capacitor C (in Figure 3-10), connected to pin 15 of U1830, initially charges to a level determined by the difference between the Z-Axis signal level and the crt cathode potential. The Z-Axis signal sets the level on the positive plate of capacitor C through R1920, CR1930, and R1941; the level on the negative plate is set by the crt cathode voltage through resistor E and diode A. Capacitor D is charged to a similar dc level through resistor F and R1922.

When the ac waveform applied to pin 15 begins its transition from the lower clamped level (set by the Z-Axis signal) towards the upper clamped level (set by the Grid Bias potentiometer), the charge on capacitor C increases. The additional charge is proportional to the voltage difference between the two clamped voltage levels.

When the ac waveform begins its transition from the upper clamped level back to the lower clamped level, diode A becomes reverse biased. Diode B becomes forward biased, and an additional charge proportional to the negative excusion of the ac waveform (difference between the upper clamped level and the lower clamped level) is added to capacitor D through diode B and resistor G. The amount of charge added to capacitor D depends on the setting of the front-panel INTENSITY control, as it sets the lower clamping level of the ac waveform. This added charge determines the potential of the control grid with respect to the crt cathode.

The potential difference between the control grid and the cathode controls the beam current and thus the display intensity. With no Z-Axis signal applied (INTENSITY control off), capacitor D will be charged to its maximum negative value, since the difference between the two clamped voltage levels is at its maximum value. This is the minimum intensity condition and reflects the setting of the Grid Bias potentiometer. During calibration, the Grid Bias pot is adjusted so that the difference between the upper clamping level (set by the Grid Bias pot) and the "no signal" level of the Z-Axis drive signal (VZOUT) produces a control grid bias that barely shuts off the crt electron beam.

As the INTENSITY control is advanced, the amplitude of the square-wave Z-Axis signal increases accordingly. This increased signal amplitude decreases the difference between the upper and lower clamped levels of the ac waveform, and less charge is added to capacitor D. The decreased voltage across capacitor D decreases the potential difference between the control grid and the cathode, and more crt beam current is allowed to flow. Increased beam current increases the crt display intensity.

During the periods that capacitor C is charging and discharging, the control-grid voltage is held stable by the long-time-constant discharge path of capacitor D through resistor F. Any charge removed from capacitor D during the positive transitions of the ac waveform will be replaced on the negative transitions.

The fast-rise and fast-fall transitions of the Z-Axis signal are coupled to the crt control grid through capacitor D. This ac-coupled fast-path signal quickly sends the crt electron beam to the new intensity level, then the slower DC Restorer path "cathes up" to handle the dc and low-frequency components of the Z-Axis drive signal.

Neon lamps DS90 and DS91 prevent arcing inside the crt should the control grid potential or cathode potential be lost for any reason.

CRT Control Circuits

The CRT Control circuits provide the various potentials and signal attenuation factors that set up the electrical elements of the crt. The control circuitry is divided into two separate catagories: (1) level setting and (2) signal handling. The level-setting circuitry produces voltages and current levels necessary for the crt to operate, while the signal-handling portion is associated with changing crt signal levels.

LEVEL-SETTING CIRCUITRY. Operational amplifier U1890B, transistor Q1980, and associated components form an edge-focus circuit that sets the voltages on the elements of the third quadrapole lens. The positive lens element is set to its operating potential by Edge Focus adjustment pot R1864 (via R1897). This voltage is also divided by R1893 and R1982 and applied to the non-inverting input of U1890B to control the voltage on the other element of the lens.

The operational amplifier and transistor are configured as a feedback amplifier, with R1891 and R1990 setting the stage gain. Gain of the amplifier is equal to the attenuation factor of divider network R1893 and R1892, so total overall gain of the stage from the wiper of R1864 to the collector of Q1890 is unity. The offset voltage between lens

elements is set by the ratio of R1891 and R1990 and the +10-V reference applied to R1990. This configuration causes the two voltages applied to the third quadrapole lens to track each other over the entire range of Edge Focus adjustment pot R1864.

Other adjustable level-setting circuits include Y-Axis Alignment pot R1848, used to rotate the beam alignment after vertical deflection. This adjustment controls the amount of current through the Y-Axis Alignment coil around the neck of the crt and is set to produce precise perpendicular alignment between x- and y-axis deflections. The TRACE ROTATION adjustment R975 is a front-panel screwdriver-adjustable control. The effect of the adjustment is similar to the Y-Axis Alignment pot, but when adjusted, it rotates both the x-axis and the y-axis deflections of the trace on the face of the crt. A final adjustable level-setting control is the Geometry pot R1870, adjusted to optimize display geometry. The potential at pin 8 for the vertical shield internal to the crt is produced by zener diode VR1891 and associated components.

SIGNAL-HANDLING CIRCUITRY. The crt termination adjustment R1301 is set to match the loading characteristics of the crt's vertical deflection structure to the Vertical Output Amplifier.

LOW VOLTAGE POWER SUPPLY

The low voltages required by the 2465 are produced by a high-efficiency, switching power supply. This type of supply directly rectifies and stores charge from the ac line supply; then the stored charge is switched through a special transformer at a high rate, generating the various supply voltages.

Line Rectifier

Ac line voltages of either 115 V or 230 V may provide the primary power for the instrument, depending on the setting of the LINE VOLTAGE SELECTOR switch S90 (located on the instrument rear panel). Power Switch S350 applies the selected line voltage to the power supply rectifier (CR1011).

With the selector switch in the 115-V position, the rectifier and storage capacitors C1021 and C1022 operate as a full-wave voltage doubler. When operating in this configuration, each capacitor is charged on opposite half cycles of the ac input, and the voltages across the two capacitors in series will approximate the peak-to-peak value of the source voltage. For 230-V operation, switch S90 connects the rectifier as a conventional bridge rectifier. Both capacitors charge on both input half cycles, and the voltage across C1021 and C1022 in series will approximate the peak value of the rectified source voltage. For either configuration, the dc voltage supplied to the power supply inverter is the same.

Thermistors RT1010 and RT1016 limit the surge current when the power supply is first turned on. As current flow warms the thermistors, their resistances decrease and have little effect on circuit operation. Spark-gap electrodes E1001 and E1002 are surge-voltage protectors. If excessive source voltage is applied to the instrument, the spark-gaps conduct, and the extra current flow quickly exceeds the rating of F90. The fuse then opens to protect the instrument's power supply. The EMI (electromagnetic interference) filter, inductors L1011 and L1012, capacitors C1014 and C1016, and resistors R1011, R1014, and R1016 form a line-filter circuit. This filter, along with common-mode rejection transformer T1020, prevents power-line interference from entering the instrument and prevents power supply switching signals from entering the supply line.

Preregulator Control

The Preregulator Control circuit monitors the drive voltage applied to the Inverter output transformer T1060 and holds it at the level that produces proper supply voltages at each of the secondary windings.

The Preregulator Control circuit consists primarily of control IC U1030, its switching buffers, and its power supply components. The control IC senses voltage on the primary winding of T2060 and varies the "on time" of a series-switching transistor, depending on whether the sensed voltage is too high or too low. The switching transistor Q1050, rectifier CR1050, choke T1050, and capacitor C1050 form a buck-switching regulator circuit. The output voltage at W1060 is proportional to the product of the rectified line voltage on C1020-C1022 and the duty cycle of Q1050. In normal operation, Q1050 is on about one-half of the time. When Q1050 is off, current flows to W1060 and T1060 through CR1050.

PREREGULATOR CONTROL POWER SUPPLY. Since the Preregulator control network controls supply startup and preregulates the secondary supplies, an independent power source must be established for it before any of the other power supplies will operate. The independent power supply for the control circuitry is composed of Q1021, Q1022, and the associated components.

Initially, when instrument power is applied, the positive plate of capacitor C1025 is charged toward the positive rectified line voltage through R1020. The voltage at the base of Q1022 follows at a level determined by the voltage divider composed of R1022, R1024, CR1023, and the load within U1030. When the voltage across C1025 reaches

about +21 V, the base voltage of Q1022 reaches +6.8 V and Q1022 turns on, saturating Q1021. The +21 V on the emitter of Q1021 appears at its collector and establishes the positive voltage supply for the Preregulator IC. With Q1021 on, R1024 is placed in parallel with R1022, and both Q1022 and Q1021 remain saturated.

The +21-V level begins to drain down as the control IC draws current from C1025. If the Preregulator Control IC doesn't start the switching supply (and thus recharge C1025 and C1023 via CR1022) by the time the voltage across C1025 reaches about +8 V, Q1021 will turn off. Resistor R1024 pulls the base of Q1022 low and turns that transistor off also. (Capacitor C1025 would only discharge low enough to turn off the transistors under a fault condition.) In this event, C1025 would then charge again to +21 V, and the start sequence would repeat. Normally, the control IC will start Inverter action before the +8-V level is reached, and current is drawn through T1050 via Q1050. This induces a current in the secondary winding of T1050 and charges C1025 positive via diode CR1022. The turns ratio of T1050 sets the secondary voltage at approximately +15 V; and, as long as the supply is being properly regulated, C1025 will be charged up to that level and held there.

PREREGULATOR START-UP. As the supply for the Preregulator Control IC is established, an internal switching oscillator begins to run. The oscillator generates a repetitive triangular wave (as shown in Figure 3-11) at a frequency determined primarily by R1032 and C1032. The simplified schematic of Figure 3-12 illustrates the voltage control functions of U1030.

As the Preregulator power supply turns on, capacitor C1034 charges from the +5-V reference level toward ground potential through R1034 and R1037. As it does, the voltage at pin 4 (one input of Dead-Time Comparator U1) will pass through the positive-peak value of the triangular waveform on the other input of the Dead-Time Comparator. The comparator will then begin outputting narrow pulses that become progressively wider as the voltage on pin 4 settles to zero volts. These pulses drive switching transistor Q1050, and their slow progression from narrow to wide causes the various secondary supplies to gradually build up to their final operating levels. The slow buildup prevents a turn-on current surge that would cause the current-limit circuitry to shut down the supply.

During the startup, capacitor C1072 acts as a substantial load, and a relatively large current will flow in the windings of T1050 for the first few cycles of Preregulator switching. These strong current pulses ensure that storage capacitor C1066 becomes charged sufficiently to start the Inverter Drive circuit. Once the Inverter Drive stage is operating, the normal switching current through T1050 maintains the required charge on C1066. (The Inverter Drive power supply is discussed later in this description.)

Dead-Time Comparator U1 is referenced at approximately 0.1 V above the ground level at pin 4 (established when C1034 becomes fully charged) and outputs a narrow, negative-going pulse that turns off switching transistor Q1050 for a portion of each switching cycle. This off time ensures that flip-flop U1064B in the Inverter Drive circuit toggles every cycle (thereby maintaining the proper duty cycle), independent of the voltage conditions being sensed by the remainder of the voltage control circuitry.

PREREGULATION. Once the initial charging at power-up is accomplished, as just described, the voltage-sensing circuitry begins controlling the Inverter switching action. The actual voltage sensing is done by error amplifier U2. The level at the center tap of output transformer T1060 is applied to pin 1 and is compared to the reference established by R1045 and R1046 at pin 2. If the sensed level at pin 1 is lower than the reference level at pin 2 (as it will always be for the first few switching cycles), the output of error-amplifier U2 will be LO. The LO, applied to the inverting input of U3, results in a long-duty-cycle drive signal to transistor Q1050 (via CR1030). Since the Inverter Drive stage will alternately turn either Q1060 or Q1070 on, relatively large current pulses will result in the primary winding of inverter output transformer T1060.

These large current pulses, over the period of a few cycles, will increase the charge on the storage capacitors on the secondary side of the transformer and will reduce the current demand on the inverter output transformer. As the demand decreases, the voltage across the primary winding will increase until it reaches the point where the two inputs of U2 are at the same potential. At this point, the output of U2 (to U3) will settle to a level approximately equal to the midpoint of the triangular waveform applied to the other input of U3. The resulting drive signal has an approximate 50% duty cycle and will respond to changes in either the ac line voltage or supply load conditions. Depending on the output levels sensed, the duty cycle of the drive signal will change (sensed level rises or falls with respect to the triangular waveform) to hold the secondary supplies at their proper levels.

Opto-isolator U1040 and resistor R1044 form a control network that allows a voltage sensed at the feedback input (FB) to slightly alter the voltage-sense reference applied to pin 2 of U2. The FB signal is generated by the +5-V Inverter Feedback amplifier (U1371, diagram 10) and is directly related to the level of the +5-V_D supply line. Base drive to the shunt transistor (in opto-isolator U1040) is increased should the FB signal go below its nominal value. Additional current is shunted around R1045 (via R1044) and raises the voltage-sense reference level to error-amplifier U2. This increases the voltage applied to the primary winding of the output transformer, since U2 sensing depends on a balanced condition. Higher currents are induced in the secondary windings, and the secondary

voltages begin to return to their nominal values. As the +5-V_D line returns to its nominal level, base drive to the shunt transistor will be reduced and the voltage in the primary winding will follow. Should the FB signal level tend too high, opposite control responses occur. Further information about the FB signal is given in the +5 V Inverter Feedback description.

Error amplifier U4 and the voltage divider composed of R1035 and R1031 provide a backup sensing circuit. Its operation is similar to that of error amplifier U2, just described, but it senses at a slightly higher level. As long as U2 is operating properly, U4 will be inactive. However, should a failure occur in the U2 sensing circuitry, the voltage on the primary winding of T1060 will rise to the sensing level at pin 15 of U4. Sense amplifier U4 will then take over, preventing a damaging over-voltage condition.

Inverter Drive

The Inverter Drive circuit performs the necessary switching to drive the Inverter output transformer. Like the Preregulator Control IC, the Inverter Drive circuit requires an independent power supply, since it must be operational before any of the secondary supply voltages can be generated.

INVERTER DRIVE POWER SUPPLY. This power supply consists of Q1062, VR1062, and their associated

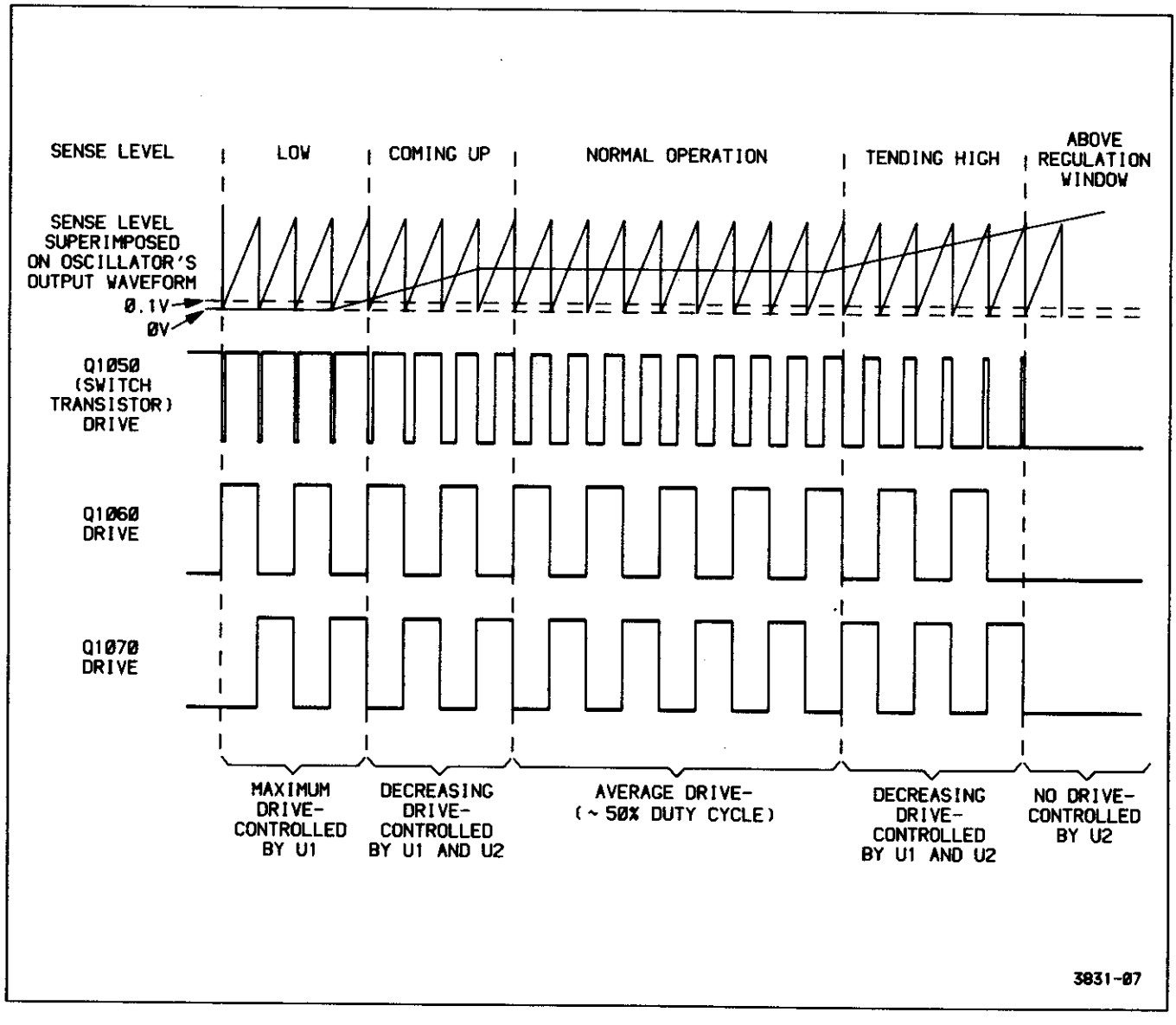

Figure 3-11. Timing relationships of the Inverter Drive signals.

components. As power is first applied, the initial charging current through T1050 induces a current in the transformer secondary winding (pins 8 and 9). The alternating current is rectified by the diode bridge composed of CR1062, CR1063, CR1064, and CR1065 and stored on C1066, providing power for the Inverter Drive circuitry.

When the Preregulator Control IC turns switching transistor Q1050 on for the first time, the charge stored on C1066 during the initial charging period is sufficient to properly turn on one of the current-switching transistors (either Q1060 or Q1070) for the first cycle. After that, the alternating drive signals continue to induce current into the secondary winding of T1050 to provide operating power as long as the instrument is turned on.

The current rectified by the diode bridge and stored on capacitor C1066 is regulated down to the required voltage level by R1061, VR1062, and Q1062. Zener diode VR1062 references emitter-follower Q1062 and holds the supply output at approximately +11.4 V.

INVERTER DRIVE GENERATOR. The Inverter Drive generator consists of U1062, U1064, U1066, switching transistors Q1060 and Q1070, and the associated components. The circuitry alternately switches current through each leg of the output transformer primary winding and produces the ac current required for transformer action.

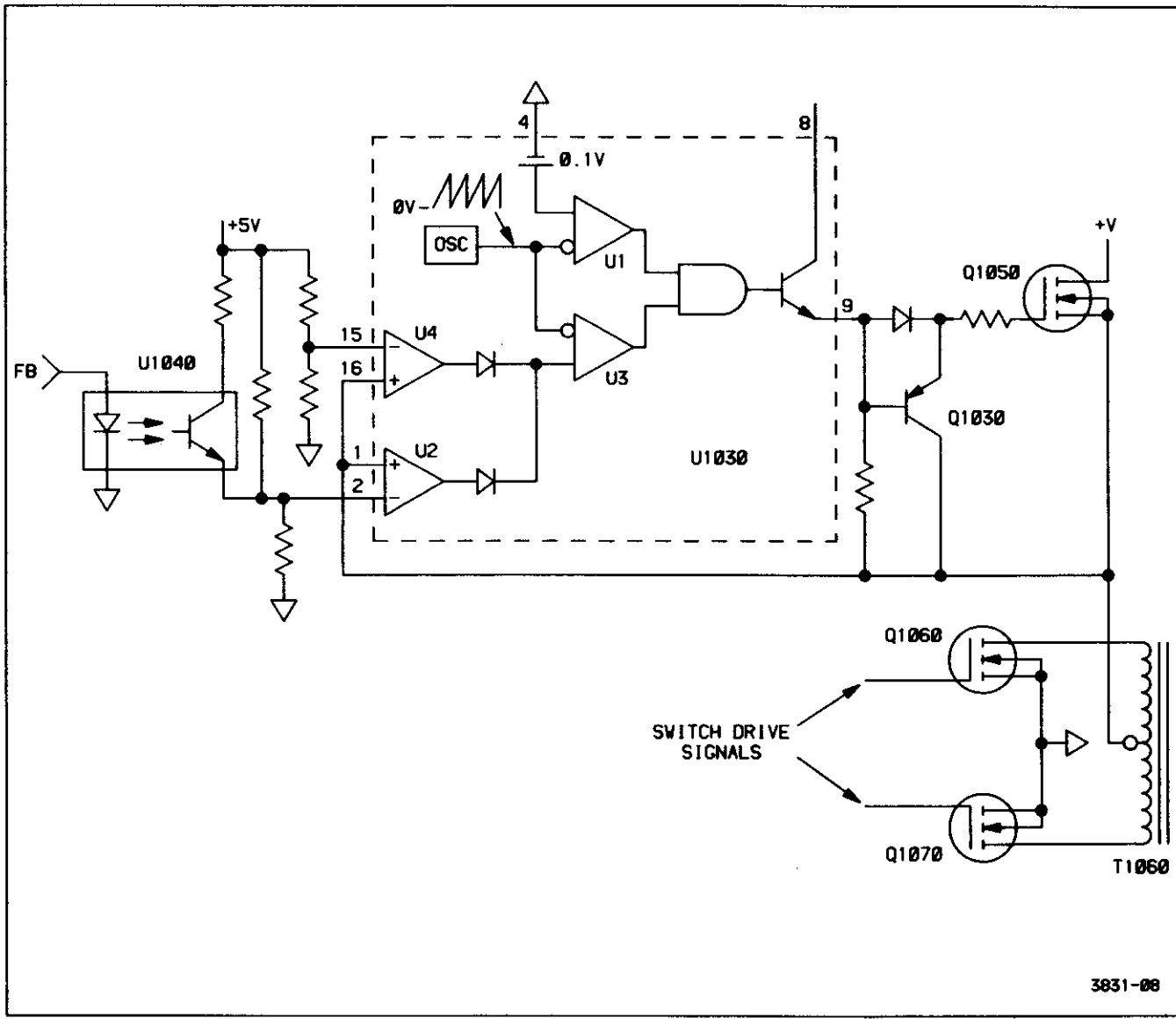

Figure 3-12. Simplified schematic of control network.

Out-of-phase input signals to comparator U1062C come from two resistive voltage dividers placed in either leg of one secondary winding of T1050. The comparator detects the phase changes (crossover points) of the secondary current caused as Q1050 switches on and off. Every complete on-off cycle of Q1050 produces a positive clock at pin 14 of U1062C that toggles flip-flop U1064B. The toggling alternately turns switching transistors Q1060 and Q1070 on, each with an approximate 50% duty cycle.

Comparators U1062A and U1062B, at the Q and Q output of the flip-flop, detect the precise crossing point of the toggling drive signals and ensure that only one switching transistor will be on at any one time. These mutually-exclusive drive signals are buffered by inverters U1066A and U1066B and applied to switching transistors Q1060 and Q1070 to alternately turn them on and off at one-half the switching rate of Q1050. By alternately switching opposite ends of the primary winding to ground, the current flowing through switching transistor Q1050 will flow alternately in each half of the primary winding. This produces ac voltages at the secondary windings that are rectifiied, providing the various unregulated dc supply voltages.

Current Limit

The Current Limit circuit, composed of transistor Q1040 and the associated components, limits the maximum current flow in the output transformer to about 1 ampere. Resistor R1040 (connected to the Preregulator Control IC +15-V supply) forward biases germanium diode CR1040 and applies approximately +0.3 V across the base-to-emitter junction of Q1040. Current flowing to the output transformer develops a voltage drop across R1050 that adds to the bias developed by CR1040. As the current to the transformer increases, the voltage drop across R1050 also increases until, at around 1 A, the combined voltage drop across R1050 and CR1040 forward biases transistor Q1040. The base of Q1022 is pulled negative through R1042, and the +15-V supply for the Preregulator IC turns off (see Preregulator Control discription). The power supply will try to restart itself; but, as long as the excessive-current condition persists, the current-limit circuit will keep shutting the supply down, protecting the instrument.

Rectifiers

The Rectifiers convert the alternating current from the secondary windings of the inverter output transformer to the various dc supply voltages required by the instrument. Rectification is done by conventional diode rectifier circuits, and filtering is done by conventional LC networks.

The +87-V unregulated supply is produced by a voltage-doubler circuit. The positive plate of C1130 at the anode of CR1132 is referenced at approximately +45 V through diode CR1131 (to the +42-V unregulated supply). As the positive half cycle from the 42-V secondary winding (actually about +45 V peak) is applied to the negative plate of C1130, the positive plate is elevated to a peak value of approximately +90 V. Diode CR1132 becomes forward biased and storage capacitor C1132 is charged to about +90 V. Following cycles replenish the charge drawn off by the loads on the +87-V supply line.

Line Signal

A sample of the ac line voltage is coupled to the Trigger circuit by transformer T1229 and provides the LINE TRIG signal to the Trigger hybrid. Transformer current is limited to a safe value by resistors R1014 and R1015 placed in series with the primary winding leads. The transformer's output characteristics are matched to the input of the Trigger circuit hybrid by R1208 and C1208.

Line Up Signal

The circuit composed of Q1029, opto-isolator U1029, and their associated components, detects when power has been applied to the instrument and the Preregulator Control power supply is functioning properly. When the rectified line voltage reaches proper operating voltage, the voltage divider composed of R1027 and R1028 forward biases Q1029. As soon as the Preregulator Control power supply turns on, current flows through R1029, Q1029, and the opto-isolator LED. The illuminated LED saturates transistor U1029 and the LINE UP signal to the Power-Up Delay circuit (diagram 1) is pulled HI, indicating that the Preregulator Control circuit should now be functioning properly.

POWER DOWN. When instrument power is turned off, the voltage across the primary storage capacitors (C1021 and C1022) begins to fall as the capacitors discharge. As the voltage drops, the bias current through R1027 to the base of Q1029 also drops until the bias voltage across R1028 reaches a point about 2 V above the average transformer drive level at pin 2 of U1029. At this point, Q1029 turns off, and the LINE UP signal to the Power-up Delay circuit goes LO. This LO signals the Microprocessor that it should start its power down routine.

The Line Up circuit tells the Microprocessor that the primary capacitors have started discharging while there is still a stored charge (set by R1027 and R1028) about 40% in excess of that required to keep the power supply voltages in regulation. This allows the Microprocessor to complete the power-down sequence before the supplies drop below their normal operating levels. Further information about the power-down sequence is given in the Microprocessor Reset Control description.

LOW VOLTAGE REGULATORS

The Low Voltage Regulators remove ac noise and ripple from the various unregulated dc supply voltages. Each regulator output is automatically current limited if the output current exceeds the requirements of a normally functioning instrument. This limiting prevents any further component damage.

+10 V Reference

Each of the power-supply regulators control their respective outputs by comparing their output voltages to a known reference level. In order to maintain stable supply voltages, the reference voltage must itself be highly stable. The circuit composed of U1290, U1300C, and associated components establishes this reference.

Resistor R1400 and capacitor C1400 form an RC filter network that smooths the unregulated +15-V supply before it is applied to voltage-reference IC U1290. The +2.5-V output from pin 2 of U1290 is applied to the noninverting input of operational amplifier U1300C. The output of U1300C is the source of the +10-V reference level used by the various regulators. The output level is set by the voltage divider formed by R1291, R1293, and potentiometer R1292. The Volt Ref Adjust pot in the divider allows the reference level to be precisely set. Zener diode VR1292 prevents the reference from exceeding +11 V should a failure in the reference circuitry occur.

+87 V Regulator

The +87 V Regulator is composed of Q1220, Q1221, Q1222, Q1223, U1281A, and the associated components. The circuit regulates and limits both the voltage and current of the supply output.

Initially, as power is applied, the voltage applied to pin 2 of U1281A from the voltage divider formed by R1227 and R1228 is lower than the +10-V reference level applied to pin 3. The output of U1281A is forced high, reverse biasing the base-emitter junction of Q1222 and turning it completely off. With Q1222 off, all the current through R1212 is supplied as base current to Darlington transistor pair Q1221 and Q1220, and maximum current flows in series-pass transistor Q1220. This charges up the various loads on the supply line, and the output level charges positive.

As the regulator output charges toward +87 V, the voltage divider applies a positive-going voltage to the inverting input of U1281A. When the output level reaches +87 volts, the inverting input equals the +10-V reference at the noninverting input. The output voltage at pin 1 of U1281A will go negative and the base-emitter junction of Q1222 will be biased into the active region. As Q1222 turns on, base drive for the Darlington pair (Q1221 and pass transistor Q1220) is reduced. The output will be held at the level required for voltage at the two inputs of amplifier U1281A to be in balance (+87 V).

Current limiting is a foldback design and is perfromed by Q1223 and its associated components. Under normal current demand conditions, Q1223 is off. If the regulator output current exceeds approximately 100 mA (as it might if a component fails), the voltage drop across R1221 and CR1220 reaches a point that forward biases Q1223 via the bias divider formed by R1222 and R1223. As Q1223 turns on, a portion of the base-drive current to Q1221 is shunted away by Q1223. This reduces the base-drive current (and thus the output current) of series-pass transistor Q1220.

+42 V Regulator

The circuit configuration and operation of the +42 V Regulator is identical to that of the +82 V Regulator. Current limiting of the +42-V supply occurs at approximately 400 mA. Base drive to Darlington pair Q1241 and Q1240 is via R1244 and is dependent on proper operation of the +87 V Regulator. This dependency ensures that the relative polarities of the two supplies are never reversed (preventing semiconductor-junction damage in the associated load circuitry).

+15 V Regulator

The +15 V Regulator uses three-terminal regulator U1260 and operational amplifiers U1371A and U1371B, arranged as voltage sensors, to achieve regulation of the +15-V supply. The three-terminal regulator holds its output voltage at pin 2 at 1.25 volts more positve than the reference input level at pin 1. The voltage at the reference pin is established by current flow in either diode CR1262 or CR1263.

Resistors R1261 and R1262 at the regulator output divide the +15-V level down for comparison with the +10-V reference applied to pin 5 of operational amplifier U1371B. When the input voltage at pin 6 (supplied by the voltage divider) is lower than the +10-V reference, the output of amplifier U1371B is high and the output voltage of U1260 is allowed to rise. As the regulator output reaches +15 V, the voltage on pin 6 of U1371B approaches the level on pin 5, and the amplifier begins sinking current away from the reference pin of the three-terminal regulator via diode CR1263. This lowers the voltage on the reference pin and holds the ouput at +15 V.

The other voltage-sensing amplifier (U1371A) ensures that the relative polarity between the +15-V supply and the

+42-V supply is maintained, preventing component damage in the load circuitry. Should the +42-V supply be pulled below +15 V (excessive loading or supply failure), the voltage at pin 3 of U1371A falls below the voltage at pin 2 and the amplifier output voltage goes low. This forward biases CR1262 and lowers the reference voltage for U1260, reducing the output voltage.

Current limiting for the +15-V supply is provided by the internal circuitry of the three-terminal regulator.

+5 V Regulator

Regulation of the +5-V supply is provided by a circuit similar to those of the +87 V and the +42 V Regulators. As long as the relative polarity between the +15-V and the +5-V supplies is maintained, base drive to Q1281 is supplied through R1283. The current through Q1281 provides base drive for series-pass transistor Q1280.

When voltage-sense amplifier U1300B detects that the output voltage has reached +5 V, it begins shunting base-drive current away from Q1281 via CR1281 and holds the output voltage constant.

Current limiting for the +5-V supply is done by U1300A and associated components. Under normal current-demand conditions, the output of U1300A is high and diode CR1282 is reverse biased. However, should the current through current-sense resistor R1281 reach approximately 2 A, the voltage developed across R1281 will raise the voltage at pin 2 of U1300A (via divider R1282 and R1286) to a level equal to that at pin 3. This causes the output of U1300A to go low, forward biasing CR1282. This sinks base drive current away from Q1281 and lowers the output current in series-pass transistor Q1280.

−15 V Regulator

Operation of the −15 V Regulator, composed of three-terminal regulator U1330, operational amplifier U1270C, and their associated components, is similar to that of the +15 V Regulator with the following major changes. The control voltage at the three-terminal regulator's reference pin (pin 1) is established by the current through series-resistors R1333 and R1334. The reference pin is clamped by CR1332 at about −5.6 V should a failure in the sensing network occur. (Clamping also prevents latchup of the operational amplifier during startup of the power supply.) Finally, the sensing divider formed by R1331 and R1332 is referenced to the +10-V reference instead of ground to enable sensing of negative voltage.

−8 V Regulator

Operation of the −8 V Regulator is similar to that of the +87 V and +42 V Regulators. Due to the lower operating voltages of the −8 V Regulator, the common-base transistor present in both the +87 V and the +42 V Regulators is not required. Current limiting in the −8-V supply occurs at about 480 mA.

−5 V Regulator

Operation of the −5 V Regulator is similar to that of the +5 V Regulator. Current limiting in the −5-V supply occurs at about 2 A.

+5 V Inverter Feedback

Operational amplifier U1371C and associated components are configured as a frequency-compensated voltage-sensing network. The circuit monitors the +5-V digital power supply line from the rectifiers and provides feedback to the Preregulator Control IC (U1030) via opto-isolator U1040 (both on diagram 9). The feedback is used to slightly vary the voltage-sensing characteristics of the Preregulator Control circuitry. The feedback (FB) signal slightly varies the voltage to the Inverter output transformer and holds the output of the 5-V secondary windings at an optimum level. Output levels of the other secondary windings are related to the +5-V_D level and are also held at their optimum values. This technique minimizes power losses in the series-pass transistors and increases regulator reliability.

Power-Up Delay

The Power-Up Delay circuit, composed of Q1370, Q1376, U1371D, and the associated components, ensures that the various regulated power supplies have time to reach their proper operating voltages before signaling the Microprocessor that the supplies are up.

When power is first applied, the LINE UP signal from the Preregulator Control circuit goes HI, indicating that the power switch has been closed and that ample supply voltage is available for driving the Inverter transformer. The HI is applied to the base of Q1370, but since the collector is not properly biased yet, no transistor current will flow. As the Inverter begins to run, the various voltages from the secondary rectifiers begin coming up to their proper levels. A +2.5-V reference voltage is applied to operational amplifier U1371D pin 12 and forces the output high, biasing Q1376 on. The resulting LO at the transistor's collector signals the Microprocessor that the power supplies are not yet stable.

Before any of the Low Voltage Regulators may function properly, the +10-V reference voltage must be established as previously described. When the +15 V Regulator turns on, current flows through Q1370, and pin 2 of U1371D is pulled above the +2.5-V reference through divider R1370 and R1372. The output of U1371D goes low, turning off Q1376. The PWR UP signal at the collector goes HI, signaling the Microprocessor that the power supplies should now be operating properly.

When power to the instrument is turned off, the LINE UP signal goes LO (as explained in the Line Up Signal description). The falling LINE UP signal turns Q1370 off and drives the output of U1371D high. The output level from U1371D turns on Q1376 and pulls the PWR UP signal to the Microprocessor LO. This LO initiates the power-down sequence used to store the current front-panel setup conditions in EAROM and to shut down the instrument in an orderly fashion. The delay between the time that the PWR UP signal goes LO and when the regulated power supplies fall below their normal operating levels provides ample time for the Microprocessor to complete the power-down sequence.

Fan Circuit

The fan motor used in this instrument is a brushless, dc motor that uses Hall-effect devices to control its rotation speed. The two Hall-effect devices sequentially drive the four field-control transistors (U1690A, B, C, and D) which in turn control field current to the fan motor windings. The fan's speed is determined by the amount of drive current supplied by Q1698 and varies with ambient temperature.

As the ambient temperature in the cabinet increases, the resistance of RT1696 decreases, and additional base drive is provided to Q1698. The transistor conducts harder, and the fan's motor speed is increased to provide more cooling capacity.

The back EMF produced by the motor field windings is also proportional to motor speed. This back EMF is rectified by diodes CR1691, CR1692, CR1694, and CR1696 and is applied to the base node of Q1698 via R1697. This current opposes the normal bias current of the transistor and acts as a form of negative feedback to stablilize the motor speed from cycle to cycle.

POWER DISTRIBUTION

Schematic diagrams 11 and 12 illustrate the power distribution of the 2465. The connections to the labeled boxes (representing the hybrids and ICs) show the power connections to each device, while connections to non-power lines are shown by the component and schematic number. Power supply decoupling is done with traditional LRC networks as shown on the diagrams.

Several intermediate supply voltages are generated by devices shown on diagrams 11 and 12. An approximate +32-volt supply for the A and B Sweeps is developed by emitter-follower Q700 and its associated components. Zener diodes VR125 and VR225 develop approximate +6.2-volt supplies for the CH 1 and CH 2 Preamps respectively, and zener diode VR2805 establishes an approximate −6.8-volt supply for U2800 and U2805.

INTERCONNECTIONS

Schematic diagram 13 illustrates the circuit board interconnections of the 2465. Connector numbers and cabling types are shown.