SECTION III
THEORY OF OPERATION
Model 112

Figure 1 is a basic block diagram of a function generator capable of delivering triangle, square and sine wave outputs. A discussion of the basic block diagram leads to easier understanding of the Models 112, 114, 115 and 116.

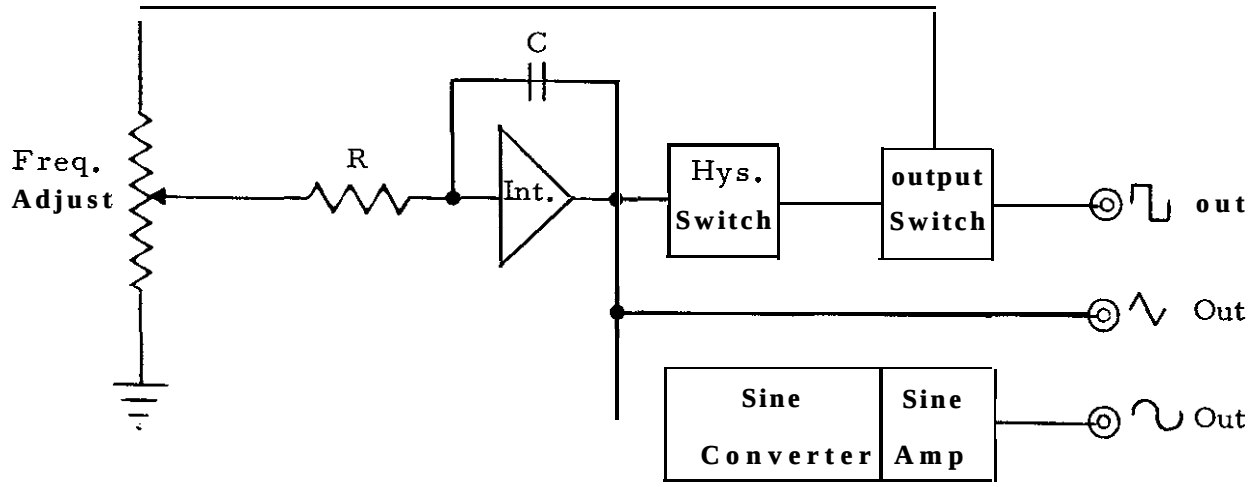

FIGURE 3-1

The heart of the basic function generator shown above in figure 1 is the integrator, a high gain, wide band d-c amplifier in an operational amplifier configuration connected for integration. Application of the negative half cycle of a square wave to resistor R results in a current directly proportional to the d-c level of the negative portion of the square wave and inversely proportional to the value of resistor R. The operational amplifier configuration offers a very high input impedance and most of the current in resistor R flows in and charges capacitor C. The right-hand side of capacitor C, and therefore the output point of the amplifier, is a positive going voltage slope. At a predetermined level, the positive going slope switches the bi-stable hysteresis switch which in turn switches the output switch, and the square wave switches to its positive half cycle. The current in resistor R changes direction and capacitor C charges in the opposite polarity. The output of the integrator is now a negative going voltage slope completing the triangle waveform. When the negative going slope reaches a predetermined level, it switches the hysteresis switch, which in turn switches the output switch, and the negative portion of the square wave is once again applied to resistor R. With the hysteresis switching levels fixed, the generated frequency is governed by the values of R and C and the amplitude of the applied square wave. With fixed values of R and C, varying

the amplitude of the square wave picked off and applied to the integrator by the frequency adjust pot (shown in figure 1) will vary the frequency. By changing either the value of R or C, the range of frequencies over which the unit will operate with the same frequency adjust pot can be changed. A square wave is available from the output switch and a triangle wave at the output of the integrator. The triangle wave is also fed into a converter which shapes it into a sine wave. Some attenuation is involved, therefore, a sine amplifier is added and a sine wave output is available.

The Model 112 uses analog control of frequency rather than the frequency pot shown in figure 1. Figure 2 is a basic block diagram of the Model 112, without the trigger mode.

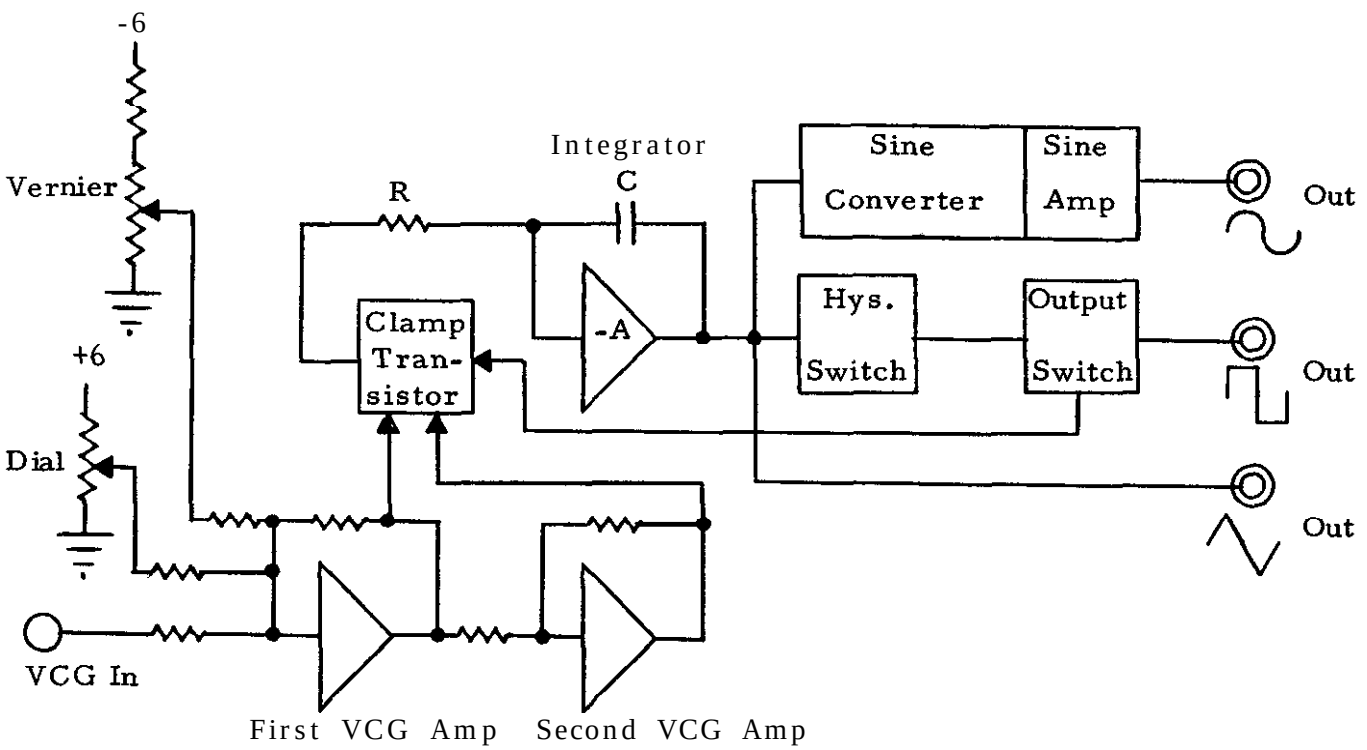

FIGURE 3-2

Basic operation is the same with the exception of frequency control. Changing the range over which the analog frequency control operates is done with the "Freq Hz" switch whichchanges the value of R or C, or both. The square wave is not applied to the integrator, but alternately turns on one of a pair of transistor clamps. The transistor clamps connect the output of two operational amplifiers alternately to the input of the integrator. The negative portion of the square wave turns on a clamp that connects the output of the first VCG amplifier to the integrator input. The positive portion of the square wave turns on a clamp that connects the output of the second VCG amplifier to the input of the integrator. The result is a square

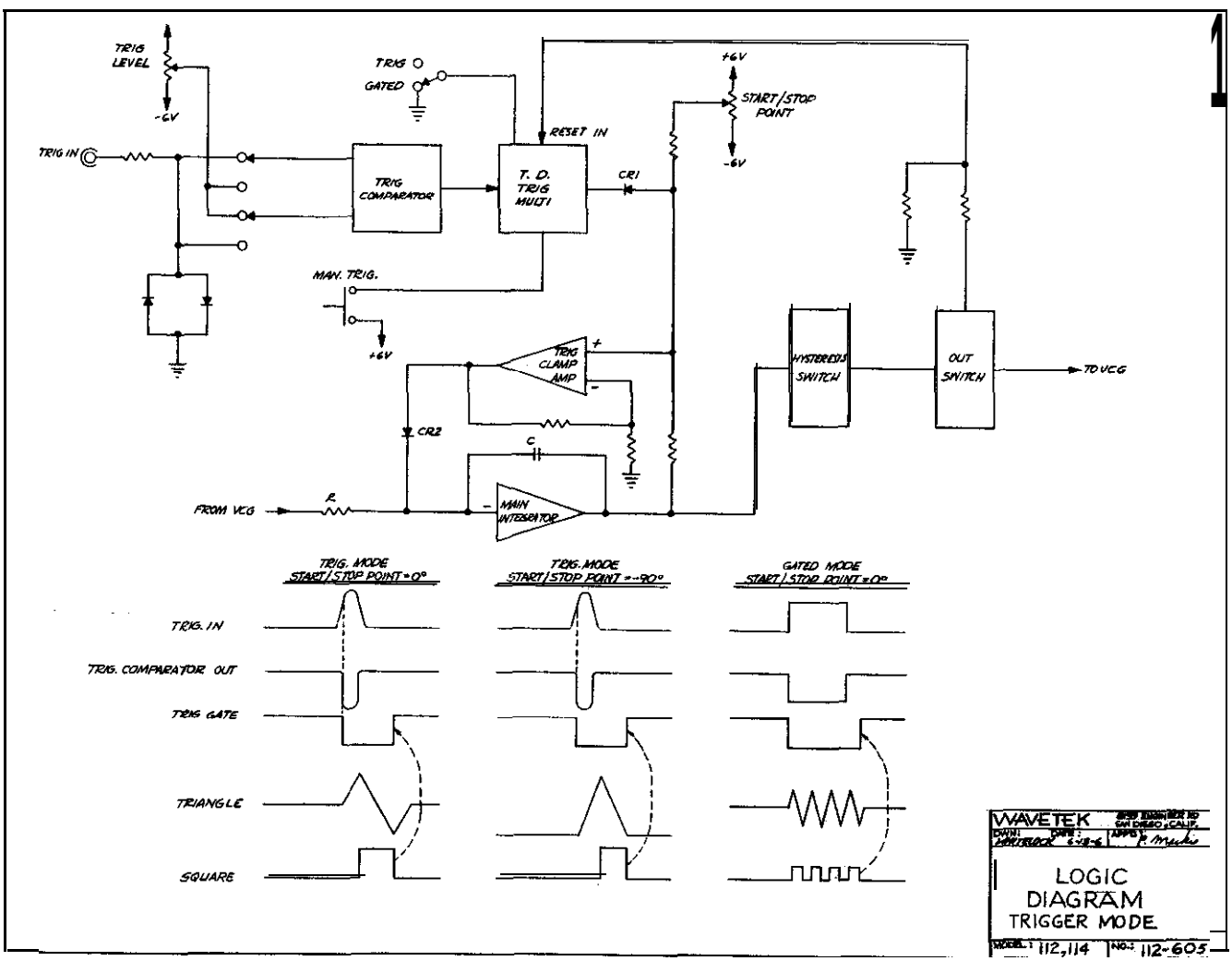
TRIG LEVEL
-6V
TRIG
GATED
+6V
START/STOP POINT
-6V
RESET IN
TRIG IN
TRIG COMPARATOR
T. D. TRIG MULTI
CR1
MAN. TRIG.
+6V
TRIG CLAMP AMP
HYSTERESIS SWITCH
OUT SWITCH
TO VCG
CR2
C
FROM VCG
R
MAIN INTEGRATOR
TRIG. MODE START/STOP POINT = 0°
TRIG. MODE START/STOP POINT = -90°
GATED MODE START/STOP POINT = 0°
TRIG. IN
TRIG. COMPARATOR OUT
TRIG GATE
TRIANGLE
SQUARE
WAVETEK
LOGIC DIAGRAM
TRIGGER MODE
MODEL: 112,114
NO.: 112-605

Figure 3-3

wave applied to the integrator, the amplitude of which is determined by the levels at the outputs of the two VCG amplifiers.

The VCG amplifiers are similar d-c wide band amplifiers in inverting operational amplifier configurations. The first amplifier has a gain of approximately 3/5 and the second, a gain of unity. Applying +5 volts to the input of the first VCG amplifier results in a -3 volts at its output. This -3 volts is applied to the second VCG amplifier resulting in t3 volts at its output. The square wave under these conditions would operate the clamps and a ±3 volt square wave would be applied to the integrator. Since the VCG amplifiers are wide band, an a-c signal up to 100 KHz can be applied and the generator frequency modulated. The input summing node of the first VCG amplifier sums the dial input, the vernier input, and any voltage, applied to the VCG input jacks. With no VCG input voltage applied, the dial and the vernier control the frequency.

Refer to the Block Diagram of Model 112.

The blocks on the left-hand side of the dial pot and frequency vernier in the diagram are concerned with triggered operation. The blocks on the right are similar to the blocks just discussed with the addition of an output power amplifier, a -1 amplifier, and an offset sine wave circuit.

The offset sine wave circuit adjusts the level of the sine wave available from the sine amplifier so that its most negative excursion is ground and its most positive excursion is t2.5 volts.

The -1 amplifier inverts the selected waveform and provides an inverted output to its BNC connector on the i-ear panel. When selected, the -1 amplifier also delivers the input to the output power amplifier through its attenuator allowing the power amplifier to deliver waveforms in phase or 180° out of phase with the waveforms available at the fixed output BNC connectors at the rear panel.

The output power amplifier is capable of delivering 30 volts peak to peak sine, square, and triangle waves into a 600Ω load, 10 volts peak to peak into a 50Ω load. It will also deliver a 15 volt peak ramp waveform into 600Ω, 5 volts peak into 50Ω.

The triangle wave is fed to the ramp circuitry where its d-c levels are adjusted so that the most positive excursion of the triangle is ground and the most negative excursion is -2.5 volts. The positive going portion of the triangle is then chopped to ground resulting in a -2.5 volt ramp, the phase corresponding to the negative going slope of the triangle wave.

The trigger circuitry and its switches are shown at the left in the diagram. Figure 3-3 is a simplified block of the triggered mode with waveforms. When the 112 is in the triggered mode and ready, the output of the tunnel diode trigger gate is near ground potential. CR1 in figure 3-3 is non-conducting and CR2 is on, clamping the output of the integrator at the level set by the start-stop point potentiometer,

through the trigger clamp amplifier. When a triggering signal is applied to the trigger input connector which overcomes the level set by the trigger level control, the tunnel diode trigger gate steps to approximately -6 volts turning on CR1. The output of the clamp amplifier is driven negative, disconnecting or turning off diode CR1 which allows the integrator to start. The d-c level at which it starts is set by the Start-Stop point potentiometer. The tunnel diode trigger gate is reset by the square wave from the output switch. Resetting the trigger gate enables the clamp amplifier once again; however, the triangle output must reach the Start-Stop level before the clamp amplifier takes control. This insures that the integrator output always starts and stops at the level set by the Start-Stop point potentiometer. The Start-Stop point potentiometer allows adjustment of $\pm 90^{o}$ to the starting and stopping point of the integrator. By using the output of the -1 amplifier (selected output) or by using the inverted output of the power amplifier, the Start-Stop point becomes adjustable over 360^{o}. When the mode switch is in the gated position an integer number of cycles is generated governed by the width of the trigger pulse or gate applied to the trigger connector. When in the triggered position, one cycle is generated each time a triggering signal is applied or the manual trigger is depressed. Adjustment of the trigger level control when in the gated mode allows a limited range for changing the number of cycles for a given pulse width.

DETAILED CIRCUIT DESCRIPTION

Refer to Model 112 Main Board schematic diagram.

INTEGRATOR, MAIN BOARD

Q1 through Q10 and their associated circuitry make up the wide band d-c integrator amplifier. The "Freq Hz" switch on the front panel selects the appropriate integrating resistors and capacitors for frequency ranging.

Q1 and Q2 are a Darlington input pair for the minus input; Q 4 and Q 3 are a Darlington pair in the plus input. Transistors Ql through Q4 are low current, high gain, wide band transistors which allow the inputs to operate with less than 40 nano amps of source current. The collectors of Q2 and Q3 work into a complex load made up of R1, R3, R4, C3, and the input impedance of Q5 and Q6. Q5 and Q6 form a differential amplifier stage driving the differential stage made up of Q7 and Q8. The output is taken off single ended at the collector of Q7 through the push-pull emitter follower, Q9 and Q10. CR1 and CR2 provide the bias voltage for Q9 and Q10 to prevent crossover distortion. R8 allows the d-c levels in the two sides of the amplifier to be balanced throughout. The triangle output is connected to pin 1. It is also fed through R22 to the sine converter and to the Hysteresis switch made up of Q25 through Q30.

HYSTERESIS AND OUTPUT SWITCH, MAIN BOARD

The transistors in the Hysteresis switch are connected to form a bi-stable switch. Either the Q25, Q26 side or the Q28, Q30 side can be on but not both at the same time. When the positive going triangle reaches the firing level set by R77, the

Q26 side turns on and the Q28 side turns off. The triangle starts its negative slope and when it reaches the firing level set by R78, the Q28 side turns on and the Q26 side turns off. The Hysteresis switch is d-c coupled to the bi-stable output switch made up of Q31 through 434. The square wave available from this output switch has a risetime of less than 10 nano seconds. The square wave is coupled to pin 10.

The 10 volt peak to peak square wave is differentiated, amplified and clipped by Q35, R96, C25, CR15, R101, C27, and R110 to provide a -10 volt sync spike which has a duration of less than 5 μsec. The sync pulse is coupled to pin 13. The square wave is also coupled to a push-pull super emitter follower made up of Q36 through 439. R104 allows the output amplitude to be adjusted, R99 adjusts the waveform so that it is symmetrical about ground. Diodes CR.16 through CR19 provide temperature compensation. The output of the super emitter follower is a 5 volt peak to peak square wave with a risetime Less than 15 nano seconds, coupled to pin 11.

SINE CONVERTER AND AMPLIFIER, MAIN BOARD

Transistors Q11 through Q18 are emitter followers in the sine converter that bias and temperature compensate the clipping diodes, CR3 through CR10. Diodes CR3, CR5, CR7, and CR9 clip the positive portion of the triangle at points set by the pots in the base of their associated emitter follower transistors. Diodes CR4, CR6, CR8, and CR10 clip the negative portion of the triangle. The diodes do not, however, clip the most positive and negative peaks of the triangle. Therefore, the input to the sine amplifier is a sine wave with small peaks at the top and bottom. The sine wave is fed to the plus input of the sine amplifier through R64. The sine amplifier is a d-c wide band operational amplifier connected in a potentiometric configuration. R69 is the feedback resistor. The peaks on the sine wave are also seen at the collectors of the emitter followers in the sine converter. These peaks are coupled through R54 and R56 to the minus input of the sine amplifier and peak cancellation occurs in the amplifier giving a clean sine wave at the output. The sine wave is coupled to pin 9. R60 adjusts the sine wave symmetry about ground and R64 adjusts the sine wave amplitude.

POWER SUPPLY AND OUTPUT AMPLIFIER BOARD (Refer to schematic diagram)

A-c voltage is coupled from the transformer to pins 14 and 15 to drive the bridge rectifier made up of diodes CR1 through CR4. Filtering is provided by Cl and C2 Q1 is a transistor connected and operated as a zener diode providing a reference voltage for the t6 volt supply. Q2 and Q3 make up a comparator type differential amplifier. Q2 and Q3 drive Q6 and Q7 which in turn drive the +6 volt pass transistor, Q10. R24 allows the base of Q3 to be adjusted slightly negative with respect to ground. Q1 has a zener voltage of approximately 6.3 volts setting the base of Q2 slightly negative. R24 is adjusted to give an output of t6. 00 volts. If the +6. 00 volts tries to increase due to a change in line voltage or load current, the collector of Q1 becomes more positive. The base of Q2 becomes less negative (moves in a positive direction with respect to ground) and Q2 draws more current. The collector

of Q2 moves less positive and this change is coupled through Q6 and Q7 to the base of Q10. This increases the resistance of Q10, returning the supply to +6.00 volts.

Q4 and Q5 form a comparator type differential amplifier in the -6. 00 volt regulator. The base of Q4 is returned to ground through R6. The divider of R26 and R27 between the plus and minus 6 volt supplies sets the base of Q5 at ground. R9 allows a small adjustment of the currents in Q4 and Q5 to set the output at -6.00 volts. An increase in the -6 volts due to line voltage variation or load current variation, results in the base of Q5 moving negative. The collector of Q5 moves less negative (in a positive direction). This change is coupled to the bases of Q11 and Q12. Q11 and Q12 form a Darlington connected pass transistor pair for added gain. The positive going change, increases the resistance of Qll and Q12, returning the output to -6.00 volts.

OUTPUT AMPLIFIER

Q13 through Q18 form an operational output amplifier with a gain of approximately -6 set by feedback resistor R37 and the input resistor made up of R31 and R32. Transistors Q13 and Q14 are a differential input stage driving a second differential stage of Q15 and Q16. The output is taken off single ended at the collector of Q16 and coupled to the push-pull emitter follower, Q17 and Q18. Diodes CR5 and CR6 provide bias for the push-pull emitter follower to prevent crossover distortion. The output is coupled through R50 and R51 to pin 3. The input is selected on the front panel and comes in on pin 5. Cl0 and Cl1 allow the amplifier to be high frequency compensated and are adjusted to give the best Gaussian response when a 1 MHz square wave is applied. A-c is coupled from the transformer to pins 1 and 2 and drives the bridge rectifier made up of diodes CR7 through CR10. The outputs of the bridge rectifier are filtered by Cl4 and Cl5 providing the supply voltages for the output amplifier. R41 is the d-c balance control allowing the output to be adjusted for symmetry about ground. R41 is a screwdriver adjustment available from the rear panel. D-C OFFSET MODIFICATION. To convert the d-c balance control, R41, to a d-c offset control, remove R40 and R42, 10K 1% and replace with 2K 5% carbon resistors. R41 will now serve as a d-c offset control allowing the. power amplifier output to be offset approximately ±5 vdc. It should be remembered that using an offset control limits the available peak output signal. The output will deliver 100 ma into a short circuit and 32. 5 volts peak to peak into an open circuit. When terminated in 600Ω, the amplifier will deliver 30 volts peak to peak. When terminated in 50Ω, the amplifier will deliver 10 volts peak to peak. When offset +5 vdc, the output when terminated in 600Ω is only capable of swinging +10 volts peak. When offset t5 vdc and terminated in 50Ω, the output is at its positive going limit point.

The input available on pin 5 and delivered to the power amplifier is coupled through an attenuator potentiometer on the front panel. The signal delivered to the attenuator pot is selected by the front panel function selector switch. In the “in phase” position of the selector switch, the signals are passed through a -1 amplifier prior to being delivered to the power amplifier; therefore, the output of the power amplifier is in phase with the fixed outputs available at the rear panel. In the “out of phase”

position of the function selector switch, the selected signals are delivered directly to the function potentiometer from the signal sources and the signals are inverted in the power amplifier resulting in an output that is out of phase with the fixed outputs at the rear panel. The function selector switch also selects the signal that is delivered to the -1 amplifier and available on the rear panel connector marked "Selected Output". The signal when selected and delivered to the selected BNC connector on the rear panel is identical to, but 180° out of phase with the other fixed outputs on the rear panel.

VCG BOARD

Refer to the VCG schematic. The two VCG amplifiers are similar operational inverting amplifier configurations. The basic operational amplifier is a μA702C integrated circuit. IC1 is the first inverting operational VCG amplifier, and serves as the main frequency control. The dial voltage from the front panel is available on pin 9 and applied through R6 to the summing node of the operational amplifier.

The voltage from the vernier potentiometer on the front panel is available on pin 8 and applied through R5 to the summing node of the operational amplifier. Any voltage applied to the front panel VCG input connector is applied to pin 4 through R8 and R7 to the summingnode of the operational amplifier. The resultant output is the sum of the input voltages.

In the case of the more complex Models 115 and 116, a phase lock voltage is present on pin 6, and coupled through the filter network made up of RI, RZ, R3, Cl and C2 to the summing node of the operational amplifier.

R4 is not included on the VCG board in the other models. R8 allows a calibration of the effect of a VCG voltage applied on the front panel to the output frequency of the instrument. CR1 and CR2 provide protection in case of an overvoltage applied at the VCG input terminal.

R9, R10 and R11 provide a zero adjust network for the non-inverting input to the operational amplifier. R51, R52 and R53 provide source current for the input of the first amplifier allowing summing node zero adjustment. R12 and R13 are the feedback resistors in the first operational amplifier. R13 is adjusted for frequency calibration at the high end of the dial, while R9 is adjusted for frequency calibration at the low end of the dial.

Pin 7 is the output point of the operational amplifier and Q1 serves as an emitter follower to prwide added current swing in the negative direction at the output of the first VCG amplifier. The output at the emitter of Ql is coupled

through saturated transistor Q3 to the feedback resistor R13 and also to the input resistor of the second VCG amplifier made up of R14 and R15.

The square wave output from the output switch on the Main Board is available on pin 13, and applied through R17 to the base of Q2. When the square wave is negative Q2 is turned on and saturated and the output of the first VCG amplifier is coupled through Q2 to pin 7, the VCG out terminal.

When the square wave is positive, Q2 is turned off. Q2 and Q3 serve as inverted switches. Q2, operating as an inverted switch. has a very low saturation voltage; however, to compensate for this voltage, Q3 is placed in the feedback loop of the first operational amplifier. This also temperature compensates the first VCG amplifier.

The first operational amplifier has a gain of approximately 3/5 with respect to the dial input, while the second operational amplifier has a gain of unity. The output of the first VCG amplifier is coupled through R14 to R15 to the summing node of the first operational amplifier.

R25 serves as a feedback resistor in the second operational amplifier. Q4 and Q5 serve the same purpose in the second operational amplifier as Q2 and Q3 in the first. However, the output of the second operational amplifier is moving positive, therefore, NPN transistors are used.

When the square wave from pin 13 is positive, Q4 is turned on and saturated coupling the output of the second VCG amplifier to pin 7, the VCG out terminal. Therefore, the signal on pin 7 is a square wave whose frequency is determined by the switching rate of the output switch set on the Main Board and whose amplitude is dependent on the levels at the output of the two VCG amplifiers.

Since the second VCG amplifier has a unity gain, it will provide an output of opposite polarity but of the same magnitude as the output of the first VCG amplifier. The square wave on pin 7 is that square wave applied to the input of the integrator on the Main Board and in turn determines the frequency of the generator.

R46 and R24 serve as the zero adjust control for the second VCG amplifier. R14 allows adjustment of the symmetry at the high end of the dial, while R46 allows adjustment of the output frequency symmetry at the low end of the dial.

IC1 and IC2, the two integrated circuits,' require a t12 volt supply. The positive high voltage supply from the power amplifier on the power supply and power amplifier board is coupled to pin 5 of the VCG board, on to the collector of Q6 and in turn, to pin 8 of both the integrated circuits.

Q6 is a transistor connected and operated as a 6 volt zener diode. The emitter of Q6 is returned to t6 volts; therefore, its collector will be 6 volts above this level or +12 volts with respect to ground. Q6 thus serves as the +12 volt regulating element for the supply for the integrated circuits. When properly calibrated the system is so well balanced that it cannot start when the machine is first turned on. The square wave output from the VCG clamp transistor on pin 7 drives the input to the integrator.

R22 is added to provide an initial unbalance to allow the integrator to start. Once the machine is running, resistors R18 and R28 offset this unbalance introduced by R22 and the system is once again balanced.

RAMP CIRCUIT

The triangle wave is available on pin 1 and is offset and attenuated by resistors R31, R32, R33. R34 and R35 so that its most positive excursion is zero volts d-c and, its most negative excursion is -2. 5 volts. Transistors Q7 and Q8 are turned on and saturated by the negative portion of the square wave applied to their bases through R37 and R38. When turned on, Q7 and Q8 chop the positive going portion of the offset triangle to ground. The result is a negative going 2. 5 volt ramp in phase with the negative going portion of the triangle output. The ramp is delivered to 'pin 10 through two emitter followers, Q9 and Q10. The two opposing base to emitter voltages insure that the ramp starts at ground and the emitter followers temperature compensate each other.

TRIGGER BOARD (Refer to Trigger Board schematic)

Ql and Q2 make up a comparator type amplifier with Q3 providing a constant current source. The divider of R2 and R4 provide the bias level for the base of Q3. When the front panel trigger slope switch is in the plus position, the triggering signal is fed via pin 12 through R9 to the base of QZ. The base of Q1 is returned to the trigger level control via pin 13. When a positive going input triggering signal overcomes the reference level established by the trigger level control in the base of Ql. the current of Q2 decreases allowing its collector to move in the negative direction. In the triggered mode pin 15 is open and Q5 is biased to saturation providing a current path for CR2, the tunnel diode.

Tunnel diode CR2 is quiescently biased in its low voltage state. A negative going excursion at the base of Q5 coupled through CR1 causes CR2 to switch to its high voltage state. Tunnel diode CR4 is quiescently biased in its low voltage state. When tunnel diode CR2 switches to its high voltage state, this change is coupled through C4 and results in CR4 switching to its high voltage state turning on transistor Q7. The output coupled to pin 10 is initially at ground potential.

When Q7 turns on, its collector moves in the positive direction and the output steps to approximately -6 volts. A reset pulse is coupled in through pin 21 through C5 to the base of Q6. This is a negative going reset pulse coincident with the negative going portion of the output square wave, This reset pulse results in the collector of Q6 moving positive and resetting the tunnel diode CR4 to its low voltage state. Transistor Q7 returns to its off state and the output returns to ground.

When the front panel mode switch is in the gated position, the base of Q5 is returned to ground by grounding pin 15. Transistor Q5 is turned off removing the current path for tunnel diode CR2. The triggering will now couple through CR1 and cause CR4 to switch to its high state; however, CR4 will remain in its high state until the triggering signal is removed. Therefore, the trigger gate will have a duration determined by the width of the trigger pulse applied at the input.

TRIGGER CLAMP AMPLIFIER

The trigger clamp amplifier is a d-c operational amplifier connected in a potentiometric configuration, Transistors Q10 and Q11 form an input differential pair driving the differential pair of Q12 and Q13. The collector of Q12 is returned to ground while the output is taken off single ended from the collector of Q13, which drives the push-pull emitter follower made up of Q14 and Q15.

CR7 and CR8 provide the bias for Q14 and Q15. R43 is the feedback resistor. R29 allows the amplifier to be d-c balanced so that the start-stop point potentiometer is adjustable between $\pm 90^{o}$ of the generated cycle. The output is taken off the junction of R40 and R41 to pin 3. In the trigger and gated mode, the output is coupled through a diode to the minus input of the main integrator. The output of the main integrator is coupled in on pin 7 through R38 to the base of Q11. The trigger gate is coupled through a diode to pin 6 and the base of Qll as well.

The start-stop point potentiometer provides the reference level at pin 1 and, therefore, at the plus input of the trigger clamp amplifier. In the triggered or gated mode, the trigger gate is initally at ground potential allowing the start-stop point potentiometer to set the reference level at the plus input of the trigger clamp amplifier. This sets the level at the output of the trigger clamp amplifier and, therefore, clamps the minus input of the main integrator to the level set by the start-stop potentiometer through the diode from the output of the trigger clamp amplifier. R29 allows the trigger circuit to be balanced so that the start-stop point moves between - 90 and +90 degrees.

When a triggering signal is applied, the trigger gate steps to a -6 volts driving the plus input of the trigger clamp amplifier negative and essentially disconnecting or cutting off the diode to the minus input of the main integrator

allowing the integrator to start. When the trigger gate is reset, the trigger clamp amplifier is once again enabled; however, the triangle wave coupled in on pin 6 must overcome the reference level set by the start-stop potentiometer before the clamp amplifier will once again clamp the main integrator. This insures that an integer number of cycles are generated and that the start-stop point will always be set by the start-stop point potentiometer.

MINUS 1 AMPLIFIER

The -1 amplifier has two main functions: 1) to provide a differential or out of phase output with the fixed output at the rear panel, and 2) to allow the power amplifier to generate signals that are in phase or 180" out of phase with the fixed outputs on the rear panel. The start-stop point potentiometer only allows the start-stop point to be varied $\pm 90^{\circ}$. By using the output from the -1 amplifier or the inverted output from the power amplifier, the start-stop point can be made to operate over 360° since the start-stop point is inverted as well as the signal.

The - 1 amplifier is an operational inverting d-c amplifier with a gain of unity set by potentiometer R63. Q20 and Q21 form a differential input pair driving the differential pair of Q18 and Q19. The output is taken off single ended from the collector of Q18 through push-pull emitter follower Q16 and Q17. CR9 and CR10 provide the bias for the push-pull emitter follower to prevent crossover distortion. R63 and R64 make up the feedback resistor while R62 is the input resistor. Cl5 and Cl8 are to shape the frequency response characteristics of the amplifier. C 12 places the plus input of the amplifier at signal ground. R48 allows the amplifier to be d-c balanced so that the signal is symmetrical about ground.

OFFSET SINE CIRCUIT

The output from the sine amplifier is coupled in on pin 18 where it is attenuated by R52 and R55. R53 and R54 returned to +6 volts, offsets the sine wave as well. R54 allows the amount of offset to be precisely adjusted. The output on pin 15 is an attenuated sine wave whose most negative excursion is ground and whose most positive excursion is +2.5 volts. This provides a convenient output on the rear panel for such application as sine-square testing.

PHASE LOCK AMPLIFIER

Since the phase lock amplifier applies only to the Models 115, 115B, 116 and 116B, its discussion will be taken up in that section which applys to those models. The phase lock amplifier is not included on the trigger board in the Models 112, 112B.

BATTERY REGULATOR BOARD

The battery regulator delivers plus and minus 6 volts dc to the Models 112B, 115B and 116B from a pack of 1.2 ampere-hour rechargeable Nickel Cadmium batteries. The t6 and -6 volt regulators are equivalent circuits and operate in the same manner as the ac regulators on the standard supply board. Q13 is the series pass transistor for the plus supply and Q21 is the series pass transistor for the minus supply. Q17 and Q25 act as zener references for the two supplies. R19, Q9 and CR9 make up the "starting" circuit. This assures that the supplies achieve full output when first turned ON. R27, Q14 and R42, Q22 provide "current limiting" circuit which engages when the voltage across R27 (or R42 for minus supply) reaches approximately 0. 6 volts. Q14 (Q22 for minus supply) conducts and limits the current through the series pass transistor. This occurs at approximately 340ma.

Transistors Ql through Q7 make up the charging circuit. The batteries are always being charged as long as SW1 is on and the line cord is plugged in an ac source. The transformer delivers center-tapped ac to pins 1 and 2. The ac is rectified by diodes CR1, CR2, CR3 and CR4 and filtered by Cl and C2, providing t24 and -24 volts dc. R10, R11, R14 and R15 sample the charging current through the batteries and provide forward bias to Q6 and Q7 through divider R8, R9, R13 and potentiometer R12. When potentiometer R12 is turned maximum counter-clockwise, the current through the current sampling resistors should be approximately 40ma to bias Q6 and Q7 on. When this occurs the current through Ql, Q2, Q3 and Q4 is reduced and an equilibrium charge rate is reached. Turning R12 fully clockwise adjusts the bias on Q6 and Q7 such that approximately 12Oma of charge current is required for equilibrium. Charge rate is adjustable from the rear panel.

This method sampling the battery current provides an essentially constant charge rate regardless of load current. It also yields an overall negative temperature coefficient which is necessary for extended battery life.

When SW1 is in the OFF position, and the power cord is connected to an ac source, R6 and R18 provide a "trickle" charge of approximately 6ma. This maintains the batteries at full charge during idle periods.

Since there is no 30 volt output amplifier in the battery instruments, the attenuator wiper arm is connected to the output binding post through a 470Ω resistor. This provides a maximum output of 5 volts peak to peak at 600Ω output impedance (2.5 volts ramp).

FRONT PANEL BOARD

The Model 112 front panel board contains the trigger input connector, the trigger slope switch and trigger level control, the start-stop point

potentiometer, the mode switch, the function selector for the power amplifier and for the selected differential output on the rear panel, the VCG input connectors, the manual trigger button, the frequency vernier, the timing capacitors and resistors for the main integrator, the main frequency dial, and the power amplifier output connectors.

The output of the power amplifier is available on pin 30 and coupled through R47 and R48 to the front panel connector. C9 attenuates the very high frequencies to insure good high frequency performance. The parallel resistance of R47 and R48 in series with a pair of parallel 49.9Ω resistors on the power supply and output amplifier board make up the 50Ω output resistance of the power amplifier. The jumper around R46 is removed when a 600Ω output resistance is desired.

The fixed amplitude triangle, sine, square wave, and ramp are fed to the function selector switch via pins 1, 22, 25, and 26. The selected function is coupled by the function selector switch to pin 32 which returns to the input of the -1 amplifier. In the "in phase" position of the function selector, the power amplifier is driven by the output of the -1 amplifier coupled in on pin 31. Note that the function selector couples the output of the - 1 amplifier to the attenuator R40, and its series resistor R41 in the "in phase" positions.

The center arm of the attenuator couples to pin 28 which is the input of the power amplifier. In the "out of phase" positions of the function selector, the fixed amplitude functions are fed directly to the power amplifier attenuator and on to the input of the power amplifier. Therefore, in the "in phase" position of the function selector, double inversion taken place; one inversion takes place in the -1 amplifier, and the second inversion takes place in the power amplifier.

With reference to the power amplifier output, only one inversion takes place in the "out of phase" position of the function selector and that is in the power amplifier itself. Note that the function selector switch, however, always delivers the selected function to the -1 amplifier so that the output at the rear panel is a signal 180° out of phase with the fixed outputs and is that function selected by the front panel function selector.

Wafers 1 and 2 of the frequency hertz switch select the appropriate integrating resistors and capacitors for the different frequency ranges. Wafer 3 selects the resistors to balance the source current in the plus side of the main integrator with different values of integrating resistors are selected in the minus input. Wafer 4 provides compensating resistors from the VCG output to ground so that the VCG clamp transistors always see the same loading.

The frequency dial attenuates the +6 volt supply and supplies an input voltage to the VCG amplifier. The VCG input connector provides an external

connector to apply voltages to the VCG to control frequency. R9 and C10 provide high frequency compensation. The manual trigger, when depressed, allows one cycle to be generated without an external triggering source required. The start-stop point potentiometer provides the reference level on the trigger clamp amplifier to determine the starting and stopping point of the integrator when in the triggered or gated mode. Diode CR3 and resistor R49 are between the trigger gate output and the plus input of the trigger clamp amplifier. The trigger slope switch selects that slope of the input triggering waveform it is desired to trigger on. The trigger level control provides a reference level for the opposite input to the trigger comparator so that different levels of triggering signals can be used. CR1 and CR2 insure that a high voltage applied to the trigger input connector will not destroy the trigger circuitry. The mode switch selects either triggered, gated, or continuous modes. The difference between the triggered and gated mode was discussed when pursuing the trigger board. In the continuous mode the generator operates like the conventional Model 111.

MOTHER BOARD

The mother board in the Model 112 provides the interconnections between the various boards used in the Model 112 and also contains the impedance determining resistors in series with the outputs. The outputs are connected from the rear of the mother board to the rear panel board and its connectors. The exception is the power amplifier output whose resistors are found on the front panel.

REAR PANEL BOARD

The rear panel board contains the eight BNC connectors for the eight fixed outputs. It also contains some high frequency compensating components for clean high frequency waveforms.

Refer to Model 115 Block Diagram.

The operation and circuit description described for the Model 112 applies to the Model 115 as well. Model 115 users should first read the Circuit Description section of the Model 112 before pursuing the Model 115 Circuit Description. The Model 115 has all of the characteristics, outputs, and capabilities of the Model 112 with the addition of the Phase Lock Mode. The block diagram of the Model 115 is similar to that of the Model 112 with the addition of the phase lock amplifier and the phase lock capacitors. The mode switch has three positions in the Model 115: phase lock, continuous, and triggered. If the gated mode is desired, a separate switch allows gated operation when the mode switch is in the triggered position. There is also a phase lock indicator light for phase lock operation that indicates when the generator is not properly phase locked. When the mode switch is in the phase lock mode, the trigger level control becomes the phase adjust allowing the output phase of the instrument to be adjusted from 0 to 180 degrees with respect to the signal being applied to the phase lock input BNC connector. The phase lock control becomes adjustable over 360° when the inverted selected output on the rear panel is used or the inverted power amplifier output is used. When in the phase lock mode, a calibrated -90° phase difference between the output and the applied signal can be obtained by rotating the start-stop potentiometer fully counter-clockwise into its detent position. This throws a switch mounted on the back of the start-stop point potentiometer that places the phase lock mode in a 90° "cal" position.

In the phase lock mode the phase multivibrator is triggered by the signal applied to the front panel BNC input connector. The phase lock multivibrator is reset by the square wave. This output is coupled to the phase lock amplifier. The signal delivered to the phase lock amplifier is the difference between the firing point on the input signal and the reset point governed by the output square wave. These pulses are passed through the phase lock amplifier which is a low pass operational amplifier. The output of the phase lock amplifier is an analog voltage proportional to the difference in the firing point governed by the input signal and the reset point governed by the output square wave. With no input to the phase lock amplifier from the phase control potentiometer, the phase lock circuit is calibrated so that the output of the generator would have a -90° phase difference with respect to the applied input signal. When the phase control is in the zero degree position, a narrow pulse is applied to the phase lock amplifier, integrated to provide an analog voltage, which is applied to the VCG input and adjusts the phase of the output signal from the generator to be in phase with the applied signal at the front panel. When the phase adjust control is in the 180° position, a wider pulse is applied to the phase lock amplifier resulting in a larger voltage applied to the VCG amplifier and the phase of the output frequency is adjusted to be -180° out of phase with the applied signal on the front panel.

The figure on the following page is a basic block diagram of the phase lock mode with waveforms.

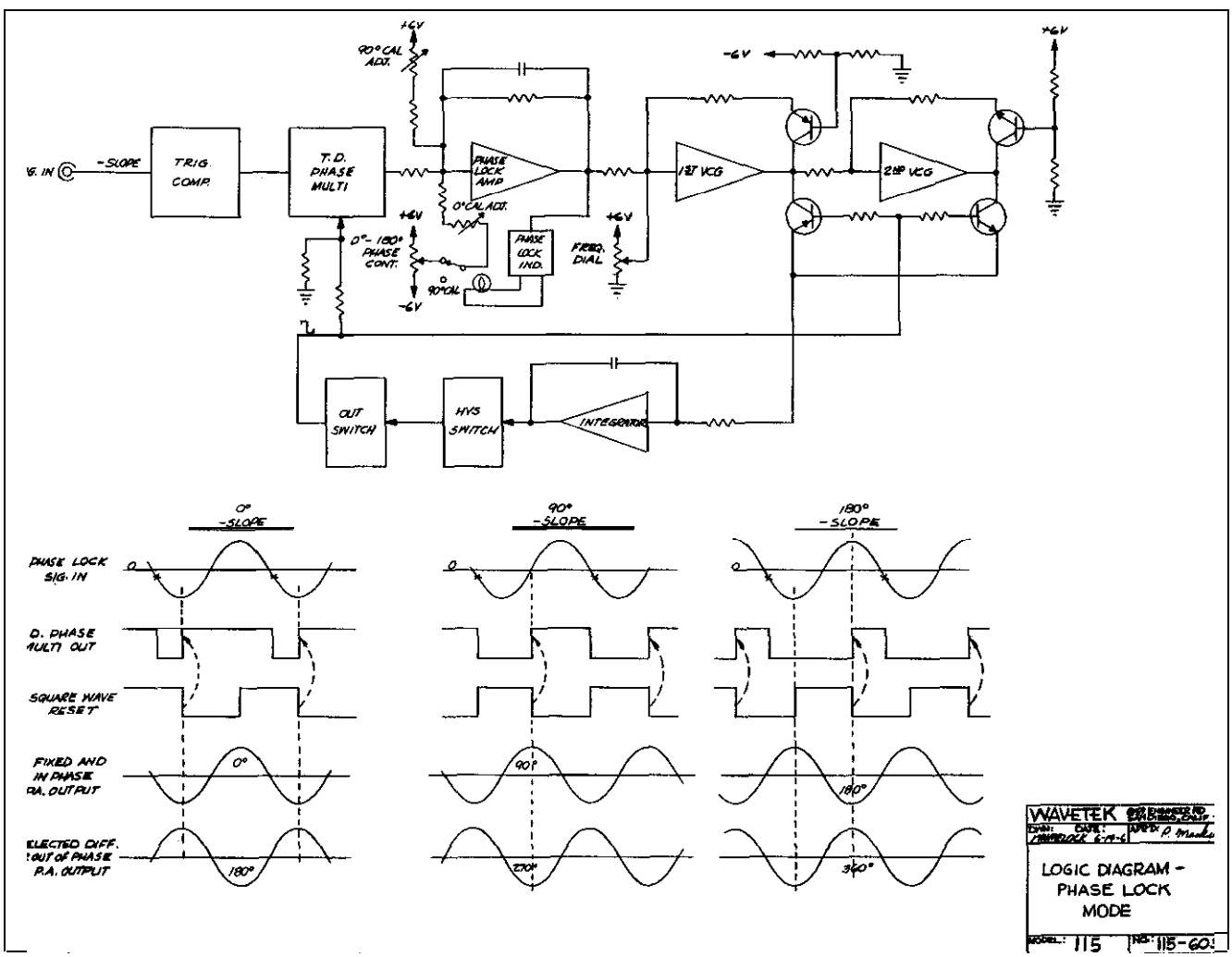
+6V
90° CAL ADJ.
-6V
+6V
V. IN
-SLOPE
TRIG. COMP.
T.D. PHASE MULTI
PHASE LOCK AMP.
0° CAL ADJ.
1ST VCG
2ND VCG
+6V
0°-180° PHASE CONT.
90° CAL
PHASE LOCK IND.
FREQ. DIAL
-6V
OUT SWITCH
HYS SWITCH
INTEGRATOR
0° -SLOPE
90° -SLOPE
180° -SLOPE
PHASE LOCK SIG. IN
D. PHASE MULTI OUT
SQUARE WAVE RESET
FIXED AND IN PHASE P.A. OUTPUT
ELECTED DIFF. OUT OF PHASE P.A. OUTPUT
0°
90°
180°
180°
270°
360°
WAVETEK
DRAWN:
DATE: 6-11-68
APPR. D. Meade
LOGIC DIAGRAM - PHASE LOCK MODE
MODEL: 115
NO: 115-601

Figure 3-4

For the greatest degree of accuracy the Model 115 should be operated in the phase lock mode with the trigger slope in the minus slopeposition. Note in the diagram that the minus slope of the applied phase lock signal in switches the tunnel diode phase multivibrator from 0 to approximately -6 volts. The negative going portion of the generated square wave resets the tunnel diode phase multivibrator. The output of the tunnel diode phase multivibrator is summed with the d-c level from the phase control and from the 90° "cal" adjustment at the minus input of the phase lock amplifier. The output is a d-c level established by the sum of the two voltages and the output of the tunnel diode phase multivibrator. The output of the phase lock amplifier drives the first VCG amplifier. The first VCG amplifier sums the input from the frequency dial, from the frequency vernier, and from the phase lock amplifier. Of course, it would also sum any applied voltage to the front panel VCG in connectors. In the 90° phase lock position of the start-stop point potentiometer, any input is removed from the 0 to 180 degrees phase control and the phase lock amplifier is automatically in the 90° phase lock condition. The waveforms on the left in the diagram show the conditions that exist when the Model 115 is in the phase lock mode with the phase control set at 0 degrees. The phase lock amplifier sums the voltage from the phase control and the output of the tunnel diode phase multivibrator. This establishes the phase of the output signal to be in phase with the applied signal at the front panel. This means, however, that the selected differential output on the rear panel and the out of phase power amplifier output are 180° out of phase with the signal applied to the front panel.

In the second set of diagrams the phase control is set at 90° and the output of the tunnel diode phase multivibrator is a symmetrical square wave. The phase of the output signal is now 90° with respect to the applied signal at the front panel referring to the fixed outputs and the in phase power amplifier output. The selected differential or out of phase power amplifier output is 270° with respect to the applied signal at the front panel. When the phase control is in the 180° position, the generated signal at the fixed outputs is 180° out of phase with respect to the signal at the input which sets a phase relationship with 360° for the output of the selected differential or out of phase power amplifier output with respect to the input signal. By adjusting the phase control and using the output that gives the desired phase difference, an output signal with a phase difference of 0 to 360 degrees can be obtained with respect to the input signal.

CAUTION

The trigger gated switch should be in the "triggered" position and the trigger slope switch should be in the minus slope position for calibration accuracy in the phase lock mode.

DETAILED CIRCUIT DESCRIPTION

TRIGGER BOARD

The Detailed Circuit Description of the trigger board covered in the Model 112 Circuit Description applies to the Model 115 as well with the exception that the Model 115 trigger board contains the phase lock amplifier. The phase lock amplifier is identical to the trigger clamp amplifier except that it is connected as an inverting operational amplifier rather than in a potentiometric configuration. The base of Q22 is the minus input. R73 is the 90° phase adjust and R81 is the 0° phase adjust. Pin 8 is connected to the trigger level/phase adjust control on the front panel in the phase lock mode. The output of the tunnel diode phase multivibrator is coupled in on pin 5 and applied through resistor R67 to the minus input of the phase lock amplifier in the phase lock mode. Phase lock capacitors are selected by the frequency hertz switch and connected between the phase lock amplifier output and pin 4, the minus input of the phase lock amplifier. Connections from the output of the phase lock amplifier to the VCG input are accomplished on the sub-panel.

POWER SUPPLY AND POWER AMPLIFIER BOARD, VCG BOARD, MAIN BOARD, and REAR PANEL BOARD Detailed Circuit Descriptions are discussed in the Model 112 Detailed Circuit Description section. These boards are interchangeable between the Model 112 and Model 115.

FIRST SUB-PANEL

The Model 115 first sub-panel contains the VCG input connector, the trigger input connector, the power amplifier output connectors, the manual trigger switch, the frequency dial potentiometer, the trigger slope switch, the trigger level control, the power amplifier function selector switch and output amplifier attenuator, the phase lock continuous trigger mode switch, and the phase lock "un-cal" indicator and its driving circuit. The triangle out, sine out, ramp out, and square wave output are available on pins 2, 21, 24, and 25 and delivered to the function selector switch. In the counter-clockwise position of the function selector switch (uppermost position in the diagram), the triangle is selected and delivered to the input of the - 1 amplifier via pin 31. The output of the -1 amplifier is always available at the rear panel; therefore, on the first position of the switch, the triangle is delivered to the -1 amplifier, amplified by a factor of -1 and made available at the rear panel. The output of the -1 amplifier is also coupled in pin 30 of the front panel and delivered back to the function selector switch. In the counter-clockwise position of the function selector switch, the output of the -1 amplifier is delivered to the output amplifier attenuator and off the center arm of the attenuator to the input of the power amplifier via pin 27. In the first position of the function selector switch, the triangle receives a double inversion and is delivered to the front panel in phase with the fixed outputs on the rear panel. In the second position from the counter-clockwise position, the triangle is delivered directly to the attenuator and to the input of the power amplifier. Note that it is also still delivered to the input

of the -1 amplifier and, therefore, in both positions marked "triangle" of the function selector, an output will be delivered to the rear panel differential connector that is 180° out of phase with the triangle on the fixed connector on the rear panel. Similar switching occurs for the sine, ramp and square wave outputs.

The output of the power amplifier is delivered to pin 29 and to the GR connectors on the front panel. The manual trigger switch simply delivers a triggering signal to the trigger board when depressed and the generator will generate 1 cycle of the selected frequency. The start-stop point of the 1 cycle generated is determined by the start-stop point potentiometer setting. The dial potentiometer attenuates the +6 volts and delivers an input to the VCG via pin 16. R16 in series with the trigger in connector sets the input impedance of the trigger in circuitry. Diodes CR2 and CR3 insure that the trigger circuit will not be damaged if an overvoltage is applied at the trigger input connector. SW2, the trigger polarity switch, switches the inputs applied to the differential trigger amplifier on the trigger board so that the user can generate a triggering signal with a positive or negative going waveform. The trigger levela djust in the triggered mode provides a reference voltage on the opposite side of the differential trigger input circuitry than that connected to the trigger input connector and allows the point, on the applied waveform that triggering occurs, to be varied. When in the phase lock mode, the trigger level control is switched to the minus input of the phase lock amplifier and provide a variable voltage for adjusting the phase difference of the output signal generated by the unit and the applied phase lock signal on the trigger in connector. SW1, the mode switch, provides the logic switching for the three modes of operation of the Model 115. The uppermost pole on SW1 shown in the circuit diagram grounds the trigger amplifier input resistor in the plus input of the trigger amplifier in the phase lock and continuous mode and connects the output of the main integrator to the resistor at the plus input of the trigger amplifier in the triggered mode. The trigger gate is available on pin 13 and applied via the second pole to a resistor in the minus input of the phase lock amplifier when in the phase lock mode. The trigger gate is disconnected by the second pole in the continuous position and delivered to CR4 and CR5 and to the trigger amplifier plus input in the trigger mode. The third pole on the switch delivers the output of the phase lock amplifier to the phase lock indicator driver and also to the fifth pole on the switch when the switch is in the phase lock mode. The fourth pole on the mode switch delivers the output of the trigger amplifier via CR5 to the minus input of the main integrator when the switch is in the triggered mode. The fifth pole of the mode switch delivers the 'output of the phase lock amplifier to the phase lock VCG input via pin 12 when in the phase lock mode. In the continuous and triggered mode this pole grounds the phase lock VCG input. The final pole in the mode switch connects the trigger level adjust to the zero degree phase adjust potentiometer and on to the minus input of the phase lock amplifier when in the phase lock mode. In the continuous and triggered mode, the trigger level adjust is connected to the trigger input comparator circuit and serves as a trigger level control.

The phase lock "un-cal" driver circuit is a go/no-go configuration. The nominal level when in perfect phase lock is zero volts applied to the phase lock indicator driver. If the output of the phase lock amplifier swings sufficiently positive to turn on Q3, the collector of Q3 moves sufficiently negative to turn on transistor Ql providing a current path for the phase lock "un-cal" light and the light is illuminated. The level required is approximately +0. 6 volts. If the output of the phase lock amplifier moves sufficiently negative to turn on Q4, the collector of Q4 moves positive turning on QZ. The collector of Q2 moves negative turning on Q1 once again, providing a current path for the phase lock "un-cal" light. The Model 115 remains in frequency lock even though the phase lock "un-cal" light might be illuminated. The light turns on to indicate that the tolerances associated with the phase adjust control are being exceeded.

SECOND SUBPANEL

The second subpanel contains the phase lock capacitors, the frequency hertz switch and its associated frequency range capacitors and resistors, the start-stop point potentiometer and the 90° phase lock "cal" switch mounted on the rear of the start-stop point potentiometer, the main frequency vernier, and the trigger gated switch. Pin 14 connects to the phase amplifier output and pin 7 to the phase amplifier minus input placing R1 from the output of the phase lock amplifier to its minus input. The rear-most wafer of the frequency hertz switch selects the phase lock capacitor for that particular frequency range. The second pole from the left of the frequency hertz switch shown in the schematic diagram selects a resistor to ground for the VCG clamps driving the main integrating resistors. As a large resistor is selected as an integrating resistor, a resistor is connected to ground to provide a constant load on the VCG clamps. The third pole from the left in the schematic diagram on the frequency hertz switch selects resistors between the integrator balance potentiometer on the main board and the plus input of the integrator. As larger integrating resistors are selected, resistors are connected in the plus input of the main integrator to balance out the voltage developed by source current in the main integrator. The fourth pole from the left on the frequency hertz switch selects the integrating capacitor for frequency ranging. Cl is located on the front panel due to its size and is connected to the frequency hertz switch via pins 1 and 2 on the second subpanel. The fifth pole on the frequency hertz switch selects the appropriate integrating resistor for frequency ranging.

The "Off X. 3 and X1" switch, SW2, allows different integrating resistors to be selected for the X. 3 and Xl range to allow overlap between the range decade. The start-stop point potentiometer selects a dc voltage to be applied through resistor R30 to pin number 6 and on to the plus input of the trigger amplifier to determine the starting and stopping point of the main integrator when in the triggered mode. The 90° phase "cal" switch opens the line between the phase adjust on the front panel and the minus input of the phase lock amplifier when switched to the "90° cal" position (counter-clockwise

rotation of the start-stop point potentiometer).

The frequency vernier attenuates a portion of the -6 volt supply and delivers it to the input of the first VCG amplifier. The frequency vernier is in a "cal" position when it is in its most clockwise rotation. This grounds the vernier input to the first VCG amplifier. When rotated to its counter-clockwise position it supplies sufficient negative voltage to the first VCG amplifier to reduce the frequency approximately one minor dial division. The trigger gated switch, SW4, grounds pin 19 in the gated position to provide for gated operation on the trigger board. R35 and R36 attenuate the 10nsec. square wave available on pin 23 and deliver it to pin 24 which returns to the trigger reset on the trigger board. The level selected by the start-stop point potentiometer is available on pin 6, and delivered to the plus input of the trigger amplifier.

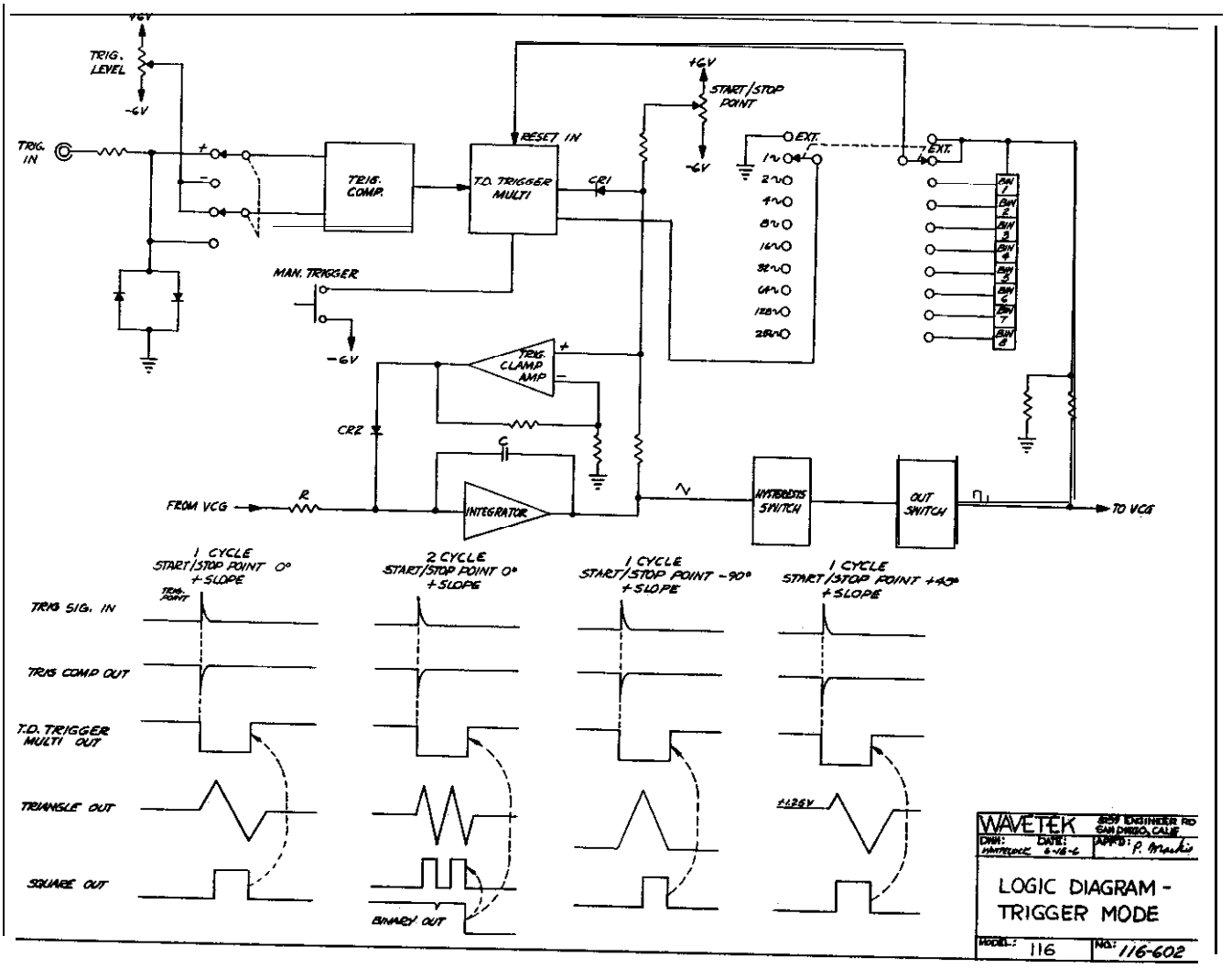
TRIG. LEVEL
+6V
-6V
TRIG. IN
TRIG. COMP.
T.D. TRIGGER MULTI
RESET IN
CR1
START/STOP POINT
EXT.
1 MΩ
2 MΩ
4 MΩ
8 MΩ
16 MΩ
32 MΩ
64 MΩ
128 MΩ
256 MΩ
MAN. TRIGGER
TRIG. CLAMP AMP
CR2
C
R
FROM VCG
INTEGRATOR
HYSTERESIS SWITCH
OUT SWITCH
TO VCG
1 CYCLE START/STOP POINT 0° +SLOPE
2 CYCLE START/STOP POINT 0° +SLOPE
1 CYCLE START/STOP POINT -90° +SLOPE
1 CYCLE START/STOP POINT +45° +SLOPE
TRIG SIG. IN
TRIG COMP OUT
T.D. TRIGGER MULTI OUT
TRIANGLE OUT
SQUARE OUT
BINARY OUT
±12.6V
WAVETEK
LOGIC DIAGRAM - TRIGGER MODE
MODEL: 116
NO: 116-602

Figure 3-5

THEORY OF OPERATION
Model 116

Refer to Model 116 block'diagram at the rear of the manual.

The Model 116 is basicly a Model 115 with an added built-in cycle counter. The Model 116 users should first review the circuit description of the Model 115 beforestudying the Model 116. All blocks in the Model 116 block diagram with the exception of those at the extreme left-hand side of the diagram, are the same as for the Model 115. The added circuitry in the Model 116 is a binary reset circuit, a power supply for the binarys used in the cycle counter, the cycle counter itself, and the switching involved. The binarys used in the cycle counter are integrated circuit J-K flip-flops and are used to count down the reset pulse applied to the trigger and phase tunnel diode multivibrator. Since the circuit description for trigger and phase lock modes of the Model 115 are the same for the Model 116, discussion of these will not be taken up in this section.

The external position of the triggered cycle switch is the same as the gated mode of operation for the Model 115. The one cycle position of the triggered cycle switch is the same as the triggered position of the Model 115. In the one cycle position, the reset pulse from the square wave output is fed directly into the trigger and phase tunnel diode multivibrator, and one cycle is generated on command by an externally applied triggering signal or by depressing the one cycle pushbutton on the front panel. In the two cycle position of the triggered cycle switch, the reset pulse from the square wave output is fed through on bistable multivitrator, an integrated J-K flip-flop, and therefore the instrument must go through two cycles of operation before the trigger multivibrator receives a reset pulse. The output of the first binary is coupled to the second binary and so forth through the eight binarys. In the four cycle position the reset pulse must pass through two binarys and, therefore, the instrument must go through four cycles of operation before a reset pulse is applied to the trigger circuit.

The use of the eight binarys to count down the reset pulse allows the Model 116 to generate 1, 2, 4, 8, 16, 32, 64, 128, and 256 discrete cycles for tone burst operation simply by selecting the number of cyles desired with the triggered cycle switch. The generator can be triggered either with an external triggering signal or by depressing the manual trigger button.

DETAILED CIRCUIT DESCRIPTION

Refer to the Model 116 Second Sub-Panel schematic at the rear of the manual.

The detailed circuit description as covered for the Model 115 applies to the Model 116 as well. The added circuitry on the second sub-panel to provide the

cycle counter will be discussed here. Detailed circuit description for the remainder of the Model 116 can be found in the section on detailed circuit description of the Model 115.

Q3 on the second sub-panel of the Model 116 serves as the pass transistor for an approximately 3.6 volt supply for the integrated flip-flop. The +6 volts is attenuated by R42 and R44 and applied to the base of Q3. The emitter of Q3 serves as the supply point for the binarys. Q4 is added to remove the supply voltage from the binarys in the external position of the triggered cycle switch. The base of Q4 is grounded in all positions of the triggered cycle switch by the second wafer and Q4 is non-conducting. In the external position of the triggered cycle switch, the ground at the base of Q4 is removed and Q4 comes into conduction grounding the base of Q3. This is added as a convenience for battery version users so that when not using the triggered or triggered cycle mode, the triggered cycle switch can be turned to the external position and conserve battery current since the binarys will be inoperative.

Transistors Ql and Q2 and their associated circuitry adjust the phase and levels of the binary reset pulse to be compatible with the positive logic of the integrated binarys. The output of the tunnel diode trigger multivibrator on the trigger board adds levels of zero and -6 volts. These levels are available at pin 25 and applied to the base of Q2. In the zero state of the tunnel diode trigger multivibrator, the binarys are reset and inhibited. When the trigger gate goes to -6 volts, the binarys are enabled. When the input level at pin 25 is zero volts, the output at the collector of Ql is approximately t3. 6 volts applied to pin 7 of all of the binarys. This sets the quiescent state and inhibits the binarys. When the trigger gate steps to -6 volts, the level of the collector of Q1 moves to approximately zero volts and the binarys are enabled. Transistors Q5 and Q6 and their associated circuitry convert the positive logic output levels from the binarys back to the zero and -6 volt logic levels compatible with the Model 116. When a selected positive level from one of the binarys is supplied to the base of Q5, Q5 is turned on turning on Q6 and clamping the output delivered to pin 24 at ground. A zero level output in the selected binary has Q5 off, Q6 off and the output level delivered to pin 24 is -6 volts.

Section A of the triggered cycle switch selects the attenuated square wave in the external and one cycle position to be delivered to the trigger reset circuitry via pin 24. In the two cycle position it selects the output of the first binary to deliver the reset pulse, and so on. Section B of the triggered cycle switch grounds pin 19 in the external position and sets up the triggered circuitry on the trigger board in the gated mode, as was discussed with the Models 112 and 115. In the one cycle through 256 cycle positions, section B grounds the base of Q4 and divides the supply voltage for the integrated circuit flip-flops. When using a battery version of the Model 116 and not using the triggered cycle mode, it is desirable to place the triggered cycle switch in the external position to conserve battery current. When operating the Model 116 in the phase lock mode, the triggered cycle switch should be in the one cycle position.

The binarys are eight identical integrated circuits (J-K flip-flops). Pin 1 is the input point, pin 8 is the supply voltage, pin 7 is the pre-set or inhibit input, pin 6 is the output pin, pins 2 and 5 are connected together to set up the proper logic sequence, pins 3 and 4 are connected to ground.