

# Building a test setup with a single motherboard in the large vacuum chamber in the HiRA lab

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- 1) Attach the motherboard tower to one of the stands.
  - We generally use the stands from the 50-cm setup.
  - Orient the motherboard tower so the water connections are below the rest of the electronics, to prevent damage if there is a leak.
  - Attach the tower as far down the stand as possible, to allow the most space for the cables that attach to the top. The cables are delicate, and if there isn't enough space between the top of the tower and the top of the stand the cables are bent beyond what is safe.
- 2) Secure the stand to the platform in the vacuum chamber.
  - The tower and electronics must be electrically isolated from the chamber to reduce electronic noise. Plexiglas or other insulating materials can sometimes be found in the machine shop general stock area or in the back of the stockroom and placed between the stand and the platform in the chamber. This also lifts the tower up so that the water connections don't touch the platform.
  - When sitting on an insulator, the tower usually needs to be secured with clamps since the screw holes are covered. Insulate the clamp from the tower as well.
- 3) Use an ohm-meter to check the isolation repeatedly while completing setup.
  - Isolation should be perfect or close to it.
- 4) Isolate the flanges on the vacuum chamber from the chamber itself.
  - Flanges on the chamber will be grounded to the electronics, so they need to be connected through plastic o-ring supports and clamped on using nylon bolts.
  - The nylon bolts tend to bend when tightened, rather than making the connection more secure. If necessary, attach and tighten the flange using metal bolts, then attach the clamps that use nylon bolts, and remove the metal ones.
- 5) Connect the water cables.
  - Metal hoses and VCO connectors are used inside the chamber, since they are vacuum-tight. Make sure these are wrapped in insulation, since they can ground the tower to the chamber.
  - Outside the chamber, Prestolok brass fittings and plastic tubing (often Parker Parflex) are generally used. These fittings are not as secure, so don't put any stress on them. Note: the plastic Prestolok Y-shaped unions are particularly sensitive to this; I would avoid them. To ensure a good fit, the plastic tubing must be cut cleanly and perpendicular to the tube, and inserted firmly.
  - Fill the chiller with low-conductivity water (LCW) up to the maximum fill line. LCW is used so that the water doesn't electrically connect the tower to the chiller. Keep a little extra on hand the first time the chiller is turned on, to account for water filling the tubing.
  - Visually check the valves on the chiller to make sure the water is allowed to flow into the vacuum chamber.

- 6) Turn the chiller on to test for leaks and to make sure the cold water circulates through the tower.
  - The appropriate temperature setting depends on how much heat is being generated, i.e. the number of towers and chipboards. I suggest starting with 16-18°C and decreasing if necessary. Never set the temperature under the dew point, or condensation will form and can drip onto the electronics.
  - The water connections should become cool to the touch within a few minutes. If they don't, check the valves on the chiller again.
  - Turn the chiller off while connecting electronics.
- 7) Set up the electronics modules in the rack.
  - In the VME crate, you need an XLM, an SIS 3300 FADC, CAEN V262 input/output module and SBS PC-VME interface.
  - In one NIM bin, you will need a splitter (e.g. NSCL splitter/attenuator module, configured to split the 34-pin cable into lemo connections with no attenuation), an ECL-NIM-ECL converter, and a trigger latch (e.g. LeCroy dual gate generator model 202).
  - In a second NIM bin, you will need a +12V lemo output, a digital voltmeter capable of accepting several lemo inputs and displaying at least to 1V, a pulser, and a 5V adjustable power supply (currently we use SPARKY instead).
    - The digital voltmeter is to read thermocouple temperatures.
    - The 5V power supply we generally use is "SPARKY", which is a separate device located in the permanent experimental setup, rather than in the NIM bin.
  - A second voltmeter is required to monitor the motherboard regulator voltage. This can usually be a regular voltmeter that does not sit in any bin or crate, but should be put in an easily visible location (e.g. attached to the rack with Velcro.)
  - All rack crates are connected to clean ground power.
  - The spdaq computer is connected to dirty power. It should be isolated from the rack, although when plugged in it will show little resistance to the crates because of the grounding. The spdaq is connected to the SBS module in the VME crate with optical cable, which is done to preserve its isolation from the electronics.
- 8) Connect electronic cables between tower and flange(s), and then from flange(s) to rack (see Figure 1.)
  - Use cables intended to be used inside a vacuum chamber. These will often be shielded from electronic noise using a metallic foil and insulated with a nylon sleeving. They will also generally be taped using Capton tape, the adhesive on which does not evaporate under vacuum as much as other tape. I recommend using the grey 34-pin GORE cable for inspect channels and thermocouple output.
  - The thermocouple output is a 34-pin cable, but in the digital voltmeter accepts lemo connections. There are connectors in the HiRA lab to go from 34-pin to lemo. Pin assignments on this cable are listed in Table 1. Connect the regulator voltage signal to the second voltmeter and the thermocouple temperatures to the first.
  - Make sure the thermocouple box is also isolated from the chamber.
  - Ground the cables to the tower, flange, or rack, usually with alligator clips.
- 9) Wire up the modules in the rack (see Figure 2.)

- The XLM ECL connection is configured so that the first 8 signals are inputs to the XLM and the second 8 are outputs. Since the ECL-NIM-ECL converters require inputs and outputs on separate connectors, the cable needs to be split in two so that the first 8 signals are output from the ECL-NIM-ECL module, and the second 8 are input to it.
- Pin assignments on the inspect channels and XLM ECL connection are listed in Table 2 and 3.
- A detailed explanation for the wiring follows in the next section.

## Introduction to HiRA acquisition logic / explanation of wiring

- 1) A detector or pulser sends an analog signal into one or more channels on one or more chipboards in the motherboard tower.
- 2) The signal enters a pseudo-constant fraction discriminator (CFD) consisting of a leading-edge discriminator and a zero-crossing discriminator. The leading edge is used to enable the zero-crossing discriminator if the signal is above the predefined threshold. The zero-crossing discriminator then generates a time signal based on the zero crossing of the bipolar analog signal. If the signal passes through the CFD, then energy, timing, and location (which channel on which chipboard fired) is sent to the motherboard buffer.
- 3) The CFD time signals from different chipboards are sent to a logical OR, which provides a single logic signal, the “OR A” on inspect channel 3. It indicates if any channels fired, and is used to trigger the XLM (XLM input 1).
- 4) Once triggered, the XLM starts the data acquisition cycle, to acquire data from the MB. Following the external trigger XLM disables the discriminators on the chips to prevent any retriggering and sends a request for data to the motherboard. Each time the motherboard receives a request, it acknowledges it and sends out data from one channel. Address (i.e. which channel on which chip has fired) information is sent directly to the XLM, and time and energy information are sent to the FADC on separate double lemo cables. After a preset delay the XLM issues a clock signal to the FADC (XLM output 9 to FADC input 1). Upon receiving the clock signal, the FADC digitizes the time and energy information and stores it to its internal buffer.
- 5) After all the channels are read out of the motherboard, the request for data is not acknowledged by the motherboard, and the XLM sends out a logical “complete” signal (output 12), which is used to trigger the computer acquisition.
- 6) The “complete” signal goes into the start of the trigger latch. The latch generates a signal on its NIM output, which is used as the computer trigger (V262 input 0). This signal persists for as long the computer needs to react to it and send an acquisition acknowledge (V262 Shp out 2) to the latch stop.

*Note: since the XLM disables the chip discriminators upon receiving the OR signal, no additional busy latch is needed to prevent computer retriggering.*

- 7) The computer reads from the XLM and FADC buffers and stores the events to file. When it is finished, it sends out a module clear on Shp out 1, which is intended to be sent to other modules to tell them to clear their buffers. Finally it pulses a “computer going ready” signal on Shp out 3, which means that the computer is ready to accept more data. We use this pulse to clear the discriminator veto, which is XLM input 3, to allow the discriminators to accept further events.
- 8) More detailed information is available in the HiRA paper, available at <http://groups.nsl.msui.edu/hira/Publications%20and%20Theses/Hira.pdf>, or at <http://www.nsl.msui.edu/~famiano/>, specifically for VME trigger information: <http://docs.nsl.msui.edu/daq/ProductionReadout/Manual/>

When turning on the setup:

- 1) The first time you turn on the setup, leave the side of the tower open so you can see the red LED on the motherboard.
- 2) Turn on the chiller.
- 3) Turn on NIM bins including 12V power supply. Make sure that you can properly read the thermocouple temperatures. Do not turn on the 5V power supply yet!
  - $10 \text{ mV} = 1^\circ\text{C}$
- 4) Turn on the VME crate
  - check that the voltage across the regulator is between 0.6-0.8 V.
- 5) Turn on the 5V power supply
  - The red LED on the motherboard should briefly turn on and then off again. If it does not turn off, too much current is being drawn from the supply, which can damage the electronics. Turn the power off immediately.
  - Check that the voltage across the regulator is 5V.
  - When turned on, the regulator will get hot. You should keep an eye on this temperature whenever the tower is on. When the tower is full of chipboards, it may reach  $40^\circ\text{C}$ . If it approaches  $50^\circ\text{C}$ , turn off the power supply and test the 5V power supply and thermocouples. A high temperature usually indicates that the regulator is working too hard, that is, it is receiving a voltage from the power supply that is higher or lower than what is ideal. You can adjust the positive voltage on the 5V power supply to provide a more appropriate voltage and minimize the regulator temperature. Since it is necessary to correct for the voltage drop across the power cable, the voltage supplied by the power supply is generally set higher than the 5V required by the MB. Usually around 6-6.5V.
- 6) Shut down in reverse order: first the 5V power supply, then the VME crate, NIM bins, and finally the chiller.

Notes on computer readout

- 1) All the software for controlling HiRA readout is located in the hiratest account.
- 2) The two main programs used for the test setup are MB control and Readout, which are both run on the spdaq computer.
  - In order for the system to find the correct files for each program, the BASH environmental variables BITFILEPATH, CURRENT, DAQHOST, and READOUTINPUTPATH must be set to the location of the XLM bitfiles, the location of the Current directory, the name of the daq computer that the system is connected to, and the location of config.dat and other Readout input files, respectively.
  - The file READOUTINPUTPATH/config.dat needs to be modified to specify the number of XLM's and FADC's that are being used, as well as the location of the XLM (crate and slot) and the base address of the FADC. The base address is set by the jumpers on the side of the FADC. Note that these specify a number in hexadecimal while Readout expects input in normal base ten, so if the jumpers are set to 33, set the base address to 51. This file is used as input for both Readout and the MB control program.

- 3) The motherboard and XLM are controlled with the script `silstrip.tcl`, which utilizes functions defined in `chip_cont.cpp`. The MB control is currently located in the `hiratest` account at `Current8.1DAQ/ASIC_control_new/CHIP_H`.
  - First, the XLM is configured using a bit file. Bit files are stored in `ASIC_control_new/bitfiles/`, which should be set as the BASH environmental variable `BITFILEPATH`. If `config.dat` has the correct XLM location, type, and bit file defined, then the bit file is loaded by selecting “Default XLM config” from the File menu. Otherwise, select “XLM config” and manually select the slot, crate and type of the XLM, and bit file on the panel that appears on the right. Use the file “`hira_f_um2.bit`” for an XLM80 and “`xxv_dm_u.bit`” for an XLMXXV.
  - While the XLM is being configured, the indicator LED’s on the top of the XLM will flash a few times in a specific pattern. If all the LED’s remain on when the bit file is done loading, it indicates that the configuration was not successful. Otherwise, the lights left on depend on which bit file was loaded.
  - The motherboard is configured with the actual setup file, which needs to be updated with the current number, location, and settings of the chipboards. The default file will be loaded from `ASIC_IN.setup`, which is in the same directory as the program. Older saved files are in the “`setupfiles`” directory.
- 4) Readout is controlled, not surprisingly, by the program `Readout`, which is currently located in `Current8.1DAQ/Readout` and started with the command `./godaq`.

Figure 1: Tower-to-rack wiring diagram (flange omitted for clarity)

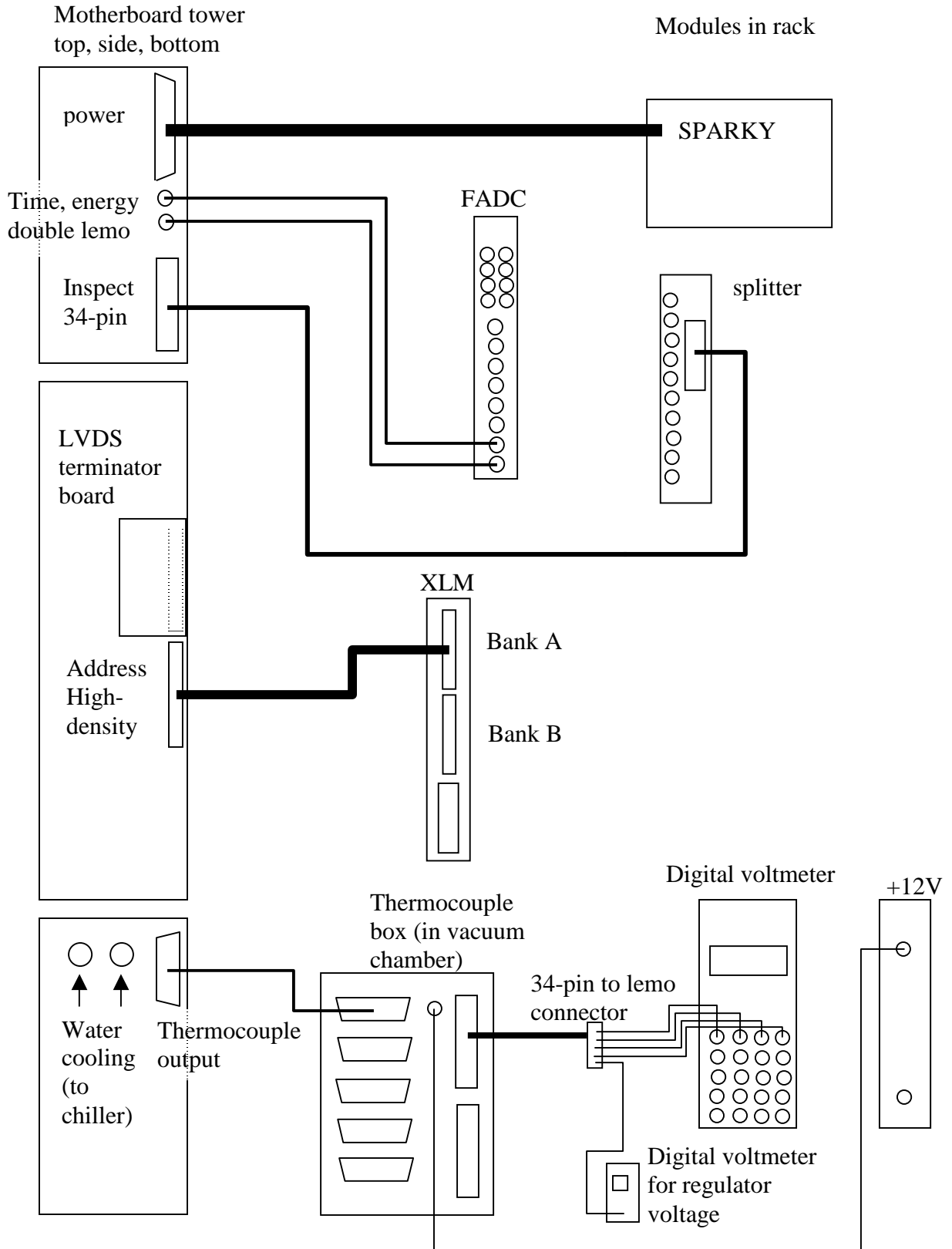


Figure 2: Rack electronics diagram

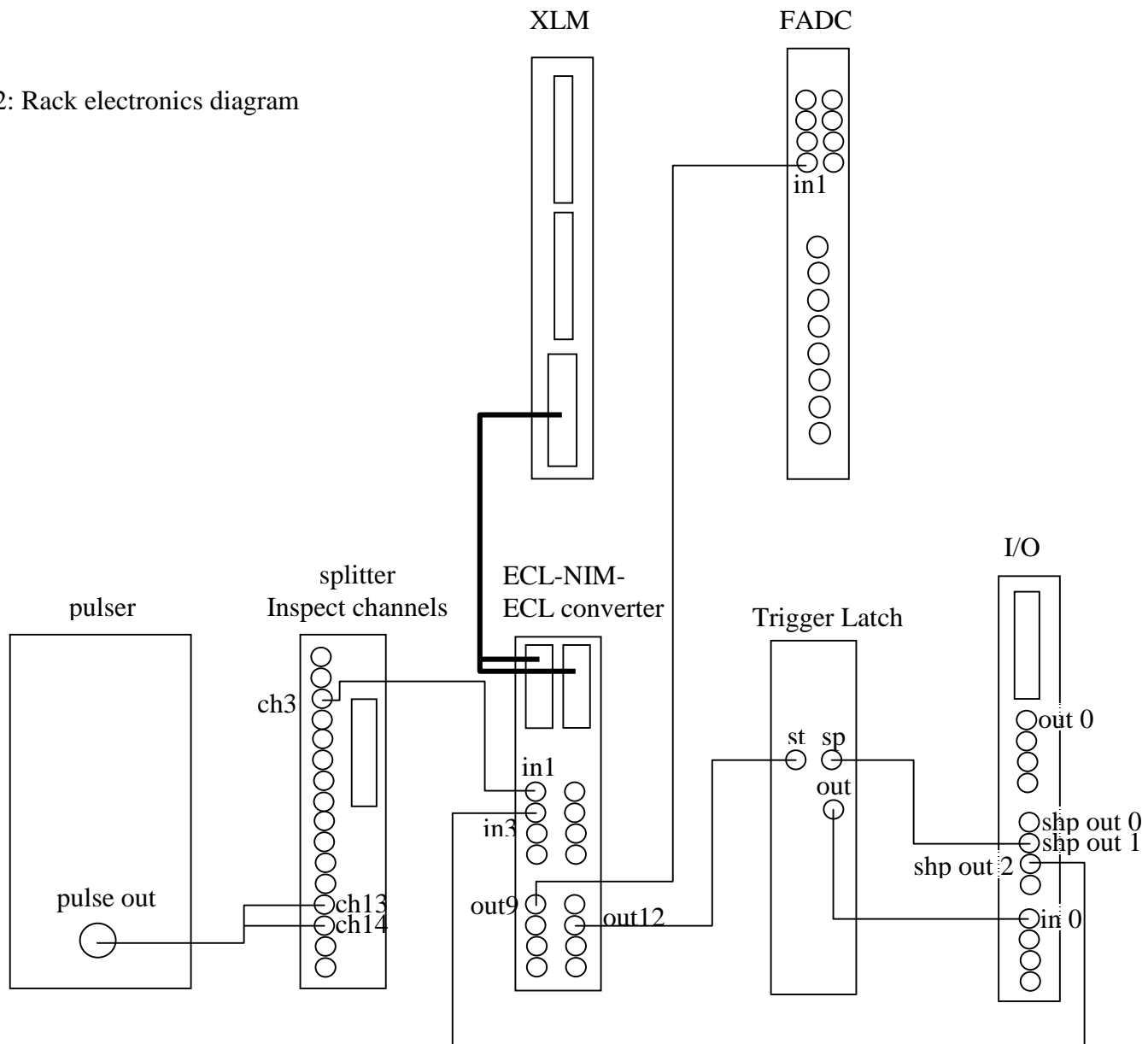




Table 1: thermocouple box outputs on 34 pin connector

Cable	pin	output
1	1	Tower 0 regulator voltage
1	3	Tower 0 regulator temp; thermocouple 0
1	5	Tower 0 thermocouple 2
1	7	Tower 0 thermocouple 1
1	9	Tower 0 thermocouple 3
1	11	Tower 1 regulator voltage
1	13	Tower 1 regulator temp; thermocouple 0
1	15	Tower 1 thermocouple 1
1	17	Tower 1 thermocouple 2
1	19	Tower 1 thermocouple 3
1	21	Tower 2 regulator voltage
1	23	Tower 2 regulator temp; thermocouple 0
1	25	Tower 2 thermocouple 1
1	27	Tower 2 thermocouple 2
1	29	Tower 2 thermocouple 3
1	31	Tower 3 regulator voltage
2	1	
2	3	Tower 3 regulator temp; thermocouple 0
2	5	Tower 3 thermocouple 1
2	7	Tower 3 thermocouple 2
2	9	Tower 3 thermocouple 3

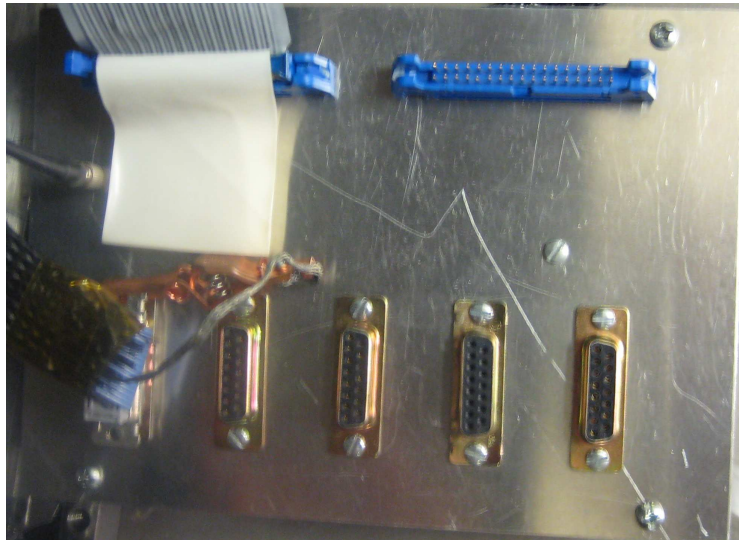


Table 2: XLM ECL channels

Channel	Designation
1	input: trigger for bank A
2	input: trigger for bank B
3	input: clear veto
4	input: fast clear
5	input: veto patch
9	output: SIS clock for motherboard attached to bank A
10	output: SIS clock for motherboard attached to bank B
11	output: Global enable
12	output: complete



Table 3: Inspect channels

Channel	Designation
1	Common stop
2	CFD test
3	OR A
4	OR B
5	OR C
6	CSA test
7	Shaper test
8	SUM A
9	SUM B
10	SUM C
11	pulse 1 odd channels
12	pulse 1 even
13	pulse 2 odd (Ef, pos)
14	pulse 2 even
15	pulse 3 odd (Eb, neg)
16	pulse 3 even



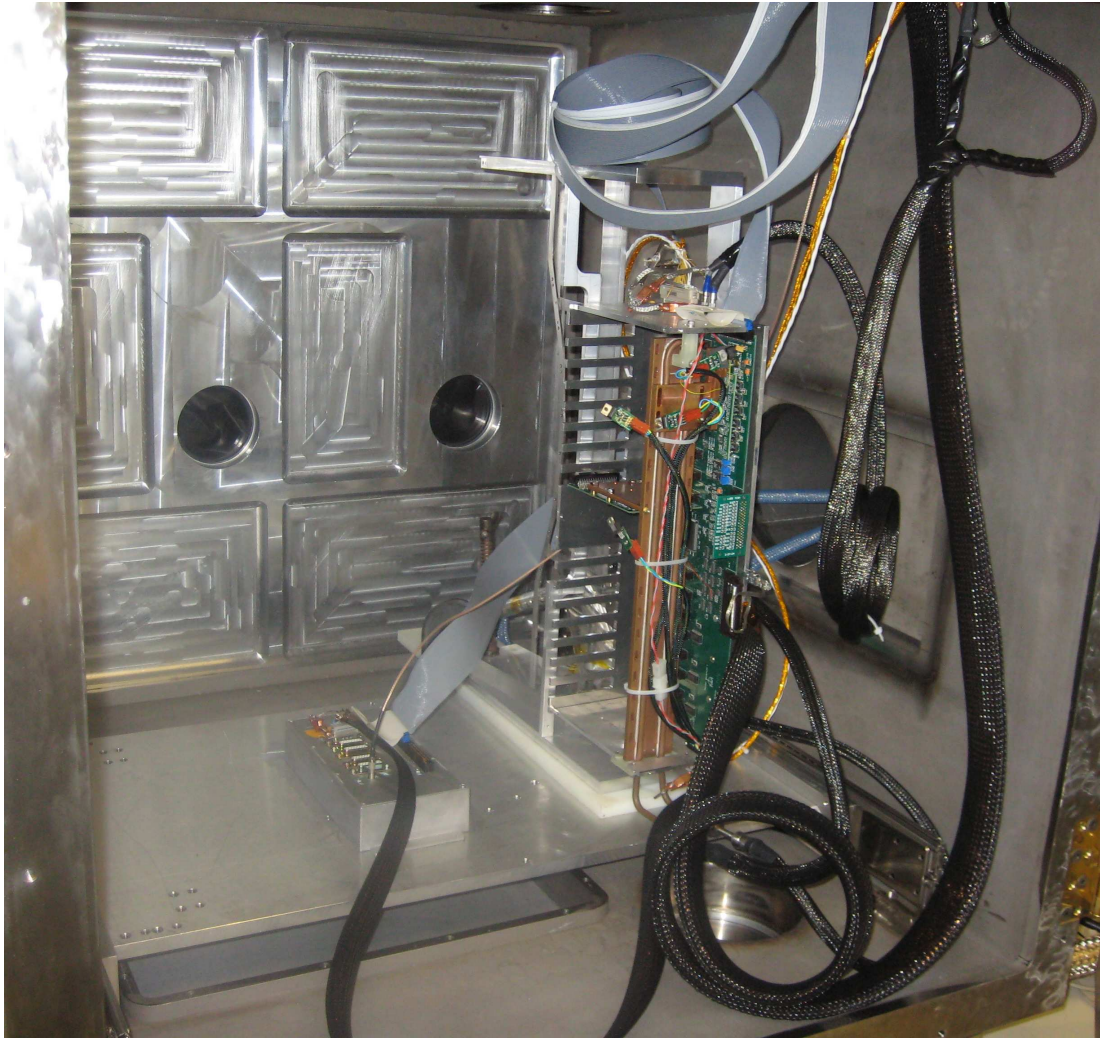


Figure 3: One tower and thermocouple box inside large vacuum chamber

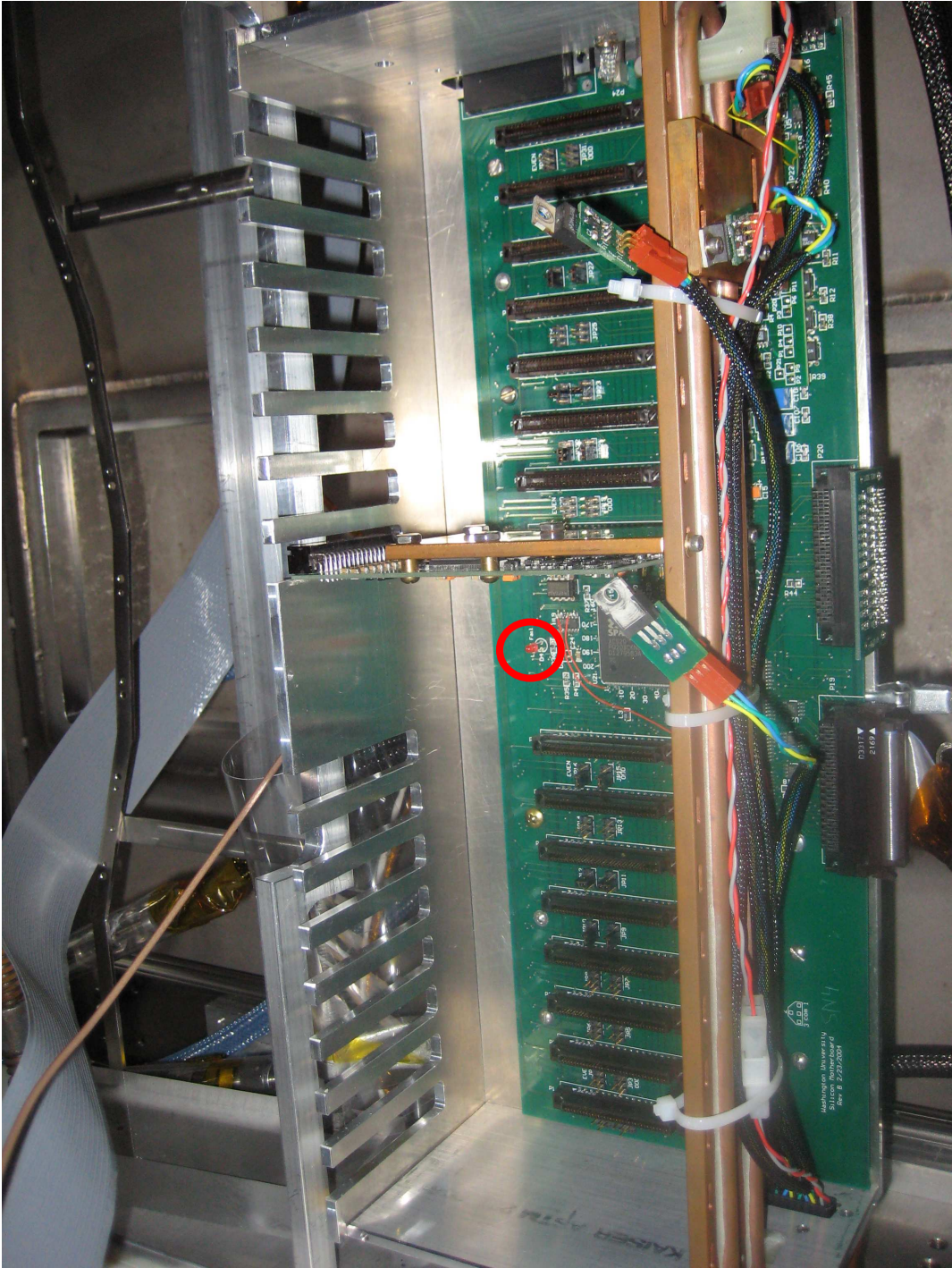


Figure 4: Close-up of HiRA motherboard tower with one chipboard in slot 9. Sides are removed to view the indicator LED (circled) on startup.

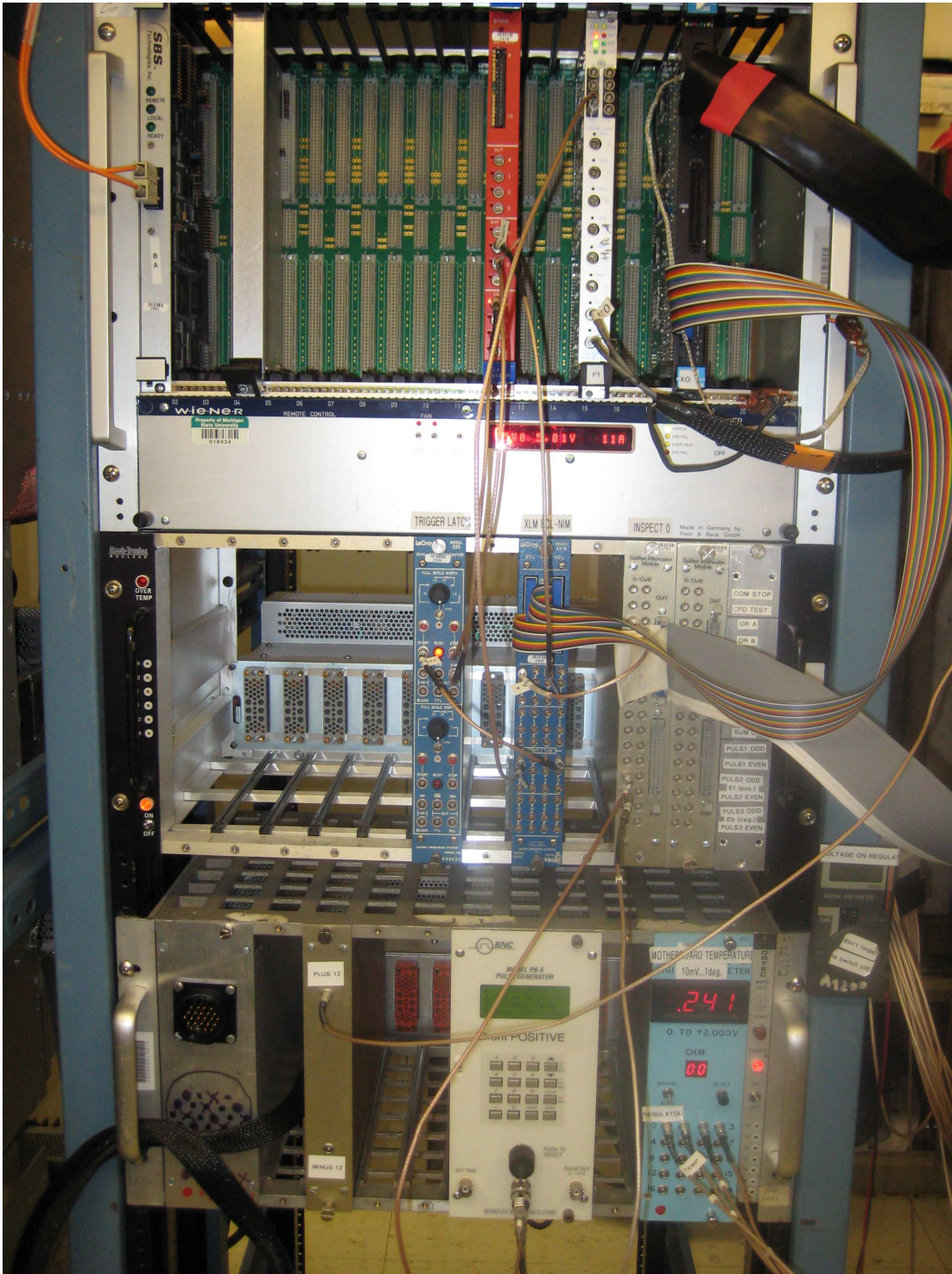


Figure 5: Test setup electronics in the rack. SPARKY power supply not shown.