Design of timing monitoring circuits for time projection chamber readout

K.Urano,[*1] A.Taketani, and H.Baba

A time projection chamber (TPC) will be built for experiments to study equation of state (EOS) of nuclear matter. In order to measure the symmetry-energy term of the EOS, it is necessary to identify the particle species and to measure their momentum vectors simultaneously in the final state of heavy ion collisions over a large phase space.[1] The TPC will be a major detector for experiments and be installed in the SAMURAI magnet. A particle passing through the TPC ionizes gas, and the ions and electrons drift along the applied electric field. Electrons reach the read-out pads and generate electronic signals. The drift time is proportional to the distance between the particle trajectory and the read-out pad. The read-out pad is 8 mm × 12 mm. There are 12000 pads. In addition to the particle trajectory, the deposited energy determines the particle charge. In order to measure the drift time and pulse height, the TPC readout is equipped with the flash ADCs.

The general electronics for the TPC (GET) is currently developed[2] by a collaboration among French, US, and Japanese institutions. The GET includes front-end preamplifiers, analog pipeline buffers, flash ADCs, trigger logic, a digital readout, timing synchronization, and data acquisition. The major specifications of the GET are as follows:

(1) Up to 100 MHz sampling clock.
(2) 12-bit accuracy of AD conversion.
(3) Up to 10 KHz trigger handling without major dead time.
(4) Up to 30,000 channel readout.

In the GET system, 128 channels of preamplifiers, pipeline buffers, and flash ADCs are packed into one printed circuit board (AsAd). Each AsAd board receives the timing signal from a master timing module. Up to 128 AsAd boards form a single GET system, and they are synchronized accurately to run with 100 MHz sampling. A timing monitoring system (SPYBOX) plays an important role for this purpose. The requirements of the SPYBOX are

(1) 128 input channels with differential LVDS from fire wire connectors.[3]
(2) Comparison of the timing between inputs.
(3) A timing resolution of measurement 1 ns.

Figure 1 shows the configuration of the SPYBOX. When the fire wire communication protocol is not employed, each AsAd board sends its reference timing signal to the SPYBOX through fire wires. Each timing signal is received by the LVDS receiver with proper termination in order to isolate the AsAd circuits from multiplexer circuits in the SPYBOX. The LVDS signals are fed into the multiplexers, and two signals are selected and transferred to a time-to-digital converter (TDC) that measures the time difference between two signals. A CPU module controls the multiplexers and reads the data from the TDC. The CPU module also communicates with the rest of the GET system.

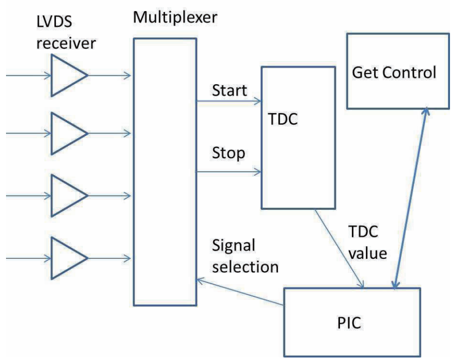

Fig. 1. Block diagram of the SPYBOX

As the LVDS receiver, the ADN4668 from Analog Devices with 200 MHz speed and 100 ps skew time was chosen. The ACAM TDC-GP21 chip with 22 ps resolution, which has 4-wire SPI interface, was selected. The CPU module PIC18F4550 from Microchip was used; it contain a USB interface, digital inputs/outputs, and an SPI interface within a single chip. 74HC251 chips were used for the multiplexers.

When design of the logic diagram and board layout were completed, we realized that the propagation time of 74HC251 is 20 ns. It was too slow for the 100 MHz sampling speed. Therefore, we decided to build a board with 16 channel input boards with slow multiplexers, which was found to be useful for exercising multiplexer control, TDC readout, and communication with the GET systems.

FPGA, which has over 100 I/O pins and programmable logic, is a good candidate of a high speed multiplexer. However, the using FPGA would require careful design to minimize the time timing differences among channels or to calibrate them with respect to the a known timing source.

References

1) T. Isobe et al. in this APR.
2) http://www-actar-get.cea.fr
3) http://www.1394ta.org

*1 Rikkyo University