Development of timing monitoring system for time projection chamber readout

K.Urano, A.Taketani, H.Baba, T.Murakami,[*1] T.Isobe, and K.Kurita[*2]

Construction of a large time projection chamber (TPC) is planned for experiments in order to study the equation of state (EOS) of nuclear matter. In order to determine the symmetry energy term of the EOS,[1] it is necessary to measure multi particles and their momentum vectors simultaneously in the final state of heavy ion collisions over a large phase space.[2] The TPC is a major part of the detector that is installed in the SAMURAI magnet gap.

The general electronics for the TPC (GET) is currently being developed[3] by a collaboration among French, American, and Japanese institutions. The GET includes front-end preamplifiers, analog pipeline buffers, flash ADCs, trigger logics, a digital readout, a timing synchronization system, and a data acquisition system. In the GET system, 256 channels of preamplifiers, pipeline buffers, and flash ADCs are packed into one printed circuit board called AsAd. The timing signal sent from a master timing module tends to fluctuate on each AsAd board upon FPGA reprogramming. Up to 128 AsAd boards form a single GET system and they must be synchronized accurately to run with an approximately 100-MHz sampling clock. A timing monitoring system, called SPYBOX, plays an important role for this purpose. The SPYBOX is required to have:

(1) 128 input channels with LVDS signals from FireWire connectors.[4]
(2) Capability to compare the timing difference between any two inputs.
(3) A timing resolution of less than 1 ns (FWHM).

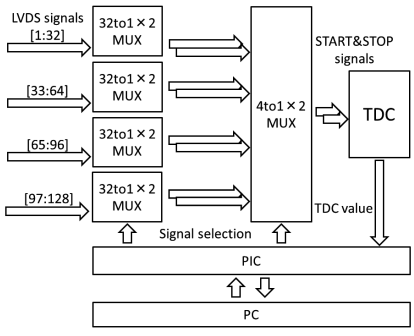

Fig. 1. Block diagram of the SPYBOX

Figure 1 shows the configuration of the SPYBOX. When the FireWire communication protocol is not employed, each AsAd board sends its reference timing signal to the SPYBOX through FireWire connections. Each timing signal is received by the LVDS receiver with a proper termination in order to isolate the AsAd circuits from the multiplexer circuits in the SPYBOX. The LVDS signals are fed into the multiplexers, and two signals are selected and transferred to a time-to-digital converter (TDC) that measures the time difference between the two signals. A CPU module controls the multiplexers and reads the data from the TDC. The CPU module also communicates with the rest of the PC.

We used Spartan3AN FPGAs as multiplexers and a converter. It supports 50 LVDS inputs. Four FPGAs were programmed to work as 32-to-1 × 2 MUX, and 2 signals were selected in each FPGA. Thus, total of 8 LVDS signals were chosen. They were fed to another FPGA and were further selected to be the start and the stop signals for the TPC. The last FPGA also worked as a LVTTL level adapter. The start and stop signals were fed to the ACAM TDC-GP21 through a coaxial cable. It had a timing resolution of 22 ps. For the CPU module, PIC18F4550 from Microchip Technology Inc. was used.

We checked the time differences among channels using the SPYBOX. The timing differences ranged over 1.5 ns before adjustments. Therefore we used buffer delays and look-up tables inside the FPGA chips to minimize the difference. Figure 2 shows the time difference among the signals after adjustments. The standard deviation was less than 0.12 ns. It found we can keep monitoring AsAd boards synchoronization upon FPGA reprogramming with a 100-MHz clock.

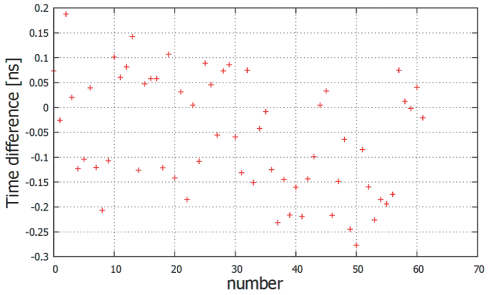

Fig. 2. Time difference of the signals passing through the FPGA

*1 Department of Physics, Kyoto University
*2 Department of Physics, Rikkyo University

References
1) L. W. Chen et al.: Phys. Rev. Lett. 94, 032701 (2005).
2) T. Isobe. RIKEN Accel. Prog.Rep. 45, 132 (2012).
3) http://www-actar-get.cea.fr
4) http://www.1394ta.org