- **ASIC x 16**

**Diagram:***

- **Shaper**
- **Hit Register**
- **TVC**
- **Peak Find And Hold**

- **H**
- **L**
- **Disc**
- **External Stop**
- **Diff-Amp**

- **ΔV ∝ E**
- **ΔV ∝ T**

- **Red Dot**

- **Inspection Points**

**Notes:**

- 2 different gain internal Charge Sensitive Amplifiers (CSA)
  - 100 MeV & 500 MeV dynamic range
  - Bypass internal CSA for use with higher gain external CSA
  - Pseudo CFD - Leading edge trigger zero cross discriminator
    - Computer controlled threshold for each strip
    - Positive and negative signals
    - On off for each channel

- TVC 150 ns & 1 μs
- Unity gain Shaper with 1 μs shaping time for both positive and negative signals
- 3 computer controlled Inspection points, shown with red dot
- Multiplexed output of E & T signals through differential Amp into LVDS flash ADC.
- Sparse readout based on hit register, or forced readout of all channels
- Pulser inputs, even or odd channels