INSTRUCTION MANUAL
453
CONSTANT FRACTION TIMING DISCRIMINATOR

Serial No. _____

Purchaser _____

Date Issued _____

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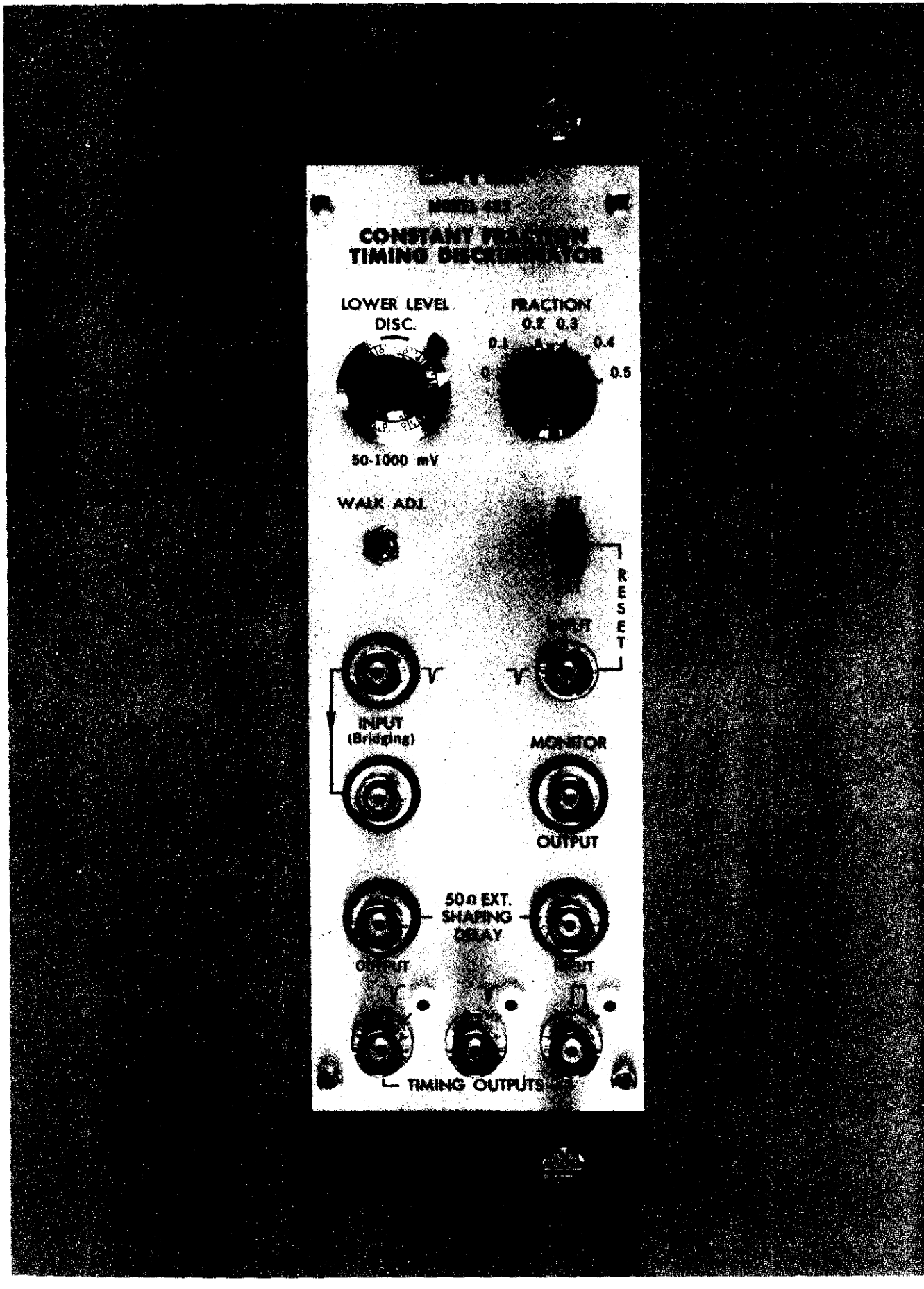

CONSTANT FRACTION
TIMING DISCRIMINATOR
LOWER LEVEL
DISC.
50-1000 mV
FRACTION
0.2 0.3
0.4
0.5
WALK ADJ.
RESET
INPUT
(Bridging)
MONITOR
OUTPUT
50Ω EXT.
SHAPING
DELAY
TIMING OUTPUTS

ORTEC 453 CONSTANT FRACTION TIMING DISCRIMINATOR

1. DESCRIPTION

The 453 Constant Fraction Timing Discriminator contains a "Constant Fraction of Pulse Height Trigger" (CFPHT)[1,2,3] for high resolution time spectroscopy. The CFPHT time pickoff is enabled by a precision lower level discriminator, variable over a range of 50mV to 1000mV. The entire circuit is dc-coupled, rendering it free from count rate dependence.

A bridging input with selectable triggering fraction and shaping delay make the 453 suitable for a wide variety of timing applications. The fast linear output from a detector system can be furnished to the 453 for time pickoff, and bridged to other modules for linear applications.

With fast scintillation detectors and a narrow dynamic range this unit provides time resolution equal to or better than leading edge timing.[3] For wide dynamic ranges the time resolution is vastly superior to leading edge timing.[1,2,3] The walk over the full 20:1 dynamic range is typically within ±120 psec.

The 453 provides excellent wide dynamic range time resolution with Ge(Li) detectors when used with the ORTEC 454 Timing Filter Amplifier.[4,5] The constant fraction timing technique has also been shown to provide improved time resolution with Si surface barrier detectors.[6]

In addition to the constant fraction timing mode, the 453 may be operated as a fast zero-crossing discriminator or a leading edge discriminator.

2. SPECIFICATIONS

INPUT (Bridging):

The bridging input permits reuse of the input signal. *Terminate the bottom connector in 50 ohms* with either a 50 ohm terminator or a terminated 50 ohm cable.

Connectors: 2 BNC connectors bridged (shorted) together; front panel

Common Input Impedance: >900 ohms (for input ≤±100 volts), dc-coupled

Polarity: Negative

Amplitude: -50mV to -1000mV; protected to ±20V dc, and ±100V at a 10% duty factor

Rise Time: $t_r \geq 2$ nsec

Reflections: Typically <20% for input rise time ≥2 nsec up to ±100V (with input terminated in 50 ohms)

LOWER LEVEL DISCRIMINATOR:

Function: Enables the CFPHT time pickoff. The lower level must be exceeded by the input to produce a timing output.

Control: 10-turn, precision locking potentiometer

Range: -50mV to -1000mV (direct reading)

Temperature Drift: ≤1mV/°C, 0 to 50°C; maximum shift ≤30mV, 0 to 50°C

Linearity: Integral nonlinearity ≤±0.3%

FRACTION:

Control: A 6 position front panel switch selects the triggering fraction *f*

Positions: *f* = 0, 0.1, 0.2, 0.3, 0.4, 0.5 (*f* = 0 with the walk adjust set full counter-clockwise provides leading edge timing from the lower level discriminator)

50Ω EXT. SHAPING DELAY (INPUT/OUTPUT):

Function: Front panel input and output provide for external selection of the 50 ohm CFPHT shaping delay

Connectors: Front panel, BNC

Input/Output Impedances: 50 ohms, dc-coupled. Terminate in 50 ohms when not used.

Internal Delay: ≈1.3 nsec

MONITOR OUTPUT:

Function: Front panel output for monitoring the CFPHT zero-crossing pulse shape, and for adjusting the walk

Connector: BNC, front panel

Output Impedance: 50 ohms, dc-coupled

Gain: ≈0.075 into a 50 ohm load (referred to the bridging input)

WALK ADJUST:

Control: A 20-turn, front panel potentiometer (screwdriver adjust) adjusts the CFPHT zero-crossing threshold for minimum walk

WALK AND DYNAMIC RANGE:

a. CFPHT Mode: Walk typically ≤±120 psec for an input pulse height range from -50mV to -1000mV with $f \geq 0.2$ (using pulses from a Naton 136 scintillator mounted on an XP 1021 photomultiplier). Walk approximately proportional to signal rise time for slower rise times.

b. Leading Edge Mode: Time shift versus amplitude ≈1.6 nsec from 2X threshold to 10X threshold (50mV threshold, $t_r \leq 2$ nsec).

INT/EXT RESET SWITCH:

A two position slide switch (front panel) selects either the internal or external reset mode.

a. Internal Reset (INT): The system is reset when the input pulse falls approximately 25mV below the lower level discriminator setting.

   Pulse pair resolution ≈25 nsec plus input pulse width above lower level (includes 25mV reset hysteresis).

b. External Reset (EXT): The system is reset by a pulse provided at the External Reset Input. System reset can be delayed up to 30μsec where desirable (system resets automatically at ≈40μsec).

EXTERNAL RESET INPUT:

Connector: Front panel BNC

Impedance: 50 ohms, dc-coupled

Polarity: Negative

Pulse Width: ⩾5 nsec

Pulse Height: (a) to trigger (one state): 600mV minimum; (b) to not trigger (zero state): 200mV maximum

Protection: Input protected to ±5V dc,and ±100V at a 2% duty factor

TIMING OUTPUTS:

Fast Negative Logic Outputs:

Number of Outputs: 2, fully buffered from each other

Connectors: Front panel BNC

Load: Intended for driving a terminated 50 ohm coaxial cable

Amplitude: Nominally -16mA (current drive), -800mV on 50 ohms, limited at approximately -1 volt

Width: ≈5 nsec

Rise Time: ⩽2.5 nsec

Positive Slow Logic Output:

Connector: One front panel BNC output

Amplitude: Nominally +5 volts (4 volts minimum)

Output Impedance: ⩽10 ohms, short circuit protected, dc-coupled

DC Offset: <±500mV

Width: Nominally 500 nsec

Rise Time: ⩽±10 nsec

PROPAGATION DELAY (Negative Outputs):

Delay Jitter: Typically 30 psec fwhm for a 100mV input with a 2 nsec rise time

Temperature Drift: ⩽7 psec/°C (0 to 50°C)

TEMPERATURE OPERATING RANGE: 0 to 50°C

COUNTING RATE LIMITATIONS:

Complete dc-coupling of the module eliminates time dispersion due to changing counting rate. Maximum rate limited only by pulse pair resolution (⩽40 MHz)

POWER REQUIREMENTS:

+24V	140mA	+12V	215mA
-24V	135mA	-12V	230mA

WEIGHT:

Shipping: 5 pounds (2.3 kg)

Net: 2.75 pounds (1.25 kg)

DIMENSIONS:

Standard double width module (2.70 x 8.714 inches) per TID-20893 (Rev.)

RELATED EQUIPMENT:

The 453 obtains its power from an ORTEC 401A/402A Bin and Power Supply (or equivalent). The input can be furnished from any detector which has a negative pulse output; optimum operation with semiconductor detectors such as ORTEC Ge(Li) or Si can be obtained by using an ORTEC 454 Timing Filter Amplifier to shape the detector output pulses ahead of the 453. The outputs are compatible with all ORTEC 400 Series modular instruments, used to measure time or determine time coincidence, or to count output pulses.

3. INSTALLATION

3.1 General Installation Considerations

The 453, used in conjunction with the 401A/402A Bin and Power Supply, is intended for rack mounting. It is necessary to ensure that other equipment operated in the same rack (particularly vacuum tube equipment) has sufficient cooling air circulating to prevent any localized heating of the all-transistorized circuitry used throughout the 453. The temperature of equipment mounted in racks can easily exceed the recommended maximum unless these precautions are taken. The 453 should not be subjected to temperatures in excess of 120°F (50°C). To obtain the best in temperature stability, the 453 should not be exposed to high velocity drafts of cooling air, especially if the temperature of the cooling air is not stable.

3.2 Connection to Power – Nuclear Standard Bin, ORTEC 401A/402A

The 453 contains no internal power supply, and therefore obtains necessary operating power from the nuclear standard bin and power supply, ORTEC 401A/402A. Turn the power supply off when inserting or removing modules. The 400 Series is designed so that it is not possible to overload the power supply with a full complement of modules in the bin. However, this may not be true when the bin contains modules other than those of ORTEC design. In such instances the power supply voltages should be checked after the insertion of modules. The ORTEC 401A/402A has test points on the power supply control panel to monitor the dc voltages. The power supply voltages should read within ±0.5% of the nominal values of proper operation of NIM standard instruments.

3.3 Warm-Up Period

The lower level discriminator in the 453 is oven stabilized. For this reason a warm-up period of at least 15 minutes should be allowed before making adjustments of the lower level discriminator threshold.

It is generally recommended that the total system of bin and modules be allowed to warm-up for a period of at least one hour before making precision measurements with the equipment. This procedure permits the convection currents and temperatures in the environment of the system to stabilize.

3.4 System Connections

The 453 is capable of accepting and producing signals with very fast rise times (~2 nsec). To preserve this fidelity of response, care must be taken in making system interconnections. All inputs and outputs of the 453 (except the positive slow logic timing output) are designed to handle signals on properly terminated 50 ohm coaxial cables.

Long cable lengths inevitably cause degeneration of the signal rise time. To avoid noticeable degeneration on 2 nsec rise time signals, the use of RG-58 cable should be restricted to lengths less than 6 meters (≈20 feet). For longer lengths, a coaxial cable of quality equal to or better than RG-8 should be used. RG-8 will begin to degrade a 2 nsec rise time noticeably for lengths greater than 30 meters (≈100 feet).

For fast rise time signals, reflections caused by BNC cable connectors, tee's and unions, etc., can be a significant problem. Use of such connectors should be kept to a minimum.

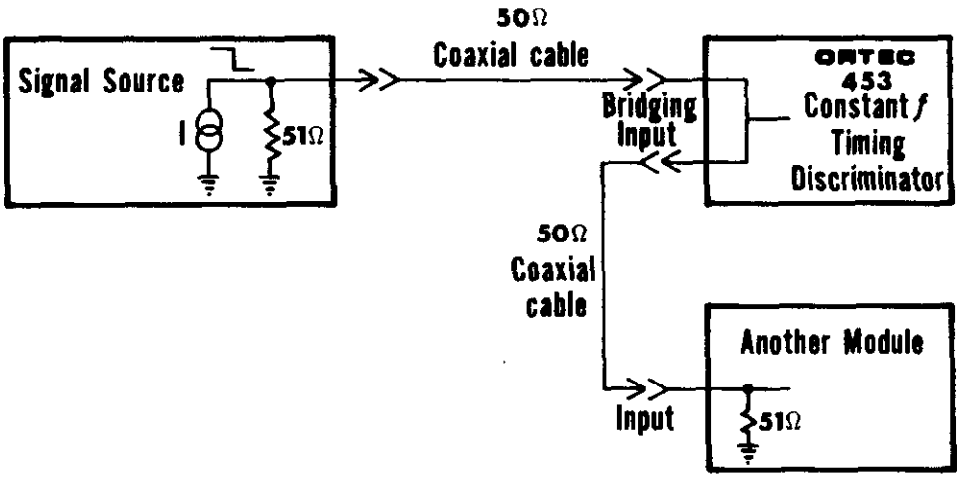
Reflections and rise time losses in cables are most serious where linear signals are involved. In the case of the 453, particular care should be taken to avoid these problems on the fast linear signal provided to the bridging input. Reflections or rise time degeneration can cause loss of the time information content in this signal, consequently degrading intrinsic time resolution of the system.

3.5 453 Input/Output Terminations

Considerable flexibility has been designed into the inputs and outputs of the 453. The following information will be useful in deriving full benefit from this flexibility.

3.5.1 Input (Bridging)

The bridging input of the 453 consists of two BNC connectors shorted together (bridged) behind the front panel. The common connectors drive a high input impedance (≈1000 ohms), making it possible to reuse the input signal. If the input signal is to be reused in another module, simply connect the input cable to the top bridging input connector, as shown in Figure 3.1 (a), and use the bottom bridging input connector to connect the signal to the next module through a 50 ohm coaxial cable. Make sure that this second cable is terminated in 50 ohms, either by the input of tne next module or by a tee and 50 ohm terminator on the input of the module. If the 453 input signal is not to be reused, terminate the input cable by adding a 50 ohm terminator to the bottom bridging input connector (Figure 3.1 (b)). To minimize reflections it is recommended that the signal source be back-terminated in 50 ohms, where practical.



(a) Input signal re-used in another module

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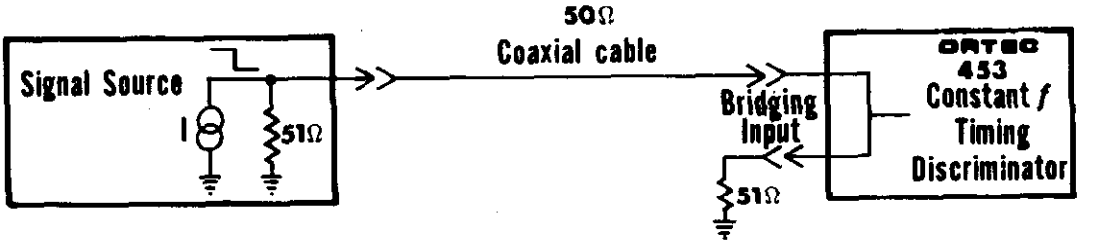


(b) Input signal terminated at the 453

Figure 3.1. Use of the 453 Bridging Input

3.5.2 Monitor Output

The monitor output should be observed on a terminated 50 ohm coaxial cable. However, no terminator is required on the output connector when not in use, since the monitor output is reverse terminated internally in 50 ohms.

3.5.3 50Ω External Shaping Delay Input/Output

When an external 50 ohm shaping delay is not used (e.g., leading edge trigger mode) the external shaping delay input and output connectors should be terminated in 50 ohms.

3.5.4 Fast Negative Timing Outputs

The negative timing outputs are designed to drive a 50 ohm terminated cable. However, it is not necessary to terminate either output when not in use. Complete buffering prevents interaction between the two outputs.

3.5.5 Positive Timing Output

This output is intended to drive 93 ohm cable (RG-62) for the purpose of operating scalers and slow logic circuitry. For cable lengths longer than 2 meter (≈7 feet) it is recommended that the cable be terminated in its characteristic impedance. This output can also drive a terminated 50 ohm cable, but with a slightly reduced amplitude.

3.6 Input Offsets

Since the 453 is dc-coupled from input to output, it is necessary to ensure that the signal provided to the input has no dc offset (<±5mV).

4. OPERATING INSTRUCTIONS

4.1 The Constant Fraction of Pulse Height Trigger (CFPHT) Mode

In order to set up the 453 for a particular application as a Constant Fraction of Pulse Height Trigger it is necessary to understand the principle of operation. The CFPHT has been treated in great detail for timing with photomultipliers in several papers.[1,2,3,7] Its application to timing with silicon surface barrier detectors,[6] and Ge(Li) detectors[4,5] has also been discussed. For this reason, only the basic principle of operation of the circuit will be dealt with here.

4.1.1 Principle of Operation

The purpose of the CFPHT technique is to trigger at a selected point on the leading edge of the input pulse, such that the effective triggering threshold occurs at a fraction *f* of the full height of the input pulse. As illustrated in Figure 4.2 (a), if the input pulse height is V_a, and the selected triggering threshold is V_f, then the fractional triggering threshold is defined as

$$f = \frac{V_f}{V_a} \qquad (4.1)$$

Figure 4.1 shows a simplified block diagram of the 453. In order to generate the proper pulse shape for triggering at a fraction *f* on the leading edge, the output of the input buffer is fed through two paths. In one leg of the system the input pulse is attenuated to a fraction *f* of its original height (controlled by the front panel FRACTION switch). In the other path the pulse is inverted and delayed by an interval T_d. Both signals are added together in the summing buffer to form a zero-crossing signal. The delay T_d (50 ohm shaping delay) is chosen so that the inverted pulse adds to the attenuated pulse after the attenuated pulse has reached full amplitude. In this manner a bipolar pulse is formed with a zero-crossing point corresponding to the desired fractional triggering threshold on the leading edge of the input pulse, as shown in Figure 4.1. A zero-crossing discriminator triggers at the zero-crossover point to provide the time pickoff information at the 453 output. Since the time of zero crossing is independent of pulse height, the timing walk of the system is negligible.

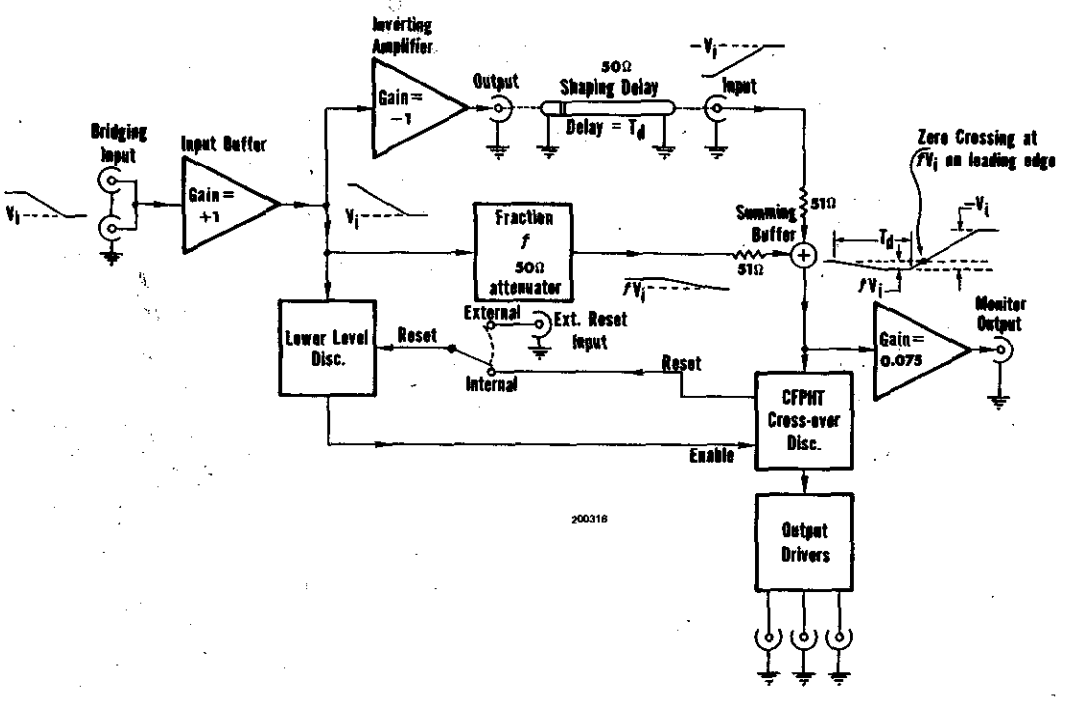


Figure 4-1. Simplified 453 Block Diagram

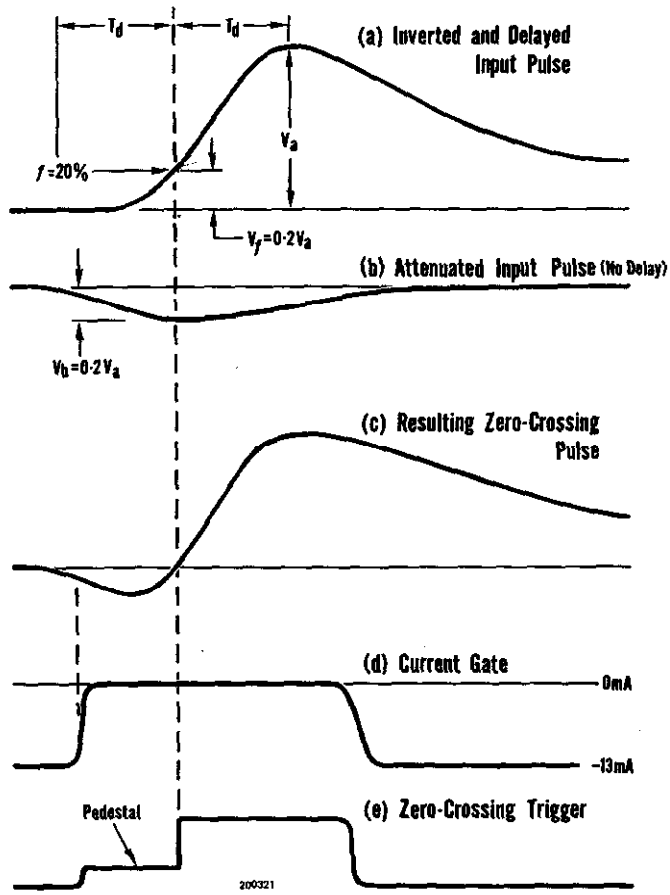


Figure 4-2. Pulse Shapes in the Constant Fraction of Pulse Height Trigger

4.1.2 Choice of the 50 Ohm External Shaping Delay

Frequently the input pulses do not have a flat top, but instead exhibit a well defined peak amplitude as illustrated in Figure 4.2 (a). In this case a more careful choice of the 50 Ohm External Shaping Delay is required. Once the desired fractional triggering threshold f has been selected, the shaping delay must be chosen to provide a delay equal to the time between the point at which the leading edge crosses the fractional triggering threshold and the peak amplitude point. In Figure 4.2 this delay has been labeled T_d. The example given is for f = 20%.

In the 453 there is approximately 1.3 nsec internal delay in the shaping delay circuit. This means that the required external 50 ohm shaping delay, t_d, should be calculated from

$$t_d = T_d - 1.3 \text{ nsec} \qquad (4.2)$$

For moderately long delays RG-58 coaxial cable may be used. It provides a delay of approximately 4.7 nsec/meter (1.5 nsec/ft). The selection of the external shaping delay may be checked by observing the output pulse shape at the Monitor Output. The pulse shape should correspond to that shown in Figure 4.2 (c).

For timing with Ge(Li) detectors using the amplitude and rise time compensated (ARC) technique[4,5,8] the 453 is not used in the conventional CFPHT mode. Refer to the application notes on Ge(Li) timing for the proper selection of t_d in this case.

Typical examples for the choice of the triggering fraction and shaping delay are given in the application notes (Section 5) for timing with scintillation and Ge(Li) detectors.

4.1.3 Walk Adjustment

Once the triggering fraction and external shaping delay have been properly selected, the cross-over discriminator threshold may be adjusted in the following manner to mininmize the walk with changing pulse height.

1. Connect the desired signal source (detector, etc.) to the 453 bridging input with 50 ohm coaxial cable.
2. Terminate this cable in 50 ohms by applying a 50 ohm terminator to the second connector on the bridging input.
3. Set a suitable source of radiation in front of the detector. The source should be chosen so that the detector output produces a wide range of pulse heights (20:1).
4. Adjust the detector system gain so that the maximum pulse height of interest is 1000mV (negative polarity) at the 453 input.
5. Set the 453 lower level discriminator to 50mV (or higher if it is necessary to avoid triggering on noise).
6. Connect one of the fast negative timing outputs to the trigger input of a sampling oscilloscope with a *terminated* 50 ohm coaxial cable of length $\leq$1 meter ($\leq$3 feet).
7. Connect the 453 monitor output to the input of the sampling oscilloscope with a 50 ohm coaxial cable of length $\geq$2 meters ($\geq$6 feet). Ensure that the cable is terminated either by a 50 ohm oscilloscope input impedance, or by a tee and 50 ohm terminator if necessary.
8. Turn the walk adjust control (front panel) to the full counter-clockwise position.
9. Check that the oscilloscope is triggering properly on the 453 timing output.
10. Set the oscilloscope sensitivity to 2 nsec/cm (horizontal) and 5mV/cm (vertical) align the delays to observe the monitor pulse.
11. Slowly turn the walk adjust control clockwise until the monitor pulse moves abruptly to the left on the oscilloscope display (Figure 4.3 to Figure 4.4).
12. Trim the walk adjust control until all pulses appear to cross through zero pulse height at the same time (see Figure 4.5). If the walk adjust is too far clockwise, the point through which all pulses converge will appear above the baseline as illustrated in Figure 4.6. For a setting that is too far counter-clockwise, the characteristic shown in Figure 4.4 will result.
13. A finer adjustment of the walk may be made by observing the shape of the peak in a coincidence time spectrum and trimming for best peak symmetry.

Note that use of a slower rise time oscilloscope may distort the above adjustments. The oscilloscope rise time should be less than the signal rise time at the monitor output for proper adjustment.

4.2 Fast Zero-Crossover Pickoff Mode

The 453 can be used as a fast zero-crossover pickoff with the settings listed below. The zero-crossing pulse must have a negative leading phase.

1. Turn the FRACTION switch to $f = 0.5$.
2. Omit the external shaping delay, and terminate the 50 ohm external shaping delay output and input separately in 50 ohms.

3. Adjust the walk as described in Section 4.1.3.

The acceptable input dynamic range for fast pulses extends from 50mV to 1000mV. For slow pulses (rise times >50 nsec) advantage may be taken of the input limiter to extend this range. In the latter case, the dynamic range is limited only by the input protection (±100V).

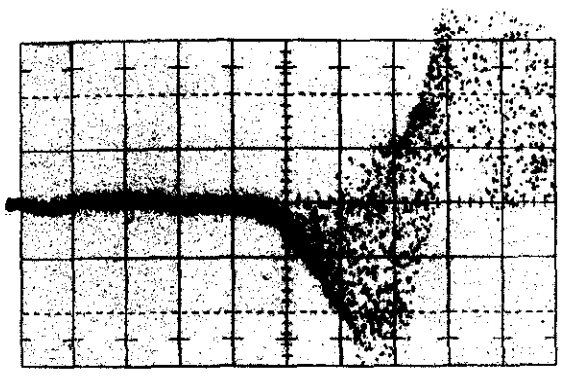


Figure 4-3. Monitor Output With Sampling Oscilloscope Triggered From 453 Timing Output
Walk Adjust: full counter-clockwise
Vertical Scale: 5mV/cm
Horizontal Scale: 2 nsec/cm
Fraction: f = 0.2

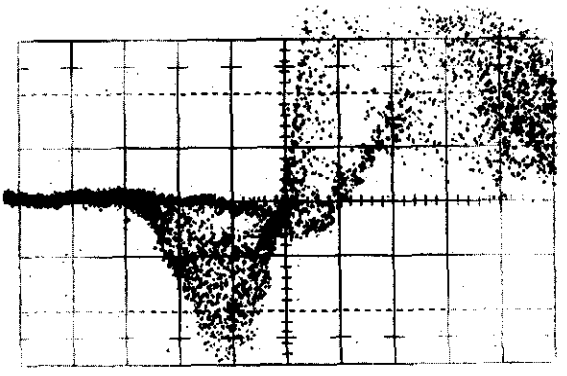


Figure 4-4. Same as Figure 4-3, but with Walk Adjust Slightly too far Counter-Clockw

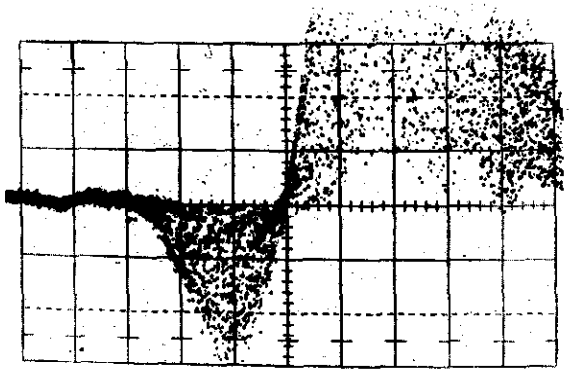


Figure 4-5. Same as Figure 4-3, but with Correct Walk Adjustment

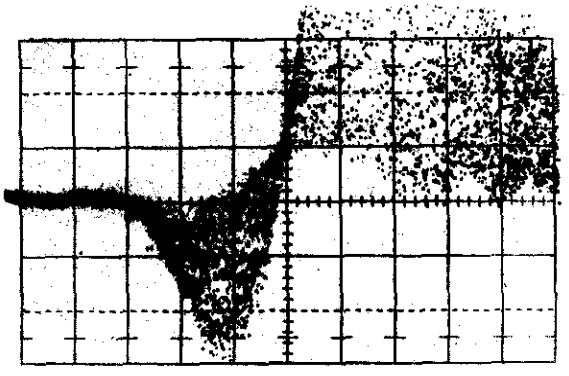


Figure 4-6. Same as Figure 4-3, but with Walk Adjustment Slighly too far Clockwise

4.3 Leading Edge Discriminator Mode

The 453 may be used as a leading edge discriminator in the following fashion.

1. Set the FRACTION switch to $f = 0$.
2. Omit the external shaping delay and terminate both the 50 ohm external shaping delay input and output in 50 ohms.
3. Turn the walk adjust control to its full counter-clockwise position.

The lower level discriminator will now function as a leading edge discriminator with a threshold variable from -50mV to -1000mV. Signals up to 100V in amplitude can be accepted.

4.4 Internal/External Reset Modes

Two modes of reset are provided in the 453 and are selectable with a front panel switch.

4.4.1 Internal Reset

In the internal (INT) reset mode, the 453 dead time is determined by the input pulse duration above the lower level discriminator threshold. Once the CFPHT zero-crossing discriminator has produced an output, the 453 attempts to reset the lower level discriminator. However, the lower level discriminator will not reset until the input pulse falls approximately 25mV below the lower level discriminator threshold. The lower level discriminator remains dead for approximately 25 nsec after reset. Hence the pulse pair resolution, t_{pp}, of the 453 is given by

$$t_{pp} \approx 25 \text{ nsec} + W \qquad (4.3)$$

where W is the interval (in nsec) from the time at which the input pulse first crosses the lower level discriminator to the time at which it falls approximately 25mV below the lower level.

4.4.2 External Reset

In some cases the trailing edge of the input pulse is characterized by a large amount of ringing (damped oscillations), or a high ratio of noise to slope (e.g., a signal from NaI(Tl)). In these situations the fast recovery time provided by the internal reset mode can give rise to multiple triggering on a single input pulse. Where this problem is likely to occur, the external reset mode should be used. One of the timing outputs can be used to generate an appropriately delayed signal for the external reset input. The delay should be sufficiently long to hold the 453 dead until all undesirable effects on the input pulse have subsided.

The external reset may also be used to hold the 453 dead until logic decisions have been completed in other modules comprising the system. The external reset provided by the system may be delayed up to 30μsec.

If no reset signal is provided, either externally or internally, the 453 automatically generates an internal overrange reset which resets the 453 after approximately 40μsec. This function can be disabled by removing transistor Q34 from its socket.

4.4.3 Extending the Range of Fractions

The front panel fraction switch on the 453 provides for $f = 0.1$, 0.2, 0.3, 0.4, and 0.5. If other fractions are desired it is possible to extend the range of values by inserting either a 50 ohm attenuator or a fast amplifier in series with the external shaping delay as indicated in Figure 4.7. If a fraction f is desired and the front panel switch is set at a fraction f, then the attenuator or the amplifier gain should be chosen according to equation (4.4) or (4.6).

$$f' = \frac{f}{\beta} \tag{4.4}$$

where

$$\beta = \frac{e_o}{e_i} \tag{4.5}$$

or

$$f' = \frac{f}{A} \tag{4.6}$$

where

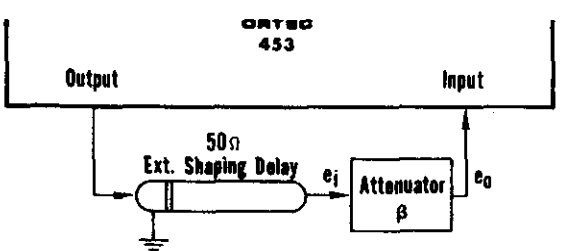
$$A = \frac{e_o}{e_i} \tag{4.7}$$

The amplifier should have a 50 ohm input impedance and be capable of driving a fast positive polarity signal (up to 1 volt high) into a 50 ohm load with negligible rise time slewing.

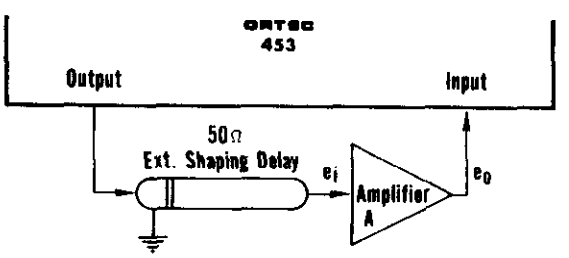
The attenuator should be a high fidelity 50 ohm T attenuator. Figure 4.7 (c) with equations (4.5), (4.8), and (4.9) shows the design criteria for such an attenuator.

$$R_1 = 50 \left[\frac{1-\beta}{1+\beta}\right] \text{ohms} \tag{4.8}$$

$$R_2 = \frac{100\beta}{1-\beta^2} \text{ ohms} \tag{4.9}$$

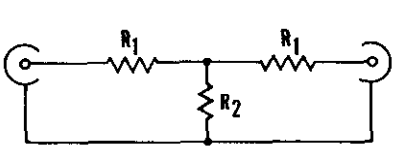


(a) Use of an Attenuator to Increase Triggering Fraction



(b) Use of an Amplifier to Decrease Triggering Fraction

200322



(c) A 50 ohm T Attenuator

Figure 4-7. Special Circuits for Extending Range of Triggering Fractions

5. APPLICATION NOTES

5.1 Timing With Fast Scintillation Detectors

Figure 5.1 shows a typical system for timing with fast scintillation detectors using scintillators such as Naton 136, Pilot B, NE 102, NE 111, NE 213, etc. The 453 Constant Fraction Timing Discriminator has been employed in the start channel. An external shaping delay consisting of approximately 32 inches (81 cm) of RG-58 is typical. Figure 5.2 compares the CFPHT time resolution to leading edge discriminator results as a function of the fractional triggering threshold. From this graph it is apparent the $f = 0.2$ is a convenient choice for this application of the 453.

Figure 5.3 provides a sample of the time resolution obtainable for a 10:1 dynamic range. More extensive discussions of timing with fast scintillators can be found in references 1, 2, 3, and 7.

5.2 Timing With NaI(T1) Detectors

Figure 5.4 shows a time pickoff system for NaI(T1) detectors, which can be used in the system in Figure 5.1. The 453 is used in the external reset mode with the 416 delay set at $\approx 1\mu$sec to prevent multiple triggering on the NaI(T1) pulse.[7] Figure 5.5 compares leading edge timing to the CFPHT for NaI(T1). A fraction of $f = 0.1$ is clearly desirable for NaI(T1) timing. Figure 5.6 shows wide dynamic range time resolution for this application.

5.3 Timing With Ge(Li) Detectors

Figure 5.7 illustrates the timing technique developed by Chase[4] for Ge(Li) detectors. This method will be referred to as the ARC (amplitude and rise time compensated) technique. The left side of the diagram is a conventional CFPHT timing system for fast scintillators. On the right hand side, ARC and leading edge timing systems are shown for comparison.

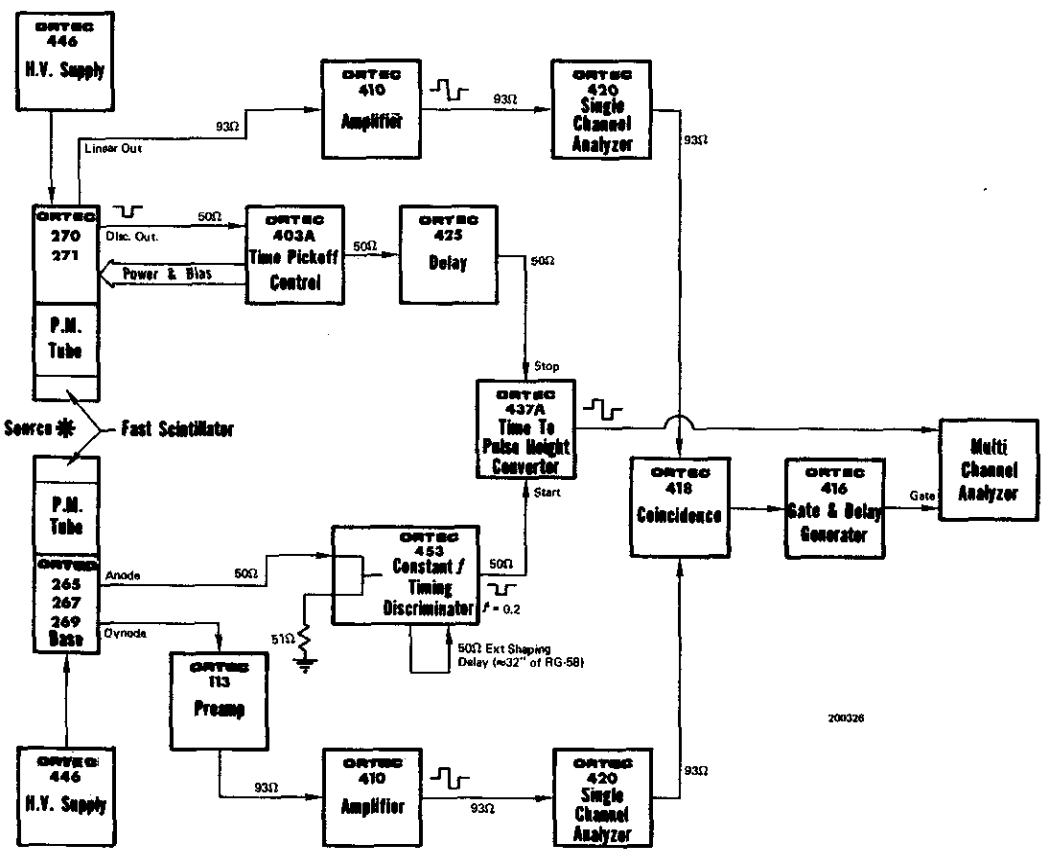


Figure 5-1. A Typical System for Timing with Fast Scintillation Detectors (Naton 136, Pilot B, NE102, NE2/3 etc.)

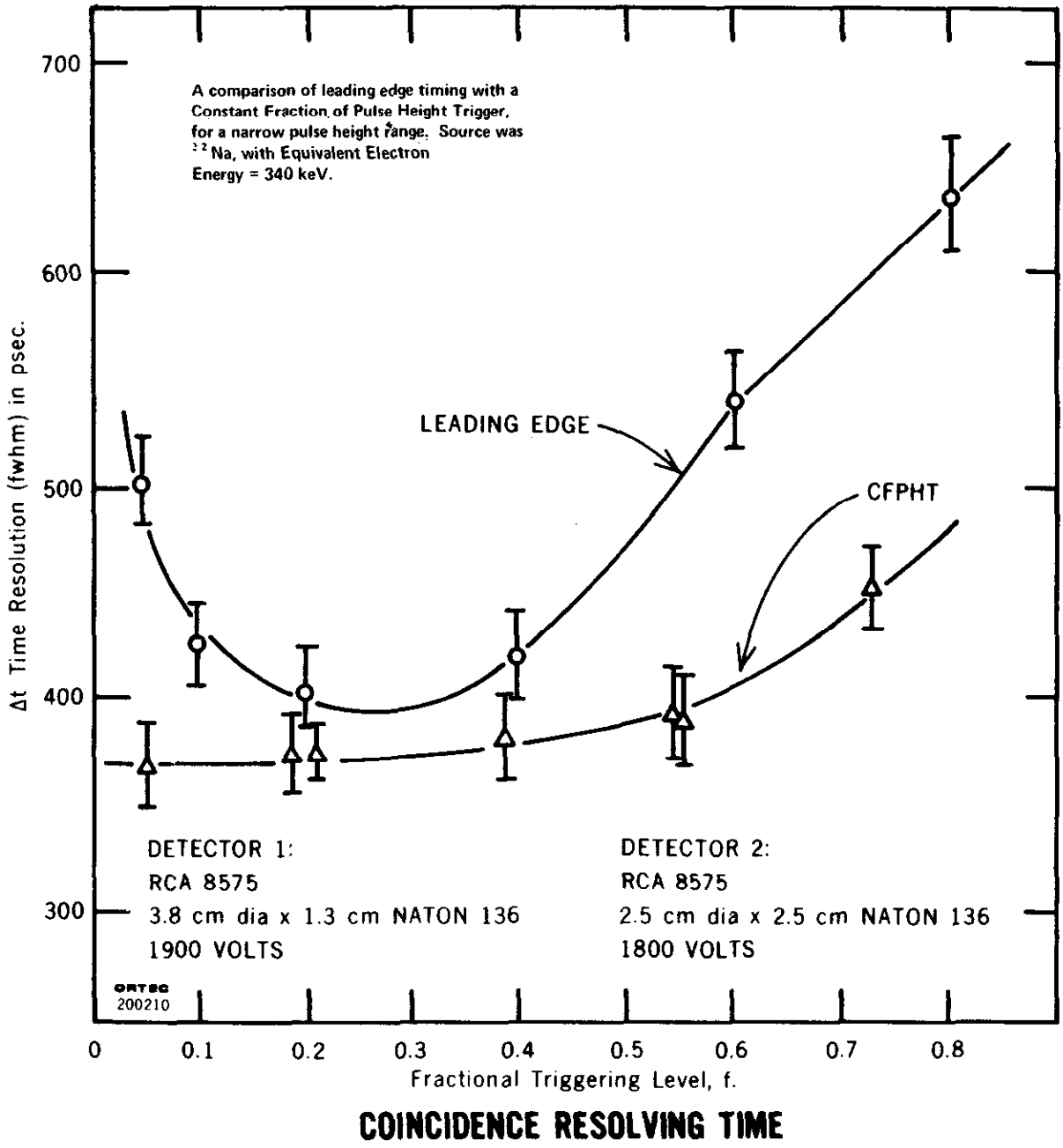


Figure 5-2. A Comparison of Leading Edge Timing With a Constant Fraction of Pulse Height Trigger (from Ref. 3) For a Narrow Pulse Height Range. The Source Was ^{22}Na. Δt is the fwhm Time Resolution.

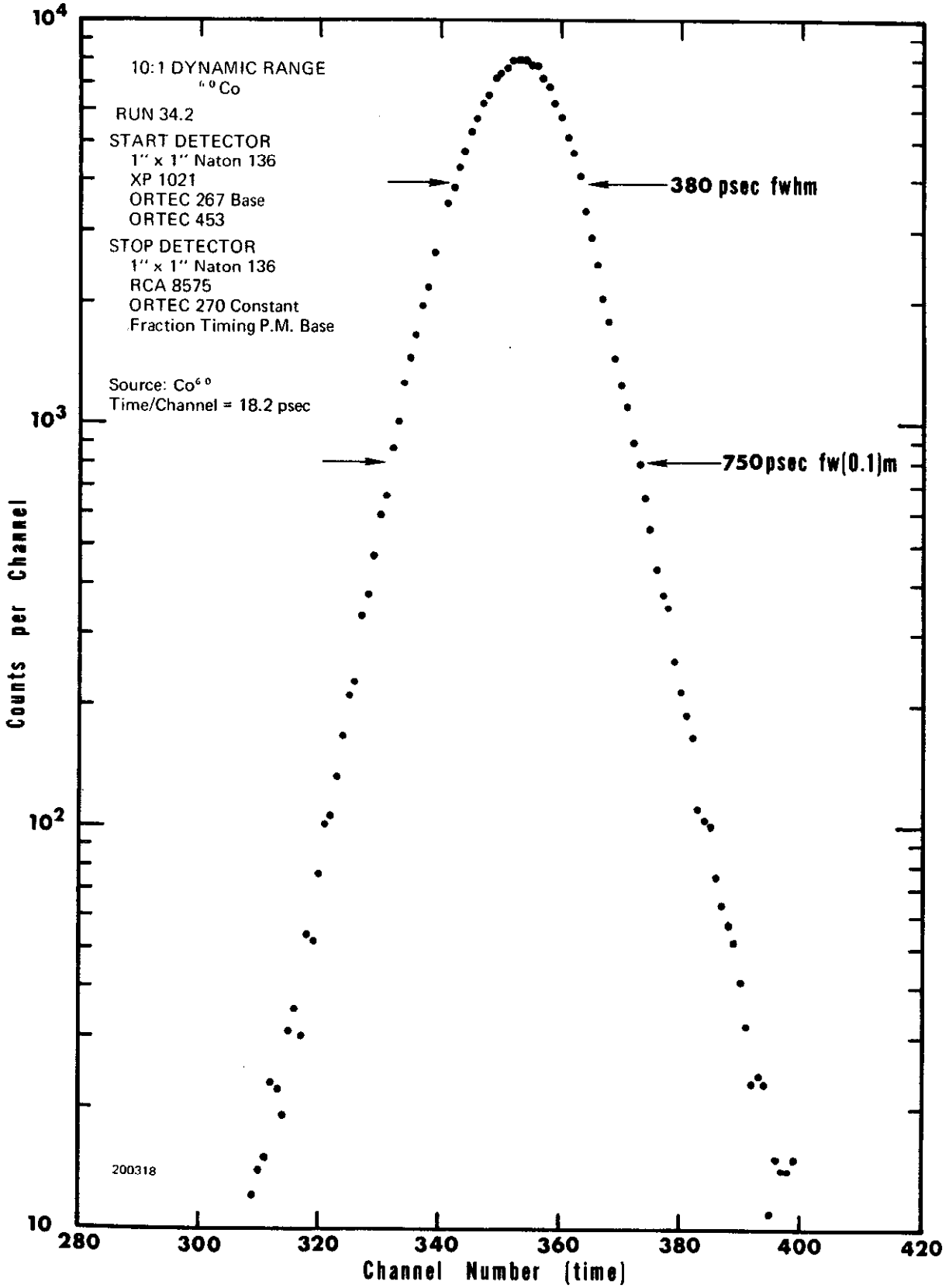


Figure 5-3. 10:1 Dynamic Range Time Resolution Obtained With the System in Figure 5.1.

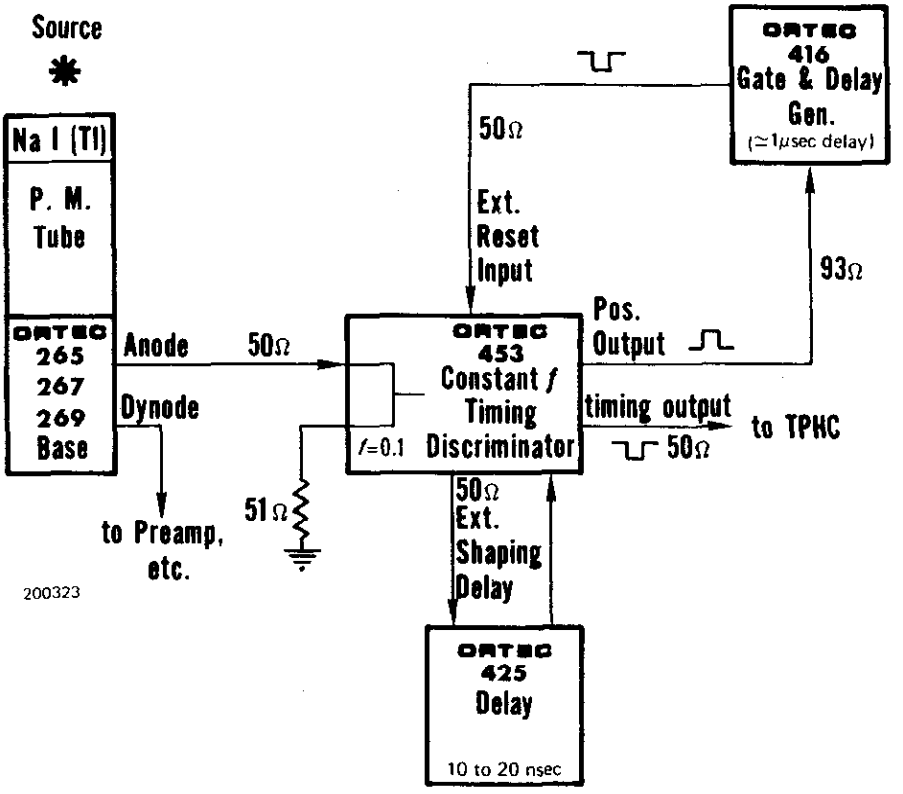


Figure 5-4. A Time Pickoff System for NaI(Tl) Detectors

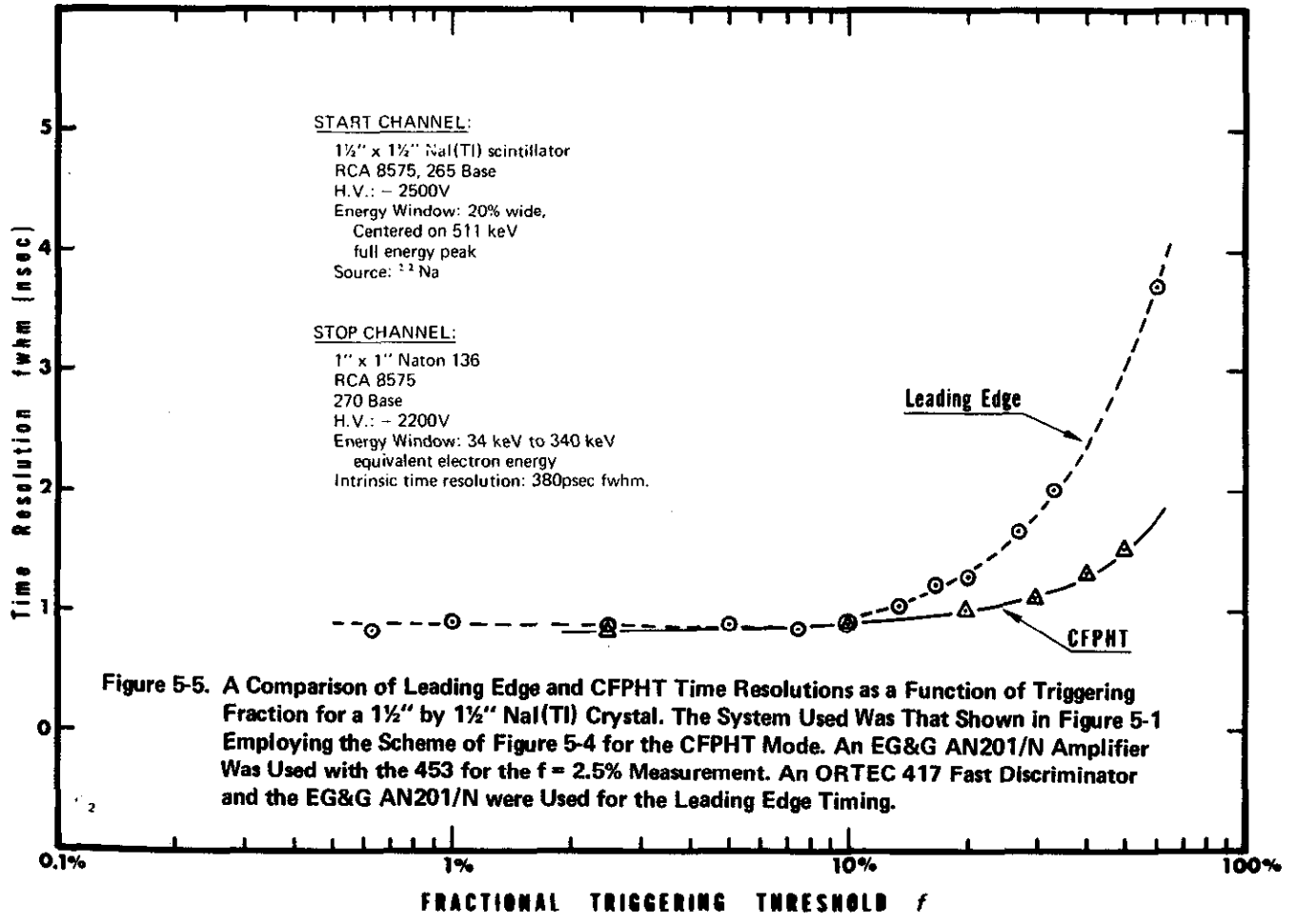


Figure 5-5. A Comparison of Leading Edge and CFPHT Time Resolutions as a Function of Triggering Fraction for a 1½" by 1½" NaI(Tl) Crystal. The System Used Was That Shown in Figure 5-1 Employing the Scheme of Figure 5-4 for the CFPHT Mode. An EG&G AN201/N Amplifier Was Used with the 453 for the f = 2.5% Measurement. An ORTEC 417 Fast Discriminator and the EG&G AN201/N were Used for the Leading Edge Timing.

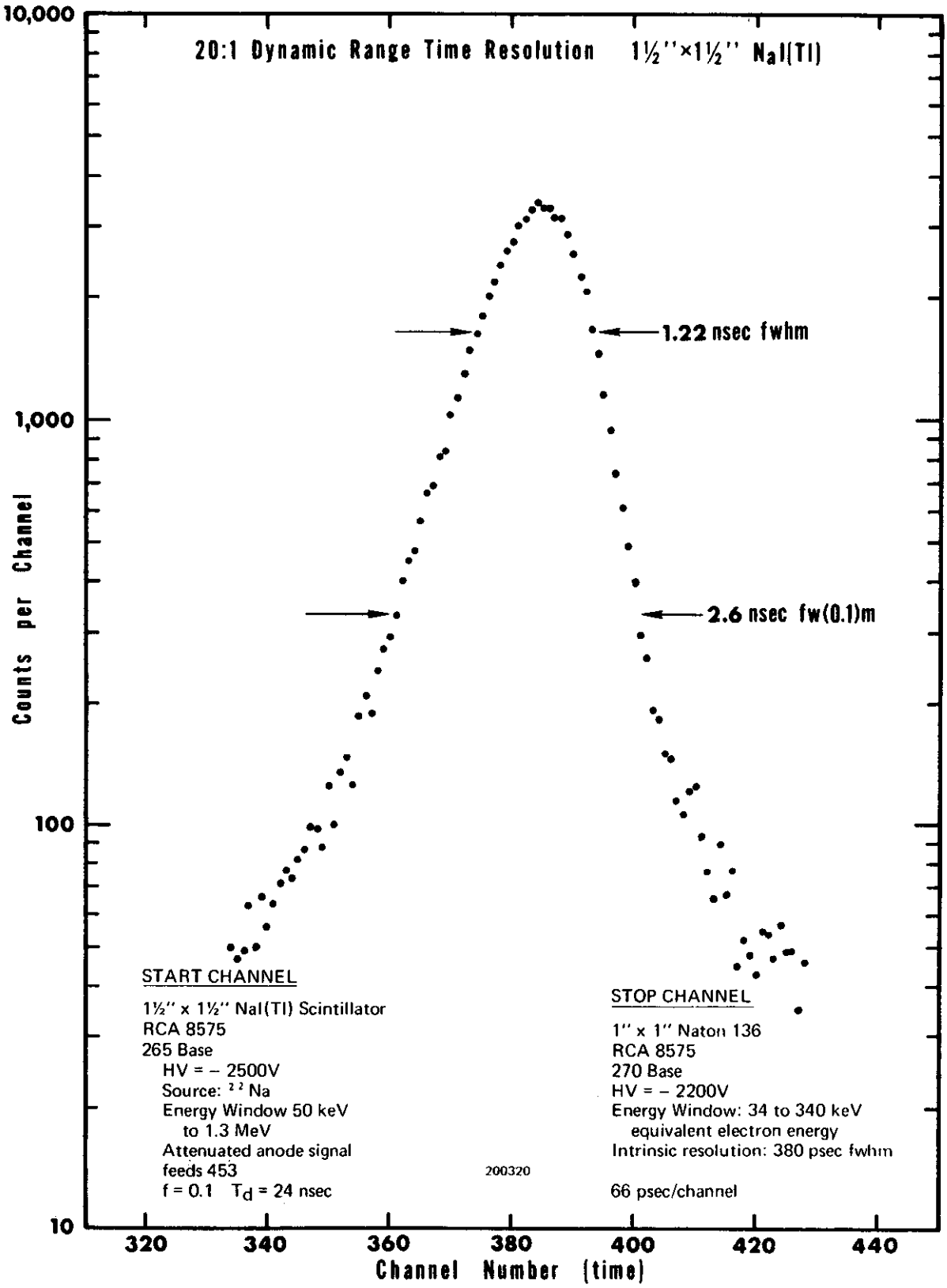
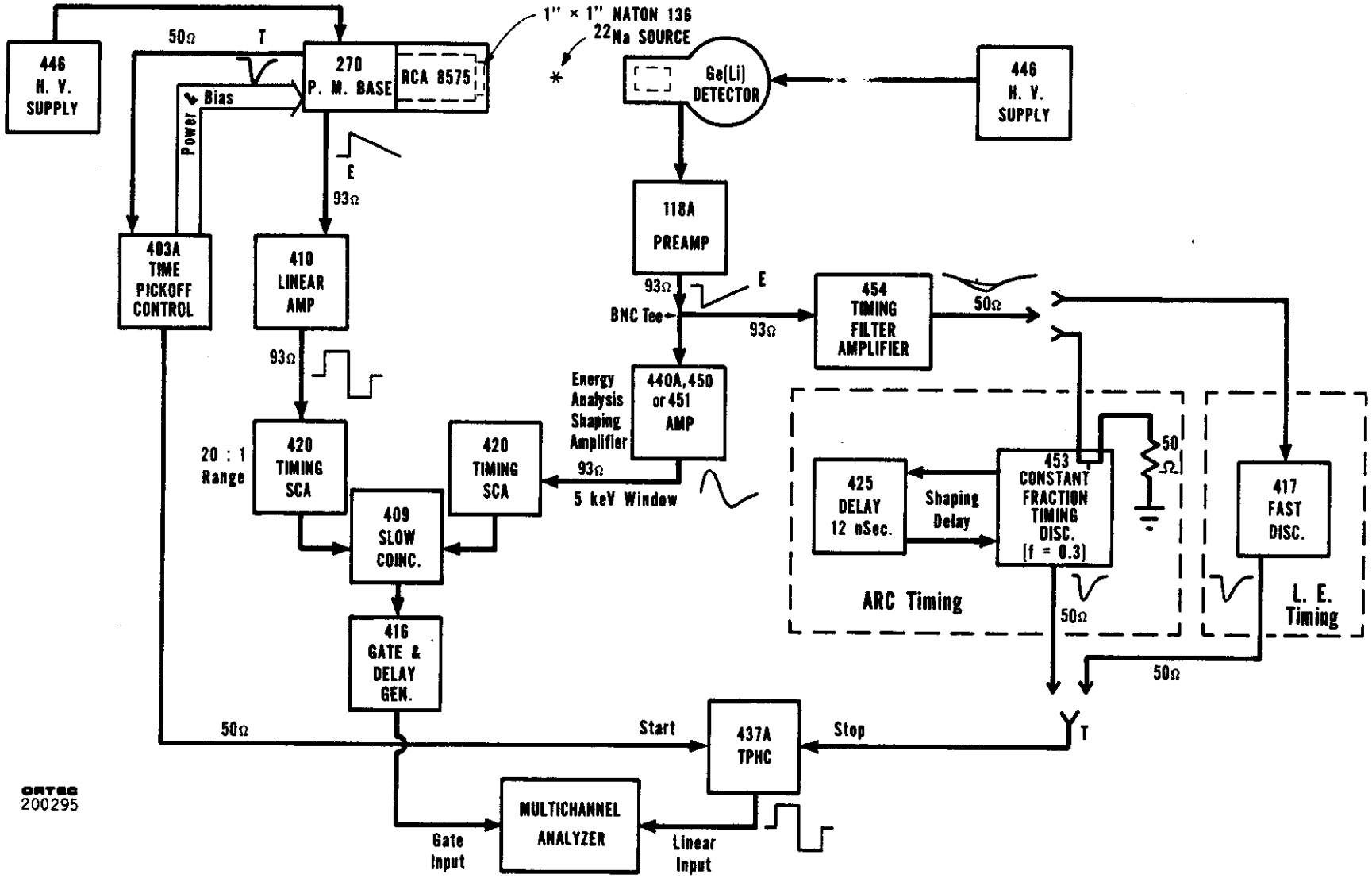


Figure 5-6. Typical 453 Wide Dynamic Range Time Resolution (50 keV to 1.3 MeV) Obtained with the Systems Described in Figures 5-1 and 5-4 Using a 1½" x 1½" NaI(Tl) Detector. The Source is ^{22}Na.



Block Diagram Showing Leading Edge (L.E.) Timing versus Amplitude and Risetime Compensated (ARC) Timing Systems for Ge(Li) Detectors.

The output from the preamplifier is brought to the shaping amplifier for energy analysis (440A, 450, or 451) through 93 ohm cable. At the energy analysis shaping amplifier input a BNC tee is used, and 93 ohm cable is employed to carry the preamplifier signal to the 454 Timing Filter Amplifier input. It is normally recommended that the cable be terminated in 100 ohms at the 454 input. However, one can leave the receiving end of the 93 ohm cable unterminated and rely on the 93 ohm output impedance of the preamplifier (for preamps with 93-100 ohm output impedances) to provide series termination. Care must be taken to ensure that the 454 input is situated at the receiving end of the cable, and also that the BNC tee is directly attached to the energy analysis amplifier input. If the 454 is not at the end of the cable, the reflected pulse from the unterminated receiving end of the cable can cause distortion of the leading edge of the signal as seen by the 454.

A detailed discussion of the operation of this system has been presented elsewhere.[4,5,8] Consequently, the following treatment will be restriced to some of the setup procedures required for a typical system employing a coaxial Ge(Li) detector.

The filters on the 454 should be set to "integration out" and "differentiation = 100 or 200 nsec". A typical setting for the 453 is $f = 0.3$ with an external shaping delay of approximately 14 nsec (total).

The gain of the 454 must be adjusted to achieve the signal conditions discussed below.

Figure 5.8 (a) shows the well-known spectrum of charge signal shapes for planar Ge(Li) detectors.[4,8] For a monoenergetic event, the charge collection time from the detector varies from a minimum of t_{min} to a maximum, t_{max}. Generally, $t_{max} \approx 2t_{min}$. These two extremes produce pulse shapes with an approximately linear rise. Between the two limits are families of pulses starting with the maximum slope, followed by a break to the minimum slope. Several examples of these have been included in Figure 5.8 (a). This model is, of course, an extremely simplified description of the actual process in Ge(Li) detectors. For planar detectors the model is fairly accurate. On the other hand, the effects of geometry and volume in coaxial detectors tend to wash out the shapes illustrated in Figure 5.8 (a). The simplified model is useful, however, in selecting the pulse amplitudes to be presented to the 453.

If the 454 differentiation switch is set to the OUT position, the resulting signal for a selected full energy peak will appear similar to those depicted in Figure 5.8 (a). In Figure 5.8 (b) a fraction f, and an external shaping delay of length T_d have been selected on the 453 such that the heavy lined signal is observed at the monitor output. Only the extreme rise times have been drawn to simplify the argument. Note that both signals cross the zero baseline at the same time. All signals for which the slope does not change before the time $t = T_d (1 - f)$ will cross through zero at the same time.

Figure 5.8 (c) illustrates the limitation on the maximum input pulse height to the 453. To preserve linearity for the cross-over point, the 453 input must not saturate before the zero-crossing time $t = T_d (1 - f)$. This means that the maximum signal height at the 453 input is

$$V_{max} = \frac{t_{min}}{T_d} (1 - f) \text{ volts} \qquad (5.1)$$

For example with $T_d = 14$ nsec, $t_{min} = 50$ nsec, and $f = 0.3$

$$V_{max} = \frac{50}{14} (1 - 0.3) = 2.5 \text{ volts} \qquad (5.2)$$

Figure 5.8 (d) illustrates the minimum input pulse height limitation for proper operation. To allow the zero-crossing discriminator to trigger on the zero-crossing point, the lower level discriminator must

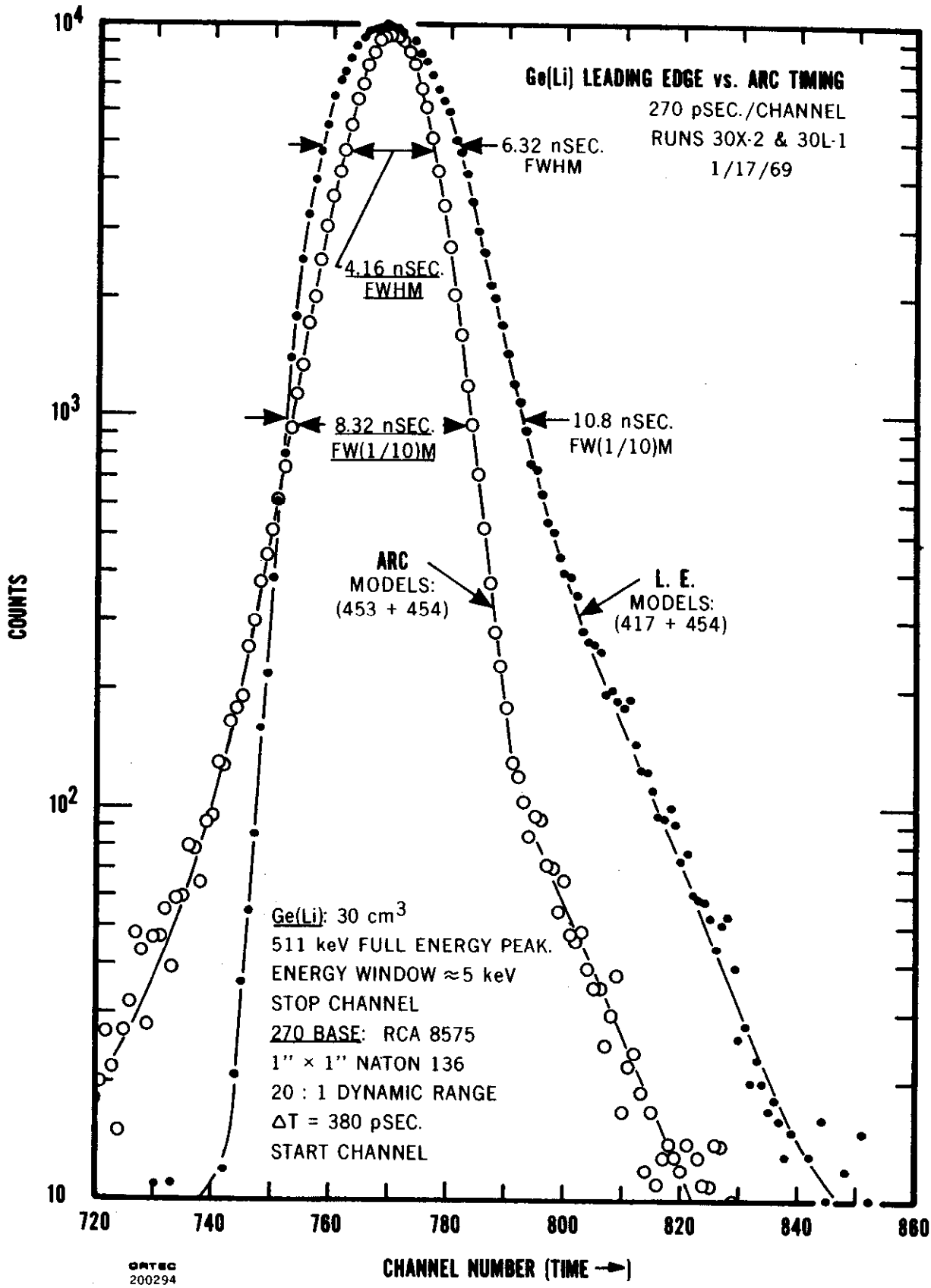


Figure 5-9. A Comparison of the Time Resolution Obtained with the Amplitude and Risetime Compensated (ARC) technique Introduced by Chase[4] Versus Conventional Leading Edge (L.E.) Timing. A 5 keV Windown Selected the 511 keV Full Energy Peak from the 30 cm^3 Ge(Li) Detector.

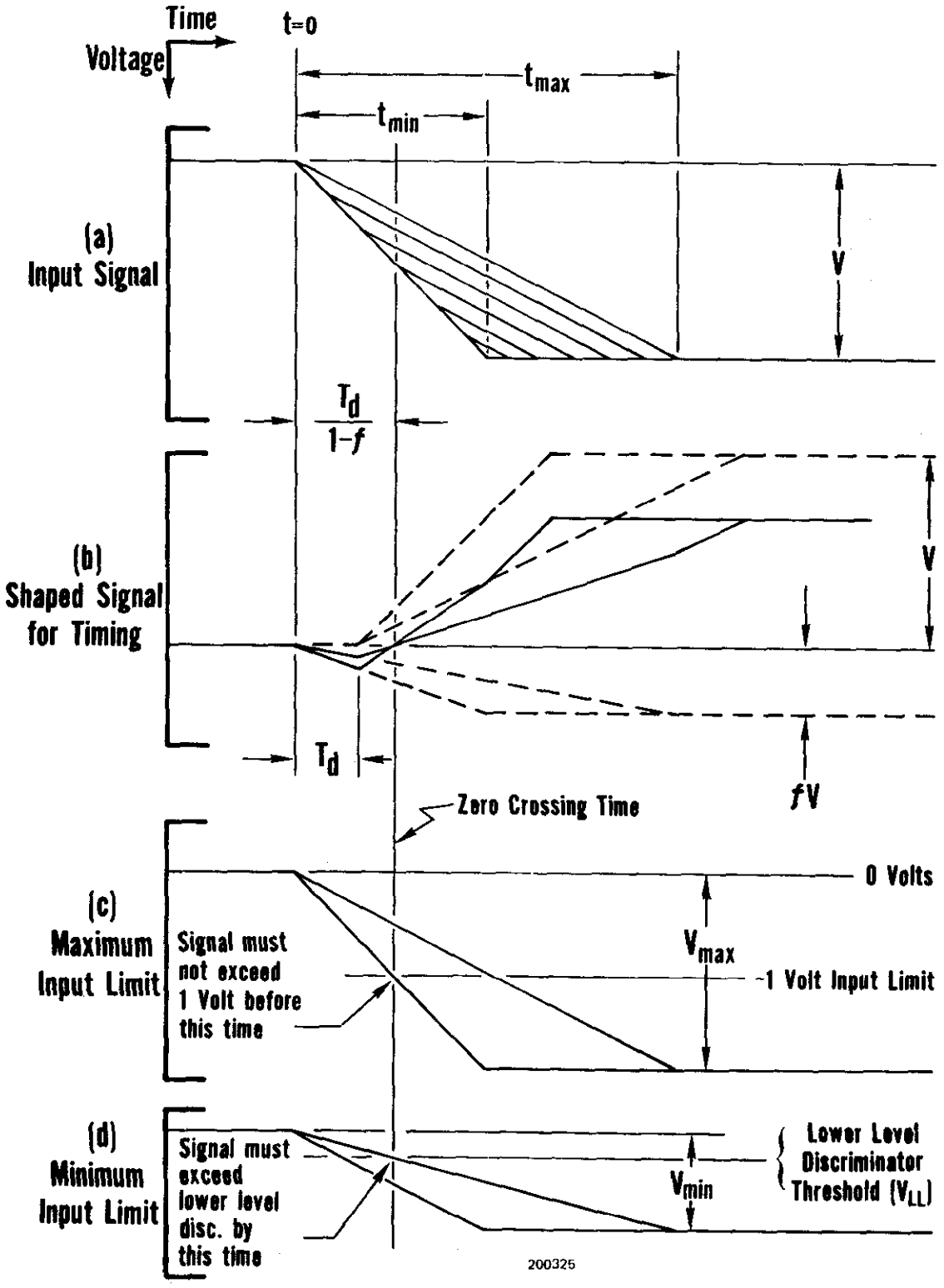


Figure 5-8. Pulse Shape Considerations for the ARC Timing Technique.

have been triggered before time t = T_d (1 - f). This implies that the minimum input pulse height limitation is

$$V_{min} = \frac{t_{max}}{T_d} (1 - f) V_{LL} \qquad (5.3)$$

where V_{LL} is the lower level discriminator threshold. For T_d = 14 nsec, t_{max} = 100 nsec, f = 0.3 and V_{LL} = 50mV

$$V_{min} = \frac{100}{14} (1 - 0.3) \times 50 = 250mV \qquad (5.4)$$

A single channel analyzer should be used on the energy pulse to restirct the accepted amplitudes in the total system to those specified in equations (5.1) and (5.3).

The walk adjustment is carried out as described in Section 4.1.3 with the following exceptions. A slower oscilloscope may be used (Tektronix 585 or equivalent) since the rise times are slower. All pulse amplitudes below V_{min} in equation (5.3) should be ignored since they will trigger late as described above. The lower level discriminator should be set as close to the noise level as possible provided it does not cause early triggering.

Figure 5.9 compares ARC and leading edge timing methods for a narrow dynamic range. The system in Figure 5.7 was used to obtain these results.

5.4 Use With a Fast SCA

In Figure 5.10 a system employing a fast single channel analyzer is illustrated. The 425 delay should be adjusted so that the 453 negative timing output arrives at the C120B/N input slightly after the leading edge of the TD101 output pulse. The TD101 pulse must also adequately overlap the 453 output. With these precautions, the leading edge time of the C102B/N AND output will correspond to the leading edge of the 453 output.

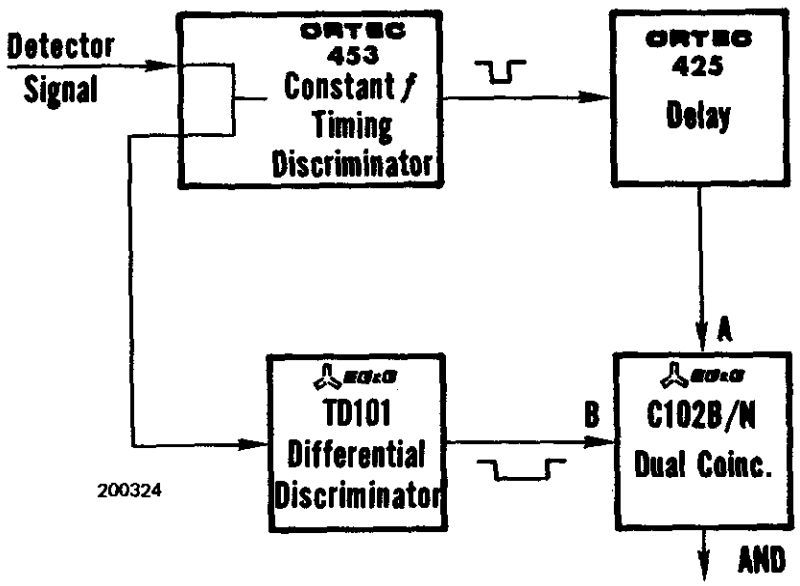


Figure 5-10. Use of the 453 with a Fast SCA

5.5 Extension of the 453 Dynamic Range

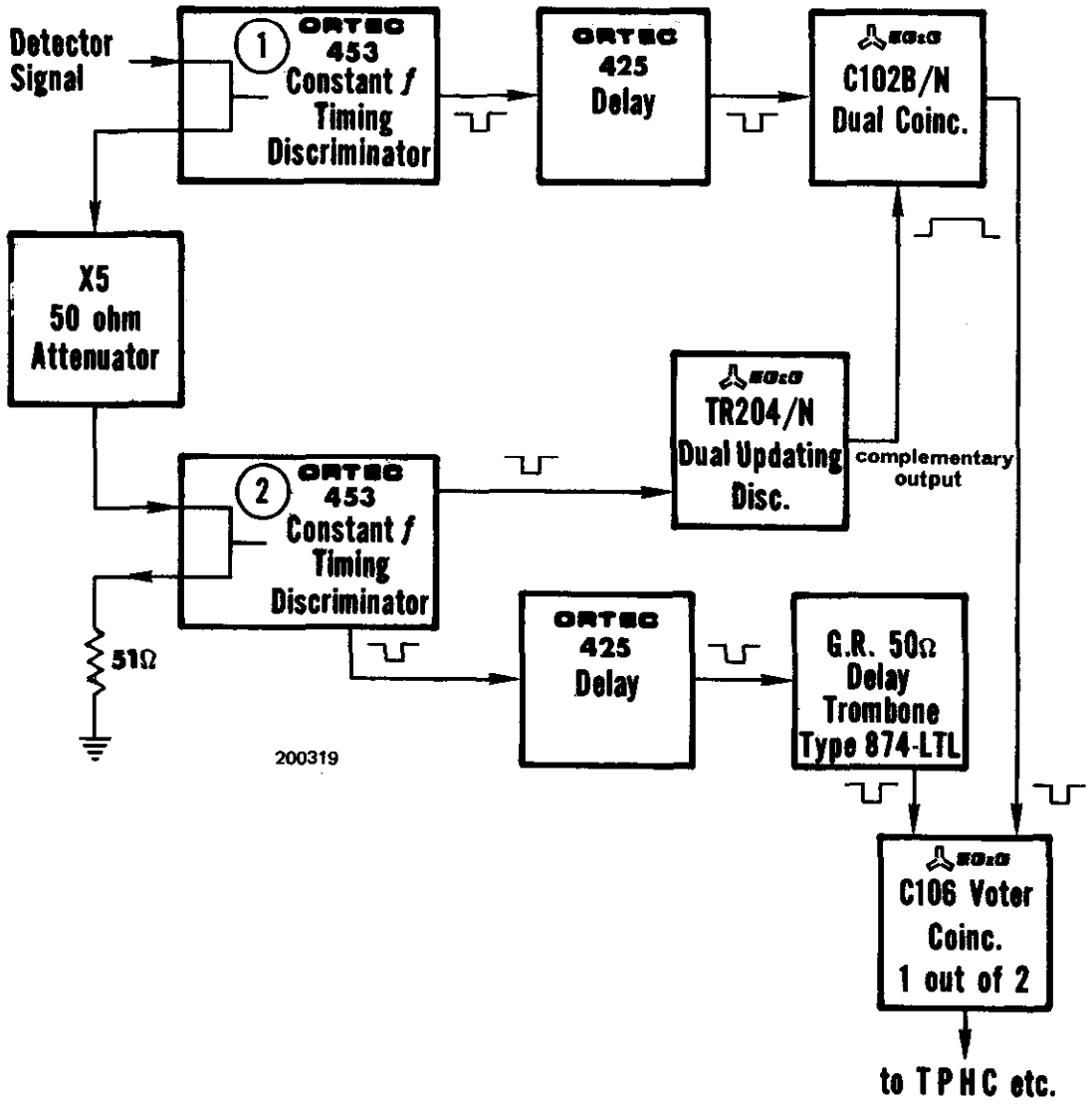


Figure 5-11. System for Extending the 453 Dynamic Range to 100:1

Figure 5.11 shows a method for increasing the 453 dynamic range to 100:1. The 453 #1 covers the range from 50mV to 1 volt. A X5 attenuator (high frequency 50 ohm type) allows 453 #2 to cover the range from 250mV to 5 volts. A blanking pulse is generated from the output of 453 #2 to prevent the pulse from 453 #1 from passing through the C102B/N coincidence module whenever 453 #2 generates a timing signal. The TR 204/N complementary output signal width and the 425 delay are adjusted to achieve proper blanking. The 425 delay and adjustable G. R. delay trombone* are used to match propagation delays in the two channels. With proper alignment the output of the C106 "OR" circuit will provide CFPHT timing over the full detector signal range from -50mV to -5 volts.

*General Radio Corporation

6. CIRCUIT DESCRIPTION

The 453 circuit will be described with reference to the schematic diagram 453-0101-S1 and the block diagram 453-0101-B1. For the general principles of operation refer to Section 4.

6.1 Input Stages

The bridging input consists of BNC connectors CN1 and CN2 shorted together behind the front panel. These connectors drive a direct coupled input impedance of approximately 1000 ohms. It is intended that connector CN2 be used to terminate the input signal cable in 50 ohms, using either a 50 ohm terminator or a 50 ohm coaxial cable terminated in 50 ohms. Diodes D1 to D7 form a high impedance voltage limiter to restrict the voltage presented to the input buffer amplifier to approximately +700mV and -2000mV. Compensation for zeroing the offset introduced by the base current of Q1 is provided through adjustment of R5.

Transistors Q1 to Q4 form the input buffer amplifier with a high input impedance and a low output impedance. The gain of this stage is approximately +1. The inverting amplifier consists of transistors Q5 to Q8. Resistors R20 and R19 provide for a gain of -2 at the emitter of Q8. The series 51.1 ohm resistor in the External Shaping Delay Output causes the gain at this output, referred to the bridging input, to be approximately -1. The external shaping delay output (CN3) should always drive a 50 ohm load to prevent oscillations. When a 50 ohm external shaping delay is connected between CN3 and CN7, this loading is provided automatically. The output of the inverter amplifier is dc-coupled and has approximately zero output offset. The delayed output from the inverter amplifier is normally connected to the summing buffer input (CN7).

The output of the input buffer amplifier is also fed to the fraction *f* switch, S1, through cable DL3. This switch consists of 50 ohm input impedance T attenuators. In the $f = 0$ setting, two 51 ohm resistors terminate both DL3 and DL4 such that the signal is not passed through the switch. This switch position is used for the leading edge trigger mode. In the $f = 0.5$ setting, the 51.1 ohm series termination at the input buffer amplifier output provides an attenuation of 0.5 for the signal. The output of the fraction switch drives a second input to the summing buffer through cable DL4.

Transistors Q46 to Q51 form the summing buffer and monitor output. This circuit consists of two identical dc-coupled, cascaded, common base stage. Q46 and Q47 provide the input buffer for the cross-over tunnel diode D18, and Q50 and Q51 form the buffer for the monitor output. In both cases the dc input and output offsets are approximately zero. Base-emitter junction offset compensation is achieved with transistors Q48 and Q49. The emitter input impedances to Q47 and Q50 are both approximately 2.5 ohms. Diodes D23 to D26 protect these inputs and hold the input impedance to the summing buffer approximately constant when overloading input pulses are applied ($>\pm$700mV). Resistor R111 in parallel with R113 (R110 in parallel with R114) yields an input termination for DL2 (DL4) of 50 ohms. Approximately 80% of the input signal from DL2 (DL4) is fed to the cross-over discriminator buffer through resistor R111 (R110), while the remaining 20% is driven into the monitor output buffer through R113 (R114). The low input impedances to Q47 and Q50 provide linear summing points for the signals from DL2 and DL4. It is at this point in the circuit that the constant fraction zero-crossing pulse shape is formed. The output of the monitor buffer (collector of Q51) is a 50 ohm coaxial cable with its input shunt terminated in 51 ohms. The shunt terminator permits the monitor output to be left unterminated when not used. However, the output must be driven into a 50 ohm terminated coaxial cable when observation of the monitor pulse shape is desired. The signals at the monitor output exhibit an attenuation of $\approx$0.075 referred to the bridging input.

The input buffer amplifier output is buffered from the lower level discriminator tunnel diode by the compensated pair of transistors Q9 and Q10. Q9 is an emitter follower driving the common base stage Q10 through 196 ohms. Q11 provides a temperature compensating sink for the bias current in Q10.

The lower level discriminator tunnel diode D13 is temperature stabilized by the Klixon oven at about 80°C. This oven draws substantial current from the +24 volt line ($\approx$200mA) for the first minute after turn on. After about three minutes the operating temperature is reached, and the current demand drops to approximately 20mA. At least 15 minutes should be allowed after turn on before using the module, to allow the lower level discriminator to stabilize.

The lower level bias control consists of transistors Q12 to Q16. This is a voltage follower amplifier which holds the potential across R43 equal to the value provided by the front panel lower level discriminator potentiometer. The field effect transistor Q12 linearly converts this voltage to a current driven into tunnel diode D13. The current is variable over a range of approximately 5mA. Resistor R51 allows the bias of D13 to be adjusted for calibration of the lower level discriminator control.

Q17 and Q18 form the current gate for the cross-over discriminator. When D13 is in the reset state (low voltage state) Q17 is conducting and Q18 is off. The 13mA current from the collector of Q17 back biases crossover discriminator D18, preventing it from triggering. When the lower level discriminator triggers, D13 switches to the high voltage state and turns off Q17. Q18 now conducts the 13mA. This action releases the gating current from D18 and allows it to fire. Internal delays are arranged so that the gating current is turned off just after the zero-crossing signal at D18 has begun to swing negative. If D18 has been biased to trigger at the zero input baseline, the negative phase of the input signal prevents D18 from firing. As the zero-crossing signal returns to the baseline and begins to go positive, D18 flips to the high voltage state to produce a timing output.

6.2 Internal Reset Mode

In the internal reset mode the base of Q21 sits at +1.0 volts. Transistor Q30 is turned off, and the external reset input is disconnected and terminated in 50 ohms.

Q19 is an emitter follower providing fan-out drive for Q25 and Q20. The offset voltage of Q19 is compensated by Q22 for the switching pair Q20 and Q21.

When D18 is in the low voltage stage, Q20 conducts and Q21 is turned off. As the crossover tunnel diode flips to its high voltage state, Q20 is turned off and Q21 begins to conduct. Transistors Q23 and Q24 constitute a constant current source. The output current is fed to the emitter of Q21. This current is adjusted by R77 to be $\approx$125μA less than that required to reset lower level tunnel diode D13 when the input pulse height to the 453 is exactly equal to the lower level discriminator setting. This adjustment forces the lower level tunnel diode to reset when the input pulse has fallen approximately 25mV below the lower level discriminator setting. Once D13 is reset, Q17 turns on and resets D18, causing Q21 to be turned off. The propagation delay around this reset loop is $\approx$12 nsec. Consequently, the lower level discriminator dead time is about 24 nsec.

6.3 External Reset Mode

In the external reset mode the external reset input is connected to the protected input of the switching pair Q28 and Q29. The diode protection circuit is similar to the one on the bridging input. The external reset switch also raises the bias at the emitter of Q22 to +1.5 volts, and increases the current to Q20 and Q21 by 3.7mA.

Now when D18 is in its high voltage state, Q21 is still not turned on. In the quiescent state, Q29 is on and Q28 is turned off. A negative signal on the external reset input turns Q29 off, switching all its current through Q28 to the load on the base of Q22. This action pulls down the base of Q21 and switches the current from Q20 into D13. The lower level tunnel diode resets, and is held reset for the duration of the external reset input pulse. As before, the resetting of D13 causes D18 to reset.

6.4 Output Stages

Transistors Q25 and Q26 form a buffering current switch to drive the timing outputs. Q25 is conducting in the quiescent state and Q26 is turned off. Q27 compensates for the offset voltage of Q19.

When the crossover tunnel diode triggers, Q25 turns off, switching its current into Q26. A negative pulse is produced on the load consisting of R22 and DL5. Shorted delay line DL5 clips this signal to a width of about 5 nsec. The clipped signal operates the negative output drivers through emitter follower buffers Q35 and Q39. Both negative outputs are identical and will be described with reference to Q36 to Q38. Transistor Q38 compensates for the voltage offset in Q35. Q36 is normally conducting $\approx$16mA, with Q37 turned off. The negative pulse from Q35 turns off Q36, switching the 16mA current through Q37 into the 50 ohm output load. Due to the clipping line, the output pulse is $\approx$5nsec wide independent of the pulse width at the bridging input. If the output (CN8) is not loaded with 50 ohms, the 16mA is drawn from the emitter of Q38 through the base-emitter junction of Q37.

Q31 and Q32 form a common base amplifier followed by an emitter-follower. When Q26 turns on, a positive 5 volt signal is generated at the emitter of Q32. This signal is differentiated by C35 and R93 plus R94, and used to trigger the positive output flip-flop (Q43 and Q44). Emitter follower Q45 drives the flip-flop output into the connector CN5. A positive 5 volt, 500 nsec wide, dc-coupled pulse is produced.

6.5 Overrange Reset

The pulse at the emitter of Q32 stays in the high voltage state as long as D18 remains in its high state. During this interval, diode D19 is back-biased, and capacitor C26 charges with the base current of Q33 and the leakage current of D19. If D18 is not otherwise reset before 40μsec, the voltage on the base of Q33 charges to +2.8 volts. At this point the current flowing in Q33 is switched into Q34, causing Q30 to turn on hard. The emitter of Q22 is clamped to ground, and Q21 is forced to turn on. The current from Q21 resets D13 which, in turn, causes D18 to reset. As D18 returns to its low voltage state, Q25 turns on and Q26 is turned off. The voltage at the base of Q32 returns to ground, forcing capacitor C26 to rapidly discharge through the emitter of Q32 and diode D19. Q33 consequently turns on, causing Q30 to turn off. Hence the reset current from Q21 is shut off, leaving both tunnel diodes in the low voltage state, ready to accept another input.

Under normal conditions, D13 and D18 are reset well before 40μsec, either by the internal hysteresis reset or by an external reset input. In this case, C26 is discharged by Q32 as D18 is reset. As a result, C26 never charges to a high enough voltage to turn Q33 off and trigger the overrange reset.

The overrange reset circuit can be disabled by removing Q34 from its socket.

6.6 Leading Edge Timing Mode

In the leading edge timing mode the fraction switch is set to zero, and both the input and output for the external shaping delay are terminated in 50 ohms. This procedure disconnects all inputs from the summing buffer. The walk adjust control is turned to the full counter-clockwise position to ensure that the cross-over tunnel diode (D18) flips to the high state as soon as the lower level tunnel diode (D13) triggers on the leading edge of the input pulse. The remainder of the circuit functions in the normal manner.

6.7 Cross-Over Pickoff Mode

In the zero-crossing timing mode a bipolar input signal is provided at the bridging input with the negative phase leading. Both the input and output for the external shaping delay are terminated in 50 ohms to disconnect the inverter amplifier output from the summing buffer. The fraction switch is set at $f = 0.5$ in order to pass the zero-crossing input signal (with minimum attenuation) through the summing buffer to the cross-over tunnel diode.

As in the CFPHT mode, the lower level discriminator fires on the leading edge of the input signal and releases the cross-over discriminator to trigger on the zero-crossing point. The remainder of the circuit function is identical to the CFPHT mode.

7. MAINTENANCE

7.1 Factory Repair Service

The 453 may be returned to ORTEC for repair service at a nominal cost. The standard procedure requires that each repaired instrument receive the same extensive quality control tests that a new instrument receives. Please contact the factory for instructions before shipping the unit.

7.2 General Maintenance

The 453 should require no regular maintenance work other than replacing components which have failed due to age. When components are changed in either the input limiter or the input buffer amplifier, the input offset should be adjusted to zero according to Section 7.3. If components are changed in the input limiter, the input buffer amplifier, the inverter amplifier, or any of the circuitry associated with the lower level discriminator, the lower level calibration procedure in Section 7.4 should be followed.

In the case of replacement of D13, adhere to the mounting schematic on the left of drawing 453-0101-S1 carefully. Use heat sinks on the tunnel diode leads when soldering to protect the diode against overheating.

DC voltages have been marked on the 453 circuit diagram to aid in identifying a malfunctioning component. The values in brackets are for the INT/EXT reset switch in the external mode.

7.3 Input Offset Adjustment

Potentiometer R5 is used to zero the dc offset on the bridging input. R5 can be found on the circuit board near the lower level discriminator potentiometer at the front of the module. Tune R5 according to the following steps.

1. Allow approximately 15 minutes warmup time after the power has been applied to the module. Check that the ±24V and ±12V supply lines on the bin are within ±0.5% of their nominal values.

2. Terminate the following connectors in 50 ohms:
   (a) one of the bridging inputs
   (b) the external shaping delay input
   (c) the external shaping delay output

3. Observe the offset on the bridging input with a voltmeter.

4. Adjust the offset to zero mV (within ±1 mV) with potentiometer R5.

7.4 Lower Level Discriminator Adjustments

This procedure should be followed whenever any components have been changed such that the lower level discriminator calibration could be affected (see Section 7.2).

1. The lower level discriminator tunnel diode is oven stabilized. For this reason, at least 30 minutes warmup time should be allowed after applying power before proceeding beyond step 12.

2. Connect a pulse generator to the 453 bridging input with 50 ohm coaxial cable. The pulser should be capable of generating a fast rise time pulse on 50 ohms with no overshoot. A rise time less than 10 nsec is preferable.

3. Terminate the second bridging input connector in 50 ohms.

4. Set the fraction switch to $f = 0$.

5. Terminate the external shaping delay input and output separately in 50 ohms.

6. Set the EXT/INT reset switch to external.

7. Turn the lower level hysteresis adjustment, R77, (top of module) to the full clockwise position.

8. Turn the walk adjust control (front panel) to the full counter-clockwise position.

9. Set the lower level discriminator control (front panel) to 50mV.

10. Select a negative polarity 50mV pulse from the pulse generator. Ensure that the pulser output has a zero dc offset ($<\pm$1mV). The pulser output preferably should be a square wave with a width of about 100 nsec.

11. Connect one of the 453 negative outputs to a fast oscilloscope (preferably a sampling oscilloscope) using a properly terminated 50 ohm cable.

12. Ensure that the condition in step 1 has been fulfilled.

13. Adjust the lower level zero adjust, R51, (bottom of module) until the 453 negative output just appears on the oscilloscope (50% triggering probability). This calibrates the lower level discriminator setting.

14. Set the reset switch to INT (internal) and remove Q34 from its socket (top rear of module).

15. Set the lower level discriminator control to 25mV (minimum setting).

16. Adjust the lower level reset hysteresis, R77, (top of module) to the full counter-clockwise position. Slowly turn the potentiometer in the clockwise direction until the 453 output is just reliably triggered. This sets the hysteresis reset threshold to $\approx$25mV.

17. Replace Q34 in its socket and set the lower level discriminator control to 50mV. Repeat step 13.

18. Replace the side covers on the module, making sure that the foam cushion contacts Q34 to hold it in place.

REFERENCES

1. D. A. Gedcke and W. J. McDonald, Nuclear Instruments and Methods 55(2): 377 (1967).

2. D. A. Gedcke and W. J. McDonald, Nucl. Instr. & Meth. 58(2): 253 (1968).

3. W. J. McDonald and D. A. Gedcke, Electronics for Fast Neutron Work, International Symposium on Nuclear Electronics, Versailles, September 1968.

4. R. L. Chase, Rev. Sci. Instr. 39, #9:1318 (1968).

5. T. D. Douglass and C. W. Williams, IEEE Trans. Nucl. Sci. NS-16, #1:87 (1968).

6. I. S. Sherman, R. G. Roddick, and A. J. Metz, IEEE Trans. Nucl. Sci. NS-15, #3:500 (1968).

7. D. A. Gedcke and C. W. Williams, High Resolution Time Spectroscopy: I. Scintillation Detectors, ORTEC Publication (August 1968), copies available from ORTEC upon request.

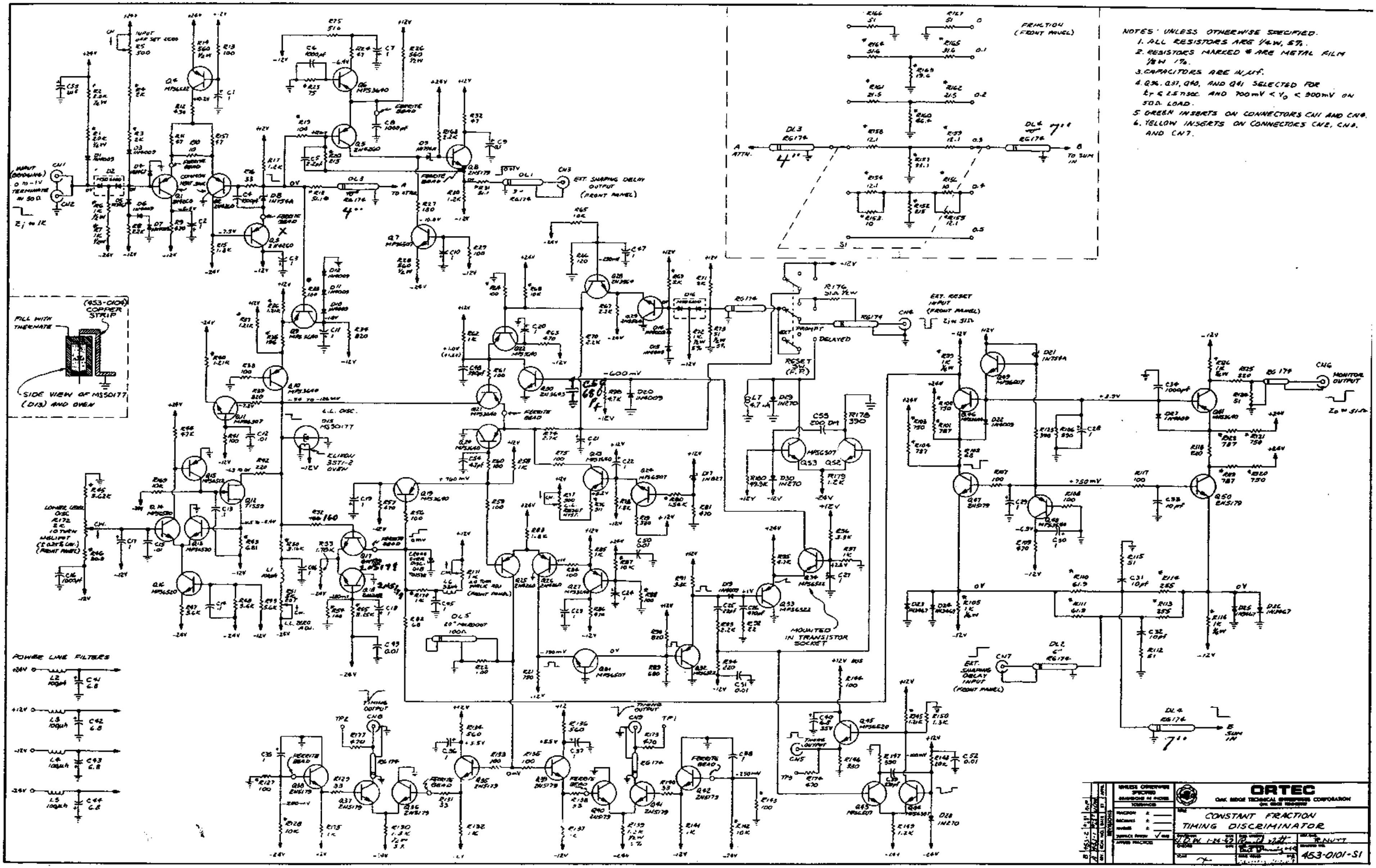
8. R. Nutt, D. A. Gedcke, T. D. Douglass, and C. W. Williams, High Resolution Time Spectroscopy: II: Ge(Li) Detectors, ORTEC Publications (1969), copies available from ORTEC upon request.

BIN/MODULE CONNECTOR PIN ASSIGNMENTS
FOR AEC STANDARD NUCLEAR INSTRUMENT MODULES
PER TID-20893

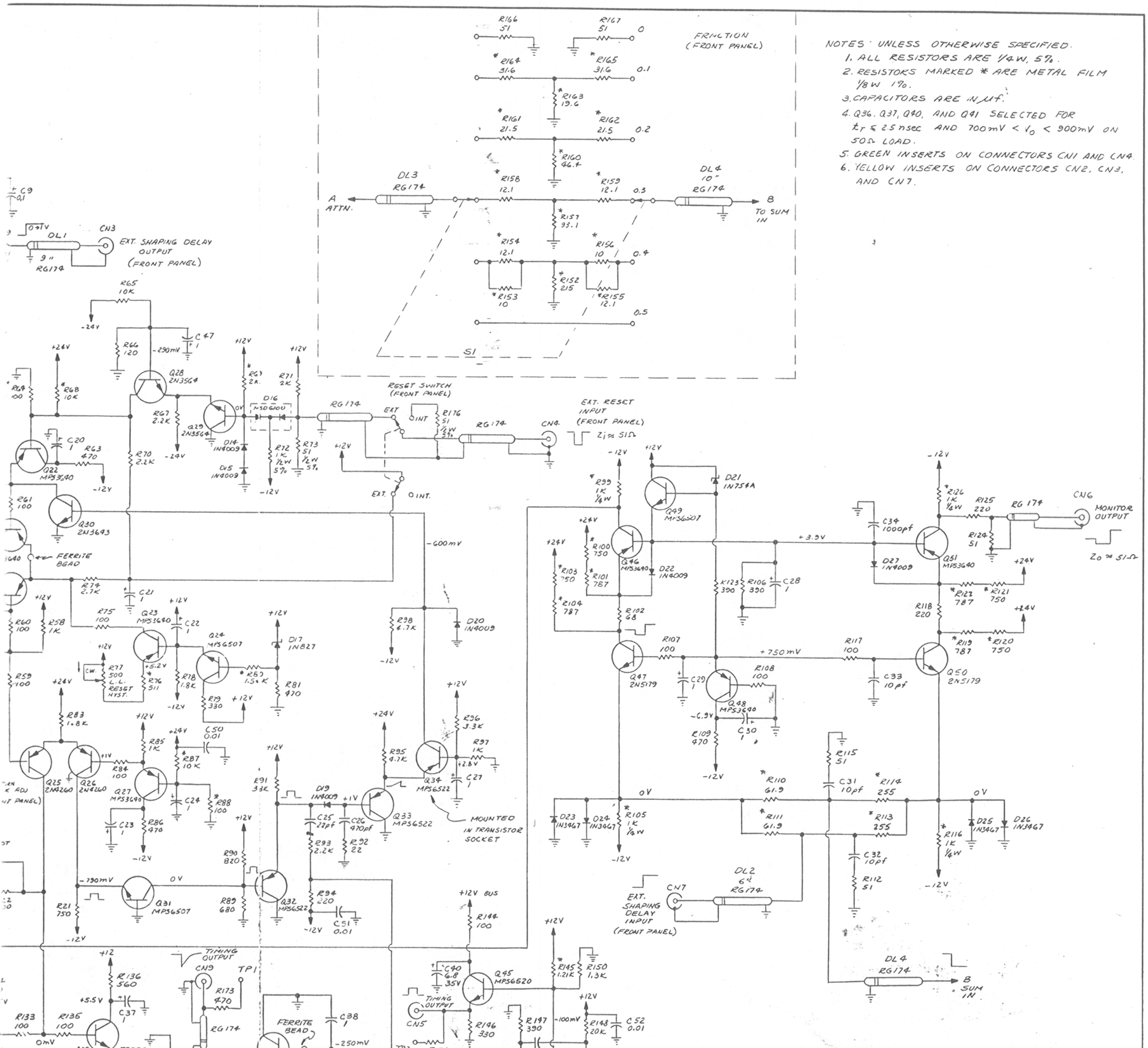
Pin	Function	Pin	Function
1	+3 volts	23	Reserved
2	- 3 volts	24	Reserved
3	Spare Bus	25	Reserved
4	Reserved Bus	26	Spare
5	Coaxial	27	Spare
6	Coaxial	*28	+24 volts
7	Coaxial	*29	- 24 volts
8	200 volts dc	30	Spare Bus
9	Spare	31	Carry No. 2
*10	+6 volts	32	Spare
*11	- 6 volts	*33	115 volts ac (Hot)
12	Reserved Bus	*34	Power Return Ground
13	Carry No. 1	35	Reset
14	Spare	36	Gate
15	Reserved	37	Spare
*16	+12 volts	38	Coaxial
*17	- 12 volts	39	Coaxial
18	Spare Bus	40	Coaxial
19	Reserved Bus	*41	115 volts ac (Neut.)
20	Spare	*42	High Quality Ground
21	Spare	G	Ground Guide Pin
22	Reserved		

**These pins are installed and wired in parallel in the ORTEC 401A Modular System Bin.*

The transistor types installed in your instrument may differ from those shown in the schematic diagram. In such cases, necessary replacements can be made with either the type shown in the diagram or the type actually used in the instrument.



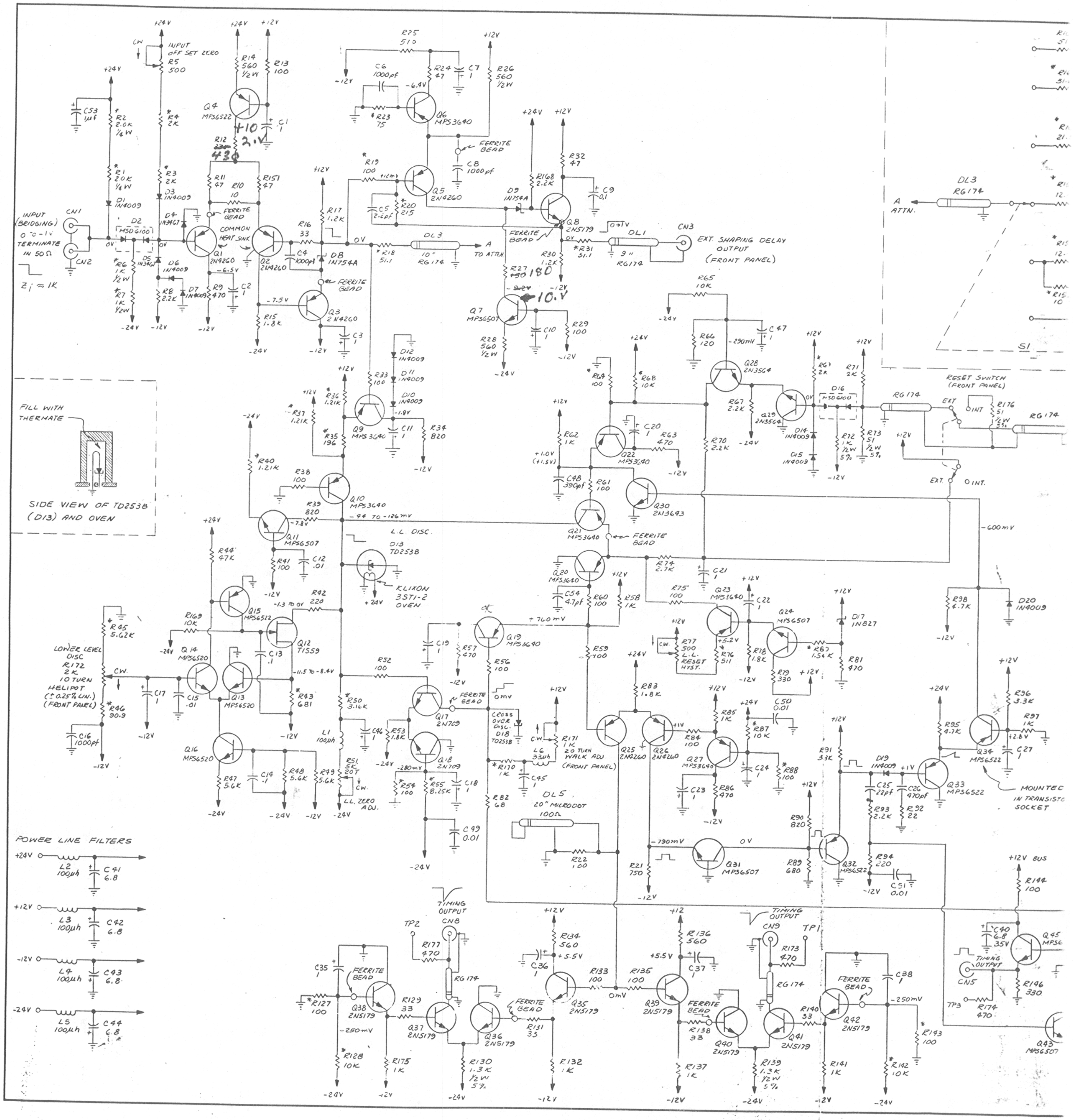
NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTORS ARE 1/4W, 5%.
2. RESISTORS MARKED * ARE METAL FILM 1/8W 1%.
3. CAPACITORS ARE IN µf.
4. Q36, Q37, Q40, AND Q41 SELECTED FOR tT ≤ 2.5 nsec. AND 700mV < VO < 900mV ON 50Ω LOAD.
5. GREEN INSERTS ON CONNECTORS CN1 AND CN4.
6. YELLOW INSERTS ON CONNECTORS CN2, CN3, AND CN7.
POWER LINE FILTERS
ORTEC
OAK RIDGE TECHNICAL ENGINEERS CORPORATION
CONSTANT FRACTION TIMING DISCRIMINATOR
453-0101-S1



NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL RESISTORS ARE 1/4 W, 5%.
2. RESISTORS MARKED * ARE METAL FILM 1/8 W 1%.
3. CAPACITORS ARE IN μf.
4. Q36, Q37, Q40, AND Q41 SELECTED FOR $t_r \leq 2.5$ nsec AND 700 mV < V_o < 900 mV ON 50Ω LOAD.
5. GREEN INSERTS ON CONNECTORS CN1 AND CN4.
6. YELLOW INSERTS ON CONNECTORS CN2, CN3, AND CN7.

UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES TOLERANCES	ORTEC OAK RIDGE TECHNICAL ENTERPRISES CORPORATION OAK RIDGE TENNESSEE
FRACTION ± / DECIMALS ± / ANGLES ± / SURFACE FINISH √ RMS / APPLIED PRACTICES	TITLE CONSTANT FRACTION TIMING DISCRIMINATOR
DRAFTSMAN J.D.W. DATE 1-24-69	RESP. ENG. D. Gedcke
SCALE	DRAWING NO. 453-0101-S1



INPUT OFF SET ZERO
R5 500
Q4 MPS6522
INPUT (BRIDGING) 0 TO -1V TERMINATE IN 50Ω
CN1
CN2
Zi ≈ 1K
COMMON HEAT SINK
FERRITE BEAD
Q1 2N4260
Q2 2N4260
Q3 2N4260
D8 1N754A
Q5 2N4260
Q6 MPS3640
C6 1000pf
C8 1000pf
D9 1N754A
Q8 2N5179
DL1 9" RG174
CN3
EXT. SHAPING DELAY OUTPUT (FRONT PANEL)
DL3 10" RG174
A TO ATTN.
Q7 MPS6507
DL3 RG174
A ATTN.
S1
RESET SWITCH (FRONT PANEL)
EXT.
INT.
FILL WITH THERMATE
SIDE VIEW OF TD253B (D13) AND OVEN
Q9 MPS3640
Q10 MPS3640
Q11 MPS6507
L.L DISC.
D13 TD253B
KLIXON 3ST1-2 OVEN
Q15 MPS6522
Q12 TIS59
Q14 MPS6520
Q13 MPS6520
Q16 MPS6520
LOWER LEVEL DISC R172 2K 10 TURN HELIPOT (± 0.25% LIN.) (FRONT PANEL)
L.L. ZERO ADJ.
R51 5K 20T
Q17 2N709
Q18 2N709
Q19 MPS3640
CROSS OVER DISC. D18 TD251B
R171 1K 20 TURN WALK ADJ (FRONT PANEL)
L6 33µh
DL5 20" MICRODOT 100Ω
Q20 MPS3640
Q21 MPS3640
Q22 MPS3640
Q30 2N3643
Q28 2N3564
Q29 2N3564
D16 HSCH100
Q23 MPS3640
R77 500 L.L. RESET HYST.
Q24 MPS6507
D17 1N827
Q25 2N4260
Q26 2N4260
Q27 MPS3640
Q31 MPS6507
Q32 MPS6522
Q33 MPS6522
Q34 MPS6522
D19 1N4009
D20 1N4009
MOUNTED IN TRANSISTOR SOCKET
POWER LINE FILTERS
+24V L2 100µh C41 6.8
+12V L3 100µh C42 6.8
-12V L4 100µh C43 6.8
-24V L5 100µh C44 6.8
TIMING OUTPUT CN8
TP2
RG 174
Q38 2N5179
Q37 2N5179
Q36 2N5179
Q35 2N5179
Q39 2N5179
Q40 2N5179
Q41 2N5179
Q42 2N5179
TIMING OUTPUT CN9
TP1
+12V BUS
TIMING OUTPUT CN5
TP3
Q43 MPS6507