CAMAC MODEL 2259B

ANALOG-TO-DIGITAL CONVERTER

WARRANTY

LeCROY RESEARCH SYSTEMS CORP. warrants each instrument it manufactures to be free from defects in material and workmanship under normal use and service for the period of 1-year from date of purchase. Custom monolithics and hybrids sold separately and all spare or replacement parts are warranted for 90-days. This warranty extends only to the original purchaser. This warranty shall not apply to fuses, disposable batteries or any product or parts which have been subject to misuse, neglect, accident or abnormal conditions of operations.

In the event of failure of a product covered by this warranty, LeCroy will repair and calibrate an instrument returned to the factory or an authorized service facility within 1 year of the original purchase; provided the warrantor's examination discloses to its satisfaction that the product was defective. The warrantor may, at its option, replace the product in lieu of repair. With regard to any instrument returned within one year of the original purchase, said repairs or replacement will be made without charge. If the failure has been caused by misuse, neglect, accident or abnormal conditions or operations, repairs will be billed at a nominal cost. In such case, an estimate will be submitted before work is started, if requested.

The foregoing warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness or adequacy for any particular purpose or use. LeCroy Research Systems Corp., shall not be liable for any special, incidental or consequential damages, whether in contract, tort or otherwise.

IF ANY FAILURE OCCURS, notify LeCroy Research Systems Corp., or the nearest service facility, giving full details of the difficulty, and include the Model number, serial number, and FAN (Final Assembly Number) or ECO (Engineering Change Order) number. On receipt of this information, service data or shipping instructions will be forwarded to you. On receipt of the shipping instructions, forward the instrument, transportation prepaid. A Return Authorization number will be given as part of shipping instructions. Marking this RA number on the outside of the package will insure that it goes directly to the proper department within LeCroy. Repairs will be made at the service facility and the instrument returned, transportation prepaid.

ALL SHIPMENTS OF LECROY INSTRUMENTS FOR REPAIR OR ADJUSTMENT should be made via Air Freight or "Best Way" prepaid. The instrument should be shipped in the original packing carton; or if it is not available, use any suitable container that is rigid and of adequate size. If a substitute container is used, the instrument should be wrapped in paper and surrounded with at least four inches of excelsior or similar shock-absorbing material.

ATTENTION

CRATE POWER SHOULD BE TURNED OFF DURING INSERTION AND REMOVAL OF UNIT TO AVOID POSSIBLE DAMAGE CAUSED BY MOMENTARY MISALIGNMENT OF CONTACTS.

SEE POCKET IN BACK OF MANUAL FOR SCHEMATICS, PARTS LISTS AND ADDITIONAL ADDENDA WITH ANY CHANGES TO MANUAL.

WHEN CURRENT IS APPLIED TO THE 2259B (SUCH AS WOULD OCCUR WHEN PLUGGING A MODULE IN AND TURNING THE CRATE POWER SUPPLY ON), THE STATES OF THE LAM LATCH AND LAM ENABLE ARE ARBITRARY. THE UNIT MUST ALWAYS BE INITIALIZED WITH AN F(24) (DISABLE LAM) OR AN F(26) (ENABLE LAM) AND AN F(10) (CLEAR LAM).

ATTENTION

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TECHNICAL DATA

LeCroy

CAMAC Model 2259B

12-Channel, 11-Bit Peak-Sensing Analog-to-Digital Converter

For:
• Liquid argon ionization chambers
• NaI pulses
• BGO pulses
• Linear multiwire proportional chambers
• General peak-sensing applications

The Model 2259B 12-Channel CAMAC ADC is based on the design of the widely used Model 2259A. Digital sections are identical, utilizing the same synchronized oscillator circuit and low-power LeCroy Model SC100 Hybrid scaler section, directly interchangeable in either ADC. The analog front end of the 2259B employs the LeCroy Model VT100C Voltage-to-Time Converter, offering superior linearity, stability and peak-sensing/holding over previous versions.

The Model 2259B accepts negative-going analog inputs up to − 2 V in amplitude within its linear dynamic range, giving an 11-bit digital output proportional to the peak of the pulse falling within an externally applied gate interval. The resultant ADC sensitivity is approximately − 1 mV/count. The analog input signal should have at least a 50 nsec risetime. Because of the nature of the peak detector, the Model 2259B is insensitive to the falltime of the input pulse. The minimum recommended gate duration is 100 nsec, and should enclose the negative peak of the input pulse. Gate widths up to 5 μsec may be employed. Digitizing time of the 2259B is fixed at approximately 106 μsec.

In common with all new LeCroy CAMAC data acquisition modules, the 2259B offers a fast clear input (< 2 μsec total clearing time) to permit fast rejection of unwanted data before, during, or after conversion is complete, eliminating the need for long analog delays. In addition, a front panel test feature permits on-line testing of the entire ADC circuit. When F25 is applied, the 2259B generates an internal 100 nsec gate at S2 time. If the CAMAC I is present, the front panel "Test" input will inject a signal with a proportionality constant of − 0.167 volt/volt into all inputs. If I is not present, the Test input is disabled; F25 will generate the internal gate at S2, but only the residual pedestal at the gate width will be measured.

The Model 2259B responds to the CAMAC Functions F0, F2, F8, F9, F10, F24, F25 and F26, and accepts or generates the following CAMAC commands: Z or C, I, Q, X, L. Packaging of the 2259B is a #1 width CAMAC module, conforming to IEEE Report 583. Current usage is low enough to permit the use of up to 23 2259B's (276 channels) in a single, standard, powered CAMAC crate.

December 1982

Innovators in Instrumentation

SECTION 1

SPECIFICATIONS

1.1   Introduction

The Model 2259B consists of 12 independent identical ADC's and associated circuitry. Referring to the 2259B Block Diagram in Figure 1.1, the 2259B circuitry is divided into 6 basic parts:

- Twelve VTC (voltage-to-time converter) channels (peak voltage).

- A gate, test, and pedestal driver circuit.

- Twelve clock synchronizers and scalers.

- A gated oscillator.

- A Q response and LAM suppress circuit.

- A CAMAC control section.

Separate descriptions of each of these circuit blocks follow.

1.2   Voltage-To-Time-Converter

Each of the 12 inputs employs a VT100D voltage-to-time converter (VTC). The VTC consists of a virtual ground input amplifier, a linear gate driving a stable integrating capacitor, a current source, and an output differential amplifier.

The virtual ground input is driven from the front panel input through a 576 Ω precision resistor (thus converting the input voltage to current) or from the common test input bus. The 576 Ω resistor is effectively paralleled (as seen from the input connector) with the 56.2 Ω precision resistor to ground to terminate the input cable to 50 Ω. Input clamp diodes are included at the hybrid input to provide input protection and reduce crosstalk on large overloads. A small current is added to the analog signal at the virtual ground input of the hybrid to force a slightly positive pedestal (intercept) for each hybrid.

The current from the virtual ground input is delivered to an internal resistor via the linear gate. The resulting voltage is transferred to a capacitor, which is subsequently "run up" by means of a stable current source after the trailing edge of the gate. Thus, the voltage across the integrating capacitor is returned to its quiescent value at a constant rate, the resulting time being proportional to the input voltage. This "run up" current is determined by the 1 M Ω resistor at pin 5 and the difference between +24 V and V_{REF} (which appears across it). The output comparator senses the voltage across this capacitor and generates an output level as long as this voltage is greater than a reference level (which is set by a resistive divider from

1.4   Clock Synchronizer and Scaler

The output of each VT100D hybrid in the Model 2259B is used to gate an oscillator into one half of LeCroy SC100 Dual Eleven-Bit Scaler (refer to Figure 1.3). The oscillator is synchronously started with respect to the leading edge of the gate (see section 1.5). This ensures no fractional pulses during the beginning of the run up cycle. The synchronizing stage also insures that each clock sync circuit (see schematic, sheet 2 and Figure 1.2) supplies an integral number of clock pulses even if the VTC output returns to its quiescent state in the middle of a clock pulse as shown in the diagram in Figure 1.3.

When the conversion cycle is complete, readout of a particular scaler is accomplished by enabling the proper SC100 (using decoded A2, A4, and A8 subaddress lines) and selecting the proper half of the SC100 (using the A1 subaddress). If this subaddress is accompanied by F(0) or F(2) and N, the 11-bit data will be gated out in parallel to the CAMAC dataway.

1.5   Gated Oscillator

The clock circuit is a modified Colpitts oscillator employing a highly temperature stable choke and a mica capacitor as resonant elements. Its frequency is 20 MHz. The oscillator is gated on 8 μsec after the leading edge of the gate pulse. Gating the oscillator in this way eliminates the uncertainty of one count associated with an asynchronous oscillator and eliminates noise and non-linearities caused by not delaying the turn-on (see Figure 1.4). The conversion time is set to 100 μsec. This allows for the $\pm$ 5% differences from channel to channel, slight temperature drifts, module to module variations, etc., and still ensures that an over-flow can occur for oversized input pulses.

1.6   LAM and Q-Response Suppress Circuit

At the beginning of the gate pulse, a monostable is set (see Figure 1.4). The RC time constant of this monostable is adjustable by a 20 K potentiometer. When the monostable resets, a latch is reset if one or more of the VT100D outputs is still on. If set, this latch disables the Q-response circuit (that normally indicates valid data on an F(0) or F(2) Read Command) and clears the LAM latch. The threshold of the suppress circuit may be set as high as 200 counts.

1.7   CAMAC Control

The decoding of the CAMAC "F" functions and N is performed by a 4 line to 16 line decoder (an SN74154). A DC level is generated at the appropriate pin for each valid CAMAC command. Scaler addressing is accomplished using a 4 line to 10 line decoder (an SN7442) on A2, A4, and A8, to enable the appropriate SC100 2 channel scaler hybrid and the A1 bit is used to select the appropriate half of the SC100. X-response is generated for all valid commands, and Q-response and LAM are generated as described in the Q and L Suppress Circuit section.
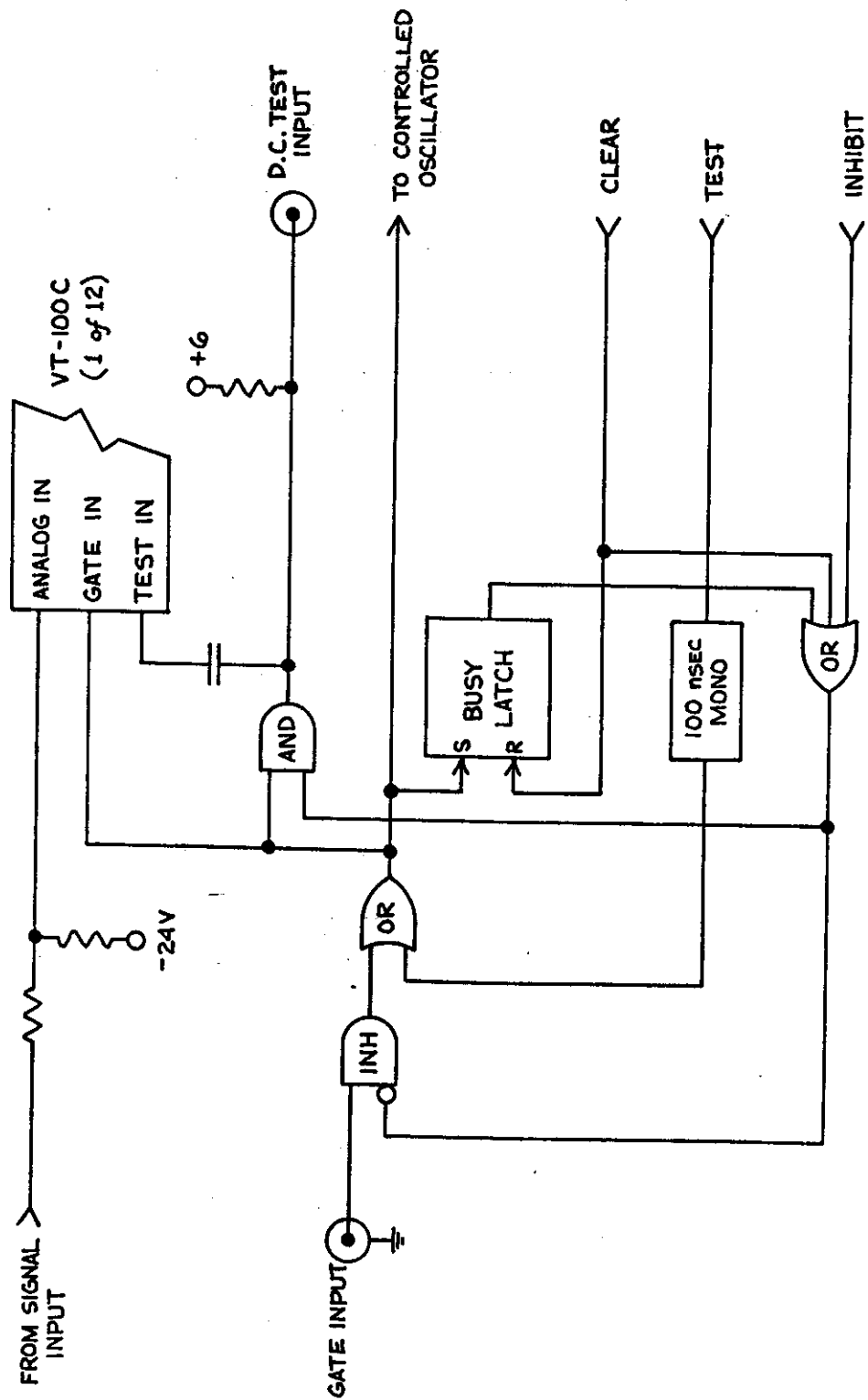
Figure 1.2

SECTION 2

OPERATIONAL DESCRIPTION

2.1   General

The LeCroy Model 2259B 12-channel ADC contains 12 complete 11-bit analog-to-digital converters in a single width CAMAC module. The analog-to-digital conversion is accomplished by the Wilkinson rundown method, which ultimately yields a digital output (in TTL negative logic binary format) which is proportional to the voltage peak of the input pulse. By the Wilkinson technique the input peak is used to generate a current (via a precision resistor) which in turn is gated and routed to a precision resistor. A capacitor is charged to this value and is then discharged at a constant rate. During the time the rundown is taking place, pulses from an oscillator are gated into a scaler, resulting in the final count proportional to the charge on the capacitor and thus to the input peak voltage.

2.2   Inputs

The 12 analog inputs of the 2259B are of 50 Ω impedance and accept negative-going pulses or levels only during an externally applied gating interval. To assure performance within the linear range of the 2259B, input signals should not have rise times faster than 50 nsec and should not exceed -2 V in amplitude. The actual peak voltage that yields a full scale digital output (normally 1980 counts) is -2 V.

The full scales of all 2259B modules are factory set to within 5% of each other.

GATE: The built in linear gate is common to all 12 analog inputs, which necessitates that analog-to-digital conversion for all channels is done in parallel. The 50 Ω input impedance accepts pulses of ≥ -600 mV in amplitude and of duration between 50 nsec and 5 µsec. The actual gate opening and closing times are approximately 2 nsec, and the gate should precede the analog inputs by 4 nsec.

IMPORTANT NOTE: The duration of the effective gate will exceed that of the gate pulse by 4 nsec.

The gate interval must enclose the negative peak of the analog input pulse. It must start at least 50 nsec before the peak, and for best linearity it should end within 50 nsec after the peak.

The 2259B gate is inhibited from the trailing edge of the gate until any CAMAC clear (C,Z,F(9) or F(2)·A(11)) or a front panel clear is applied. This effectively locks out spurious analog signals and noise from the ADC while the desired signal is being processed. The ADC's internal oscillator is synchronized with the leading edge of the gate pulse (although it occurs somewhat later), eliminating inaccuracies caused by the utilization of free running oscillators.

very little effect should occur. The pedestal value will change by < 2 counts per microsecond. A second effect is that the initial 7% of the conversion characteristic becomes slightly less linear (see Figure 2.1).

2.5 Conversion Time

The conversion time of the 2259B is 108 µsec for any input. With application of a Fast Clear, however, any conversion can be terminated and the front end ready to accept a new gate signal within 2 µsec.

2.6 Data and Readout

The output data of the 2259B is standard CAMAC-compatible (TTL negative logic) is 11-bit binary format. The 11-bit digital resolution (1 mV/count) matches the overall ADC accuracy of .05%. The 11 bits of digitized information are gated onto the R1 to R11 (2^0 to 2^{10}) Dataway bus lines by $F(0) \cdot N \cdot A$, where $F(0)$ signifies the read function, N signifies the 2259B to be read, and A (from A(0) to A(11)) signifies which ADC channel in the 2259B is to be read out. Generally, the unit is ready for readout when LAM appears. The function F(2) (Read and Clear) may also be used to read information. However, this readout is destructive when A(11) is addressed. The $F(2) \cdot N \cdot A(11)$ command will clear all channels. The F(2) command on addresses A(0) through A(10) will cause the ADC contents to be read with no clear and the input gate will remain disabled.

2.7 LAM

A LAM (Look-At-Me) signal is generated from end of conversion until a module Clear or Clear LAM (Z, C, F(9) or F(10)). LAM is disabled for the duration of N. LAM can be permanently enabled or disabled by the Enable F (26) or Disable F(24) function command, and can be tested by Test LAM F(8). LAM may be suppressed for empty modules as indicated in "Q and LAM Suppression" section below.

The test function F(8) allows the LAM to be tested. In response to application of $F(8) \cdot N \cdot A$ (where A is any A from A(0) to A(11)) independent of Disable LAM, a Q response will be generated if LAM is set. Although the LAM is disabled while the 2259B in question is being addressed (i.e., for the duration of N), once latched it will produce a Q response when an $F(8) \cdot N \cdot A$ is applied.

IMPORTANT:

> When current is applied to the 2259B (such as would occur when plugging a module in and turning the crate power supply on), the states of the LAM latch and LAM enable are arbitrary. The unit must always be initialized with an F(24) (Disable LAM) or an F(26) (Enable LAM) and an F(10) (Clear LAM).
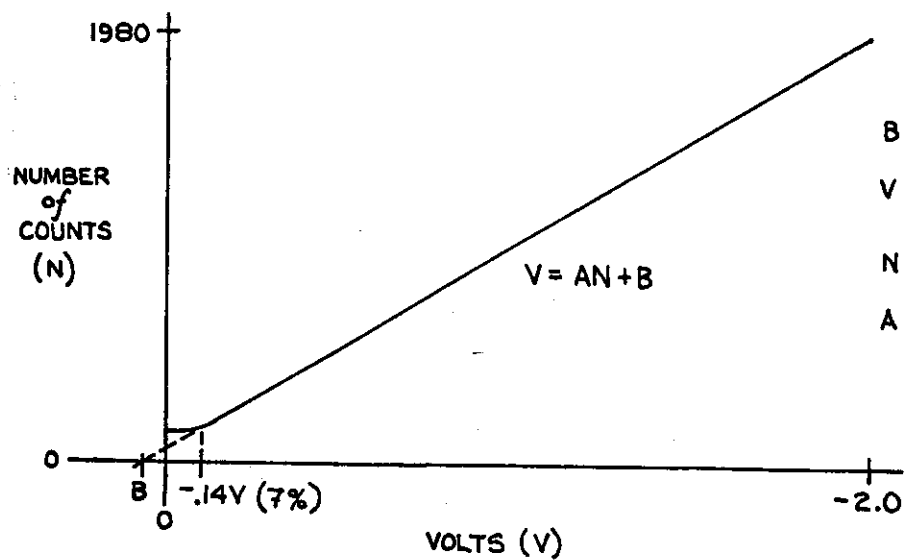
Figure 2.1

B IS AMOUNT OF PEDESTAL

V IS VOLTAGE PEAK APPLIED TO ADC
   ANALOG INPUTS

N IS TOTAL NUMBER OF COUNTS

A IS CONVERSION SLOPE
   I.E. $A = \dfrac{(V-B)}{N}$

$V = AN + B$