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CYCLOTRON LABORATORY

OVERVIEW OF THE DATA ACQUISITION SYSTEM AT NSCL

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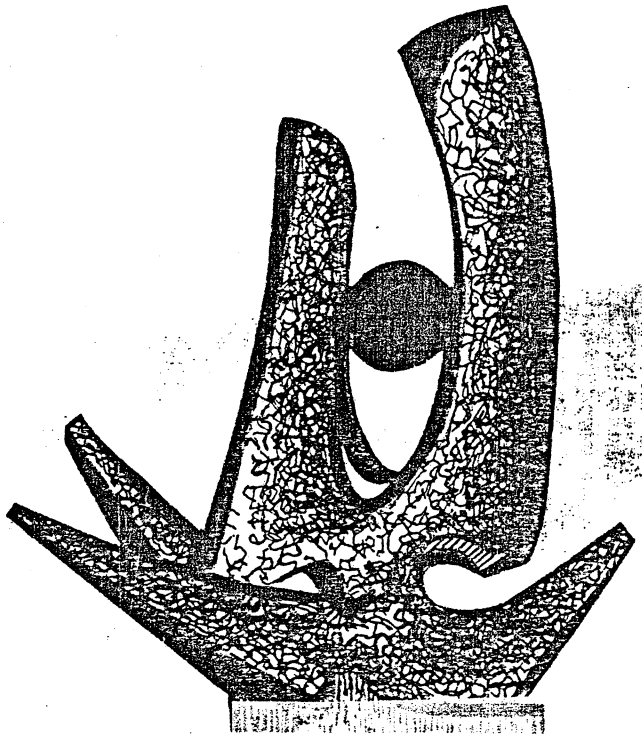

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OVERVIEW OF THE DATA ACQUISITION SYSTEM AT NSCL

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Abstract

The integrated data acquisition/analysis system for nuclear experiments is described. The selection criteria for the multi-processor system is discussed and the current configuration and planned expansion is shown. Operational rates and limitations of this system are given for some typical experiments. An overview of the multi-tasking software and user interfaces is given.

Introduction

This paper describes the data acquisition system as it currently exists at the National Superconducting Cyclotron Lab (NSCL). We will start by listing the requirements and objectives which dictated the choice of hardware and the software philosophy. We will then proceed with an examination of the hardware chosen showing how the system ties together and how we attempt to meet our objectives. We will then give data on the actual performance of the system as currently implemented, pointing out the strong points as well as the limitations, drawing on experiments that were recently performed at NSCL using this system. Finally, we present a discussion of the various expansion and improvement paths open as well as some preliminary indications of the directions we intend to follow.

Design Goals and Requirements

In designing a data acquisition system, as in designing any computer system, it is important to establish first a working set of performance goals and requirements. At NSCL, the performance goals of the data acquisition system must be designed meet the expected needs of the coupled cyclotron facility (phase II). Additionally, being an outside user facility, it is necessary for us to build a system which can

easily be tailored to meet the needs of users not necessarily familiar with our computing environment. The present facility (phase I) operation provides an excellent test of the system design concept and implementation.

The current phase I and the final phase II facilities are well documented elsewhere[1] and at this point it is only appropriate to summarize the experimental apparatus which is proposed for phase II. The phase II facility will consist of a coupled K-500 and K-800 superconducting heavy ion cyclotron system which will direct beam to any of the experimental areas shown in figure 1. Several devices in the planned phase II facility have a strong impact on the design of the data acquisition system e.g. the two dimensional focal plane detector for the S-800 spectrograph and the multiparticle 4π solid angle detector array.

We developed the following design goals and requirements[2]:

1. It is desirable to be able to accumulate data at rates on the order of 200,000 16 bit parameters per second.

2. It is important that the acquisition system be able to support the simultaneous accumulation of several 1-D and 2-D histograms.

3. It is necessary to be able to ship signals over the long distances between the experimental areas and the data acquisition computers in a noise-free manner.

4. It is important to be able to store the acquired data in a manner which is as compatible as possible with the equipment available to outside users.

5. The system should be easily tailorable to meet a wide variety of experimental needs.

6. The system should be able to accept, with minimal changes, codes developed by outside users on their own equipment.

7. Hardware and software should be commercially available whenever possible.

8. The system should support both the group using the cyclotron as well as a group setting up for subsequent cyclotron use.

9. The system should be organized around a 32 bit architecture to allow the accumulation of a large number of counts in a spectrum channel without overflow or the use of multiple precision arithmetic.

10. The machine should support virtual memory so that programs may be used which require the full addressing space on machines without a full physical complement of memory.

11. Some form of network or other interprocessor data link must be available.

12. All CPU's should be of the same or substantially similar types in order to facilitate the exchange of programs between machines and to allow failing machines to be quickly spared.

13. Extended precision/range floating point capabilities must be available to allow the importation of computational programs from outside the facility.

It was clear from the event rate requirements and the spectrum size requirements that a single computer system would not meet performance objectives since typically computers with virtual addressing spaces large enough to fulfill requirement 2 are equipped with operating systems and interrupt structures which react too slowly to external events to allow the desired event rates to be maintained. We therefore decided on a two tiered distributed system with a front end microprocessor which collects events into relatively large buffers for shipment back to a larger supermini or mainframe computer. We also decided that the actual data acquisition hardware would, until FASTBUS becomes a commercially viable option, reside in one or more CAMAC[3] crates, and that the microprocessor front end should reside in the crate as well.

To meet the requirement that we be able to push noise immune signals around over long distances at high speed, it was decided that the interface between the CAMAC crates and the mainframe computer should allow the crates themselves to be located at a great distance from the mainframe. This gave us a choice between the CAMAC parallel highway[4], and the CAMAC serial highway[5]. In the end we chose to use the serial highway run at 2Mhz in byte mode since this allowed communications at the speeds required while not sacrificing drive distance. Additionally, the relatively few number of wires in the serial interface were deemed a considerable advantage when planning long highway runs.

The remaining design goals determined the selection of the computers, as well as the medium on which event data would be stored. In order to facilitate the transportation of event data to other facilities, we selected magnetic tape as the primary event storage medium making 800, 1600, and 6250 bpi densities at 125 ips. available. For the supermini/mainframe computer we chose DEC VAX 11/750 minicomputers. Since experiments which would require several

megabytes of spectra to be accumulated can easily be foreseen, the large virtual address space of the VAX makes it ideal. Additionally, VMS with its English like command language offers an operating system easy for novice users to learn. The ability to create loosely coupled cooperating processes offered by VMS allows one to cleanly isolate the experiment dependent portion of the data acquisition system from the experiment independent part. Finally, since a large part of the nuclear physics community already uses either DEC PDP-11's or VAX's, we felt that the VAX would offer the minimum acclimatization time to outside users.

For the front end microcomputer, we chose to use DEC LSI-11/23's. The software for the 11/23 can be easily developed on the VAX and then down loaded over the serial highway to the target crates. The operating system in the 11/23 is a custom built low overhead event driven multitasking memory based executive. The system supports some basic synchronization primitives and a pipelined interprocess communication scheme as well as timer directives. I/O is supported via device primitive macros and with device allocation and deallocation macros. Programs running under this system are somewhat protected from each other, but overlapping data areas and mapping processes to the executive reduces the context switching overhead to a minimum.

The LSI-11 is connected to two CAMAC crates with differing attributes. One crate is mapped directly into the I/O page of the LSI-11 allowing it to read one or more data items quickly. The second crate is accessed through a DMA controller which allows one to set up and read block mode devices, such as the LeCroy PCOS Databus interface[6], quickly. This second crate also is interfaced via an L-2 type controller to the VAX controlled CAMAC serial highway. This allows the LSI-11 to set serial graded LAM's which the VAX can detect. Another CAMAC module allows the VAX DMA access to the LSI-11 memory which provides the mechanism by which data acquired and buffered in the LSI-11 are transferred back to the VAX for taping and sorting. To allow quick replacement of failing hardware, the VAX acquisition computers are connected to the serial highways running to the experimental areas through a patch panel.

We purchased four VAX 11/750 minicomputers for data acquisition, analysis, and program development. The systems are roughly configured as shown in fig. 2. We also purchased a VAX 11/780 for use in large scale analysis and general computation. One machine, the analysis computer is reserved for offline data reduction and analysis and will not be discussed here. A second machine is used for program development and test and is available for system development and test, detector tests, and electronics test. It also may be used for data analysis with the understanding that service can be interrupted without notice. The final two computers

are configured for data acquisition as shown in figure 3. Each machine is assigned to an experimental group, one of these is currently using the cyclotron, while the other group is scheduled to use it next and is doing set up and debugging work. Obviously, the set up and debug group can share the machine with other users.

With such a large number of systems, it is important to be able to exchange files between machines in a relatively transparent manner. Originally, we intended to use DECNET for this communications task, but recent developments in software and hardware which will allow VAX's to share peripherals have forced us to reevaluate this decision. We now intend to install the recently announced VAX cluster as an interconnect between all of the VAX 11/750's and the VAX 11/780. This would allow disk and tape storage units to be shared between all machines operated by the laboratory and fulfills the basic file transfer requirements of the network. It is also necessary to allow users to log in on any of the machines from any of the terminals in the facility. We have installed a terminal switching system to meet this need.

The user interface

In order for an experimenter to use the system, it is necessary to provide a hardware, a program and a human interface. The hardware interface is the means by which the experimenter directs signals to the digitizing hardware and thence to the data acquisition computers. The program interface provides a method by which the experimenter can determine what form of processing is to be done on this data. The human interface determines the manner in which an experimenter insteracts with the system to control the operation of programs which process and select data for display.

The hardware interface consists of a U shaped set of racks containing the CAMAC system and its associated front end hardware, along with several NIM bins into which the experimenter plugs such signal shaping and fast logic electronics as may be required. At present there are two program interfaces, the first being a tailored program to be loaded into the LSI-11, and the second being an analysis program in the VAX.

The LSI code is determined mainly by the hardware configuration of the experiment. Code is generated to buffer up an appropriate set of parameters depending on bits set in a coincidence register. We have provided several tailoring options for a user to choose from. The first of these is a tailoring program that takes a skeleton code which understands reasonably regular hardware configurations and creates a prefix file which controls the conditional

assembly code options. These options include the number of ADC's, TDC's and QDC's which must be read for each device, the number of devices which exist, and the definition of a single irregular device. Additionally, it is possible to accumulate singles spectra within the LSI-11, shipping them back to the VAX either on demand or at the end of a run. In the future, we plan to use the LSI-11 to perform initial event rejection.

The second tailoring option is somewhat harder to use, but is far more general. It requires that the user define a set of macros which tell the LSI how to clear devices, how to enable/disable LAM's on devices, and, for each bit in a coincidence register, which devices must be read, and how they are to be read. These macros are then included into a second skeleton program. Defining these macros is made easier by providing the user with fairly complete set of macros that are directed at performing CAMAC operations. These typically free the user from the need to know anything about the LSI-11 machine language.

A word should also be said about scalers and local scaler displays. The LSI-11 programs read several scalers at fixed intervals and send scaler buffers back to the VAX for processing. It is useful during a run to see a display of the total and incremental scaler values as well as a selected set of scaler ratios. The LSI code provides a display of this sort on a local terminal. The display titles and the ratios which are displayed may be defined by the user.

The final operating environment in the VAX is not yet completely defined. It is intended that the user will only have to write a histogramming program or program unit (assuming a suitable one does not yet exist), and that several fairly standard program skeletons would be provided to make this job easier. In addition, we make available a fairly general and quite powerful display program which operates independently from the histogramming program to produce 1D histograms and 2D color density plots on a high resolution color graphics terminal. The program operates on spectra descriptions and spectra stored in a shared data region in the VAX. This program also accepts user commands typed at the terminal to tell it how to present the data. This isolation of display program from histogram program makes the user's program easier to write and debug since obscure errors cannot be introduced into the display logic by accident. Additional graphics presentations created either during or after the run can be displayed on Tektronix 401X compatible terminals. Hardcopy graphics is available either through raster dumps of the Tektronix compatible terminals, or via a Printronix matrix printer. In the future, we plan to be able to produce publication quality graphics on CALCOMP incremental plotters and on a laser printer which

has recently be acquired.

At present, typical user processes acquire CAMAC data, tape it and histogram it. This is dangerous since if the user process fails, event data recording ceases until it can be restarted. We intend to decouple the user histogramming program from the CAMAC and tape I/O by fronting it with an additional program which acquires CAMAC buffers, sends them to tape and forwards them via mailboxes (a VMS internal pseudo device) to the user program. In this case, should the user program fail, event taping could continue uninterrupted. Furthermore, since data buffers can be sent in a replacement mode, where a new buffer overwrites previously unaccepted buffers, the tape process is able to send data to tape limited only by the data rate and the tape speed, rather than by the rate at which data can be gated and histogrammed by the histogramming process. As the disk cluster is brought on line, this buffer routing program may also be used to ship event data to remote CPU's for more time consuming analysis.

Operational Experience and Status

At this time, we have accepted delivery on the bulk of the computing hardware. The analysis, test one data acquisition computer and the VAX 11/780 have been installed, and installation is proceeding on the last of the acquisition machines at the time this is being written. The test machine has been on line for 18 months, while the analysis and first acquisition machine have been available for 3 months. The acquisition system was made available on the test machine in time for the first experiment at NSCL in mid September 1982. Since then, 8-10 experiments have been performed with the system interleaved with beam development work on the K-500.

During this time, the LSI has shown itself to be an easily tailorable system. A user modifiable buffering process was made operational in late March which reduces tremendously the programming load on the facility staff. The VAX has shown itself to be a very reliable computing engine, and several utility programs have been developed to insulate the user sorting programs from the outside world. These programs include a detached process which produces 1D and 2D histogram displays on a high resolution (512 x 512) color graphics terminal, and a master process which runs the user sorting program as a subprocess insulating it from the acquisition of data from the CAMAC system and from event taping.

In pulser timing tests, the system is able to acquire and tape on the order of 20,000 parameters/second. Although in practice, due to the pile up effects of real data, the

system only acquires in the neighborhood of 15,000 parameters/second. The current bottleneck does not appear to be the VAX, since use of the taping front end process ensures that data can go to tape at the speed of the serial highway. The bottleneck appears to be the slow cycle time of the LSI-11, coupled with the conversion times of the digitizers currently in use, which is about 80μs for ORTEC AD-811 ADC's.

Future expansion paths

The need to meet future rate requirements leads us to conclude that the LSI-11 itself should be front ended or replaced with a faster processor. Additionally, ADC's with a faster conversion time could bring us close to acquisition at CAMAC dataway speeds. A problem which crops up with pulsed ion sources, a high peak count rate with low integrated count rates, must also be addressed. The increasing availability of FASTBUS devices will also influence our future planning.

We plan to deal with the LSI speed problem by acquiring a high speed (100-200 nsec cycle time) microprogrammable bit slicer which would increase the rate at which CAMAC data could be made available to the LSI-11 and the VAX. It is possible to for this device to communicate with the VAX via a dual access CAMAC memory which resides on the CAMAC dataway or via DMA to the LSI-11 which would then handle the multibuffered transfers to the VAX.

Our ADC conversion time limitation became quite apparent during recent experiments involving a beam of ^{22}Ne derived from an ion source which was pulsed in an attempt to extend its lifetime. The peak currents of this source were much higher than the time averaged currents, and the duty cycle was such that the system typically could only acquire one or two events per pulse. What this suggests is the use of faster digitizers with front end FIFO buffers to allow the processor to untangle the event stream during the, millisecond or so off times. This would allow the higher peak beam currents to be useful to the experimentalists by spreading the acquisition of the short event bursts over the entire duty cycle of the source.

At this time, it is too early to predict how FASTBUSS will fit into the picture at NSCL, since at this time too few commercially manufactured devices are available, and the manpower resources of the lab are inadequate for the design effort required to develop this hardware in house. The 32-bit structure of this system does imply, however that the latest wave of 16/32 bit microprocessor devices may well play an important role in the front end of the system.

Conclusions

It is clear to us now that the NSCL data acquisition system, while providing users of the facility with the capability to acquire data at moderately high rates (10k to 20k parameters per second) is still in an early stage of development. Additionally, if we hope to cope with some of the high parameter rates projected for some of the future experiments, it is apparent that the front end processing power of the system must be substantially increased, and that this increase must be coupled with the concurrent introduction of faster digitizing devices than are currently used, and possibly the introduction of buffered digitizers to smooth out the duty cycle of pulsed beams. The user LSI-11 interface seems well debugged and is able to present the experimentalist with easily understandable runtime diagnostic information. Each new piece of apparatus brought on line, and each new experiment, will present us with a new set of challenges which must be met.

Acknowledgments

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References and Notes:

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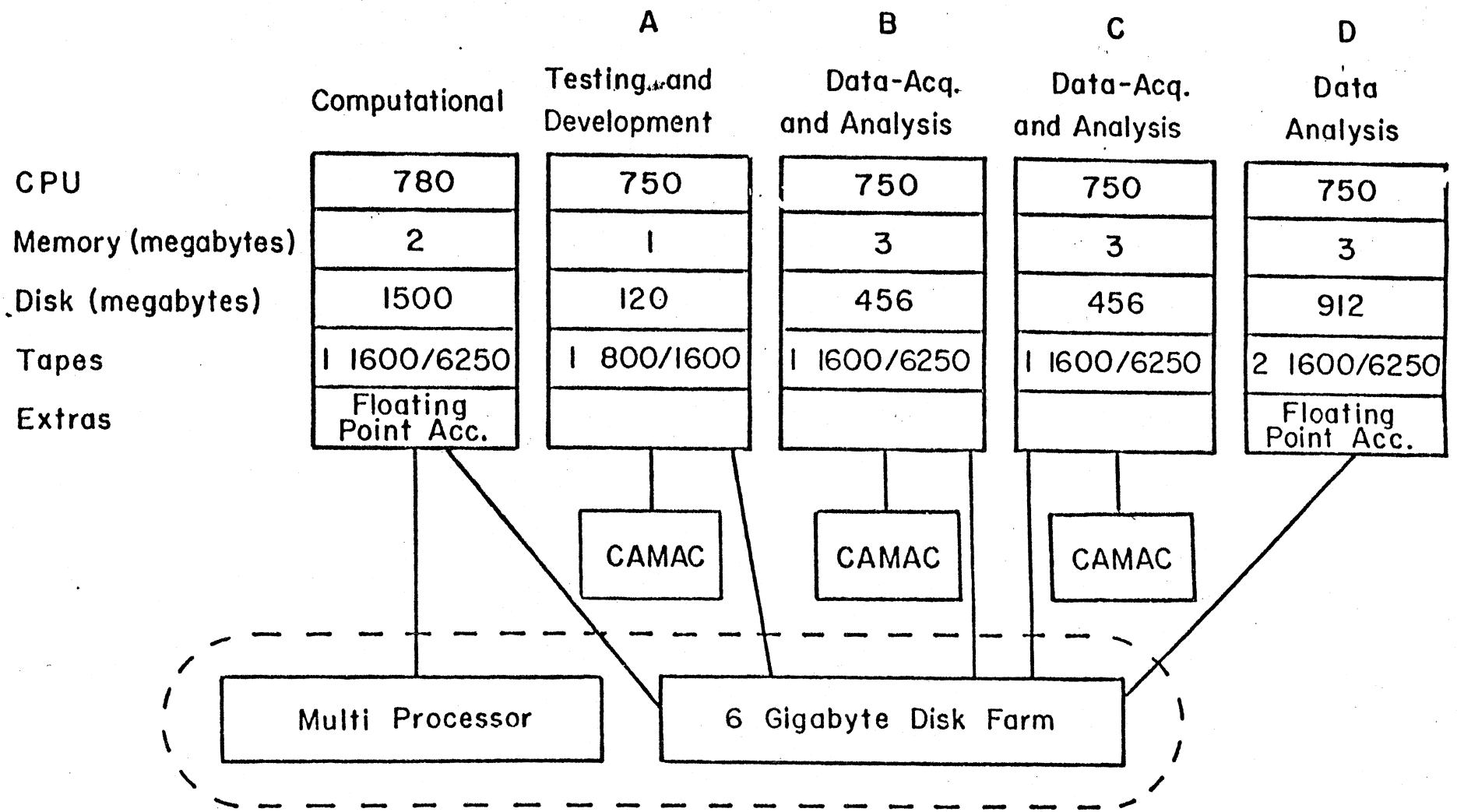
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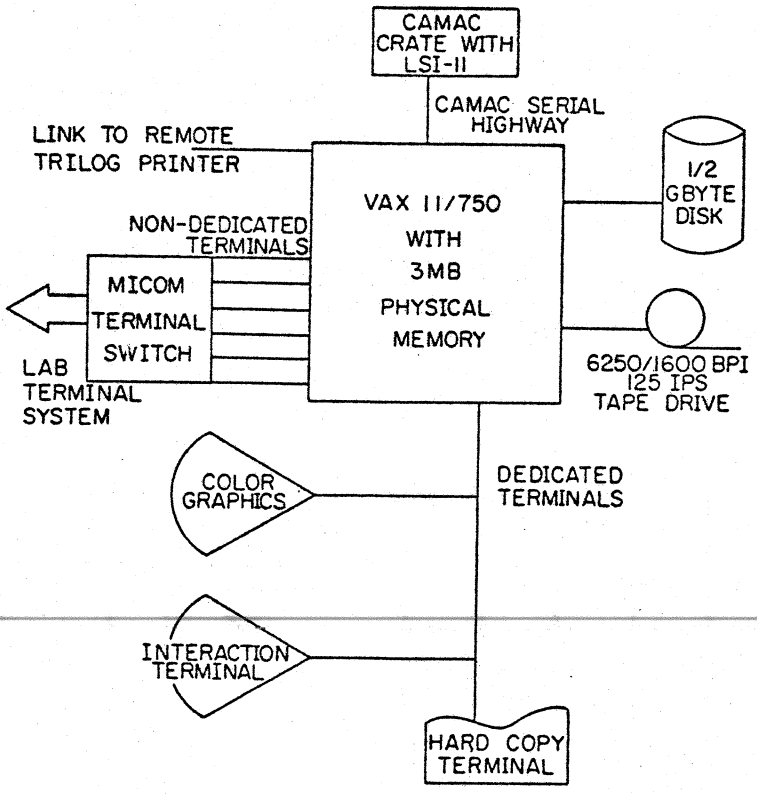
CAMAC CRATE WITH LSI-11
CAMAC SERIAL HIGHWAY
LINK TO REMOTE TRILOG PRINTER
VAX 11/750 WITH 3MB PHYSICAL MEMORY
1/2 GBYTE DISK
NON-DEDICATED TERMINALS
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6250/1600 BPI 125 IPS TAPE DRIVE
COLOR GRAPHICS
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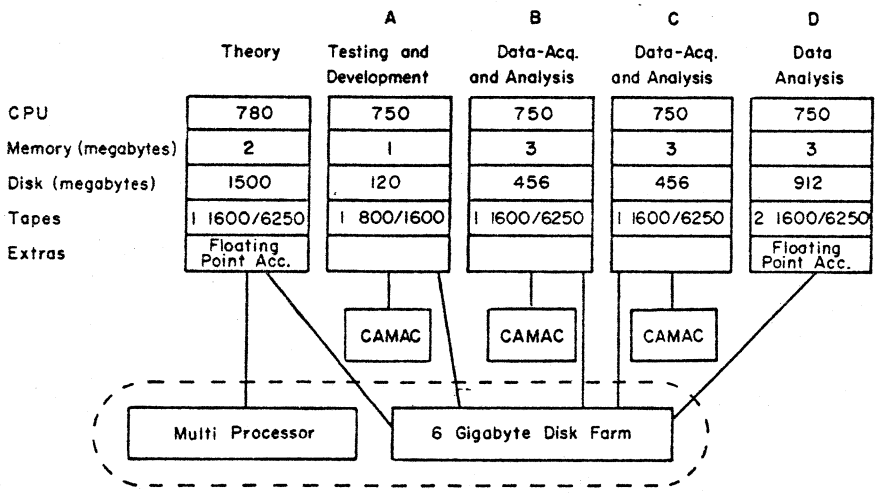
A
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Theory
Testing and Development
Data-Acq. and Analysis
Data-Acq. and Analysis
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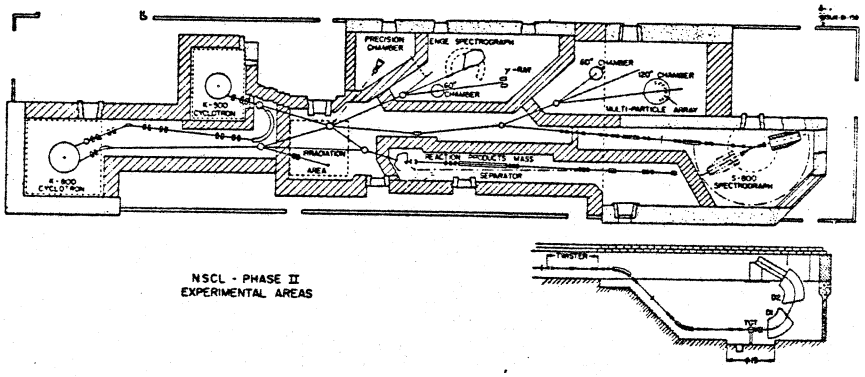

NSCL - PHASE II
EXPERIMENTAL AREAS

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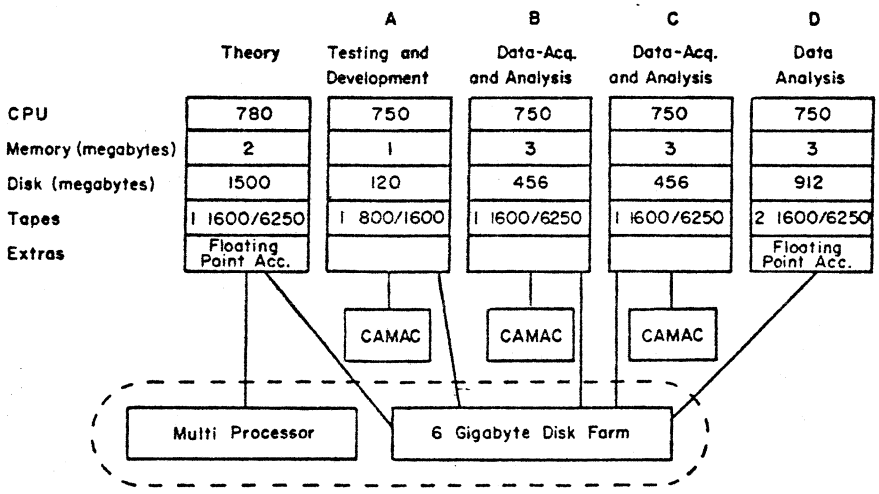
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Theory
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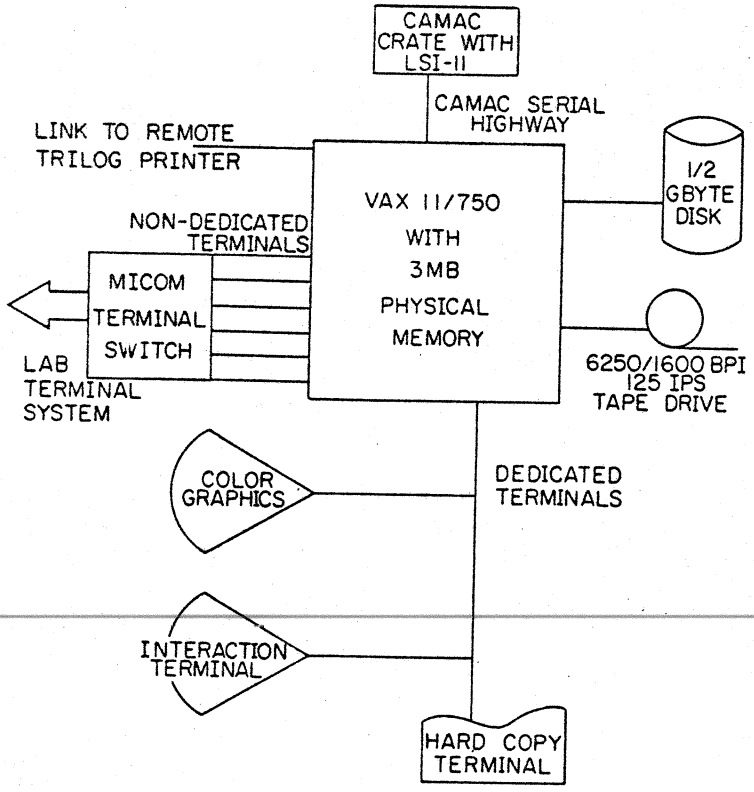
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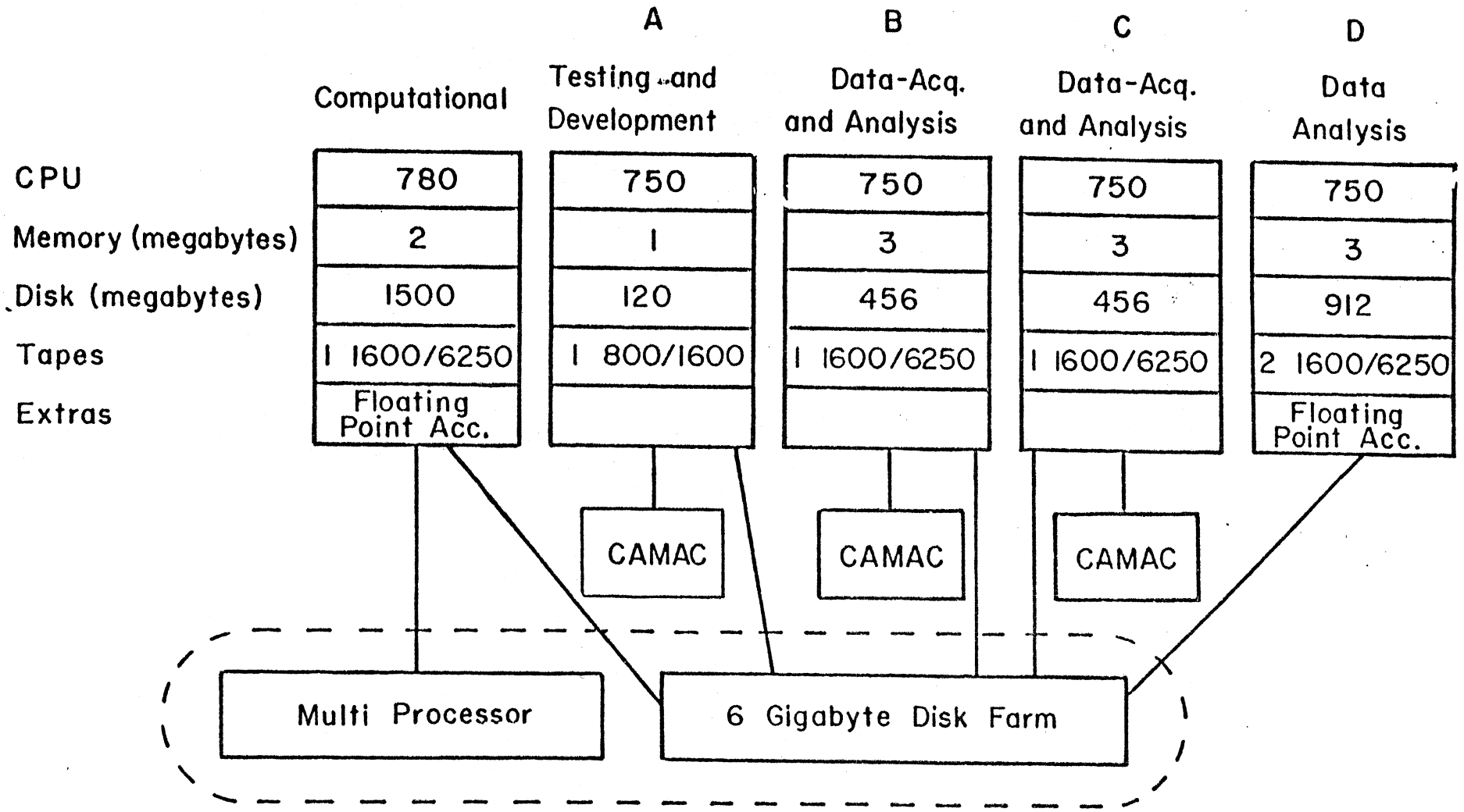
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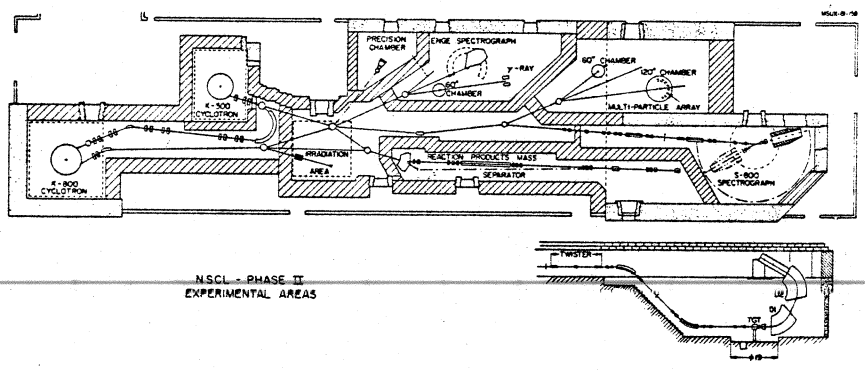

N.S.C.L. - PHASE II
EXPERIMENTAL AREAS