A NEW DIGITAL READOUT SYSTEM FOR GAS DETECTORS

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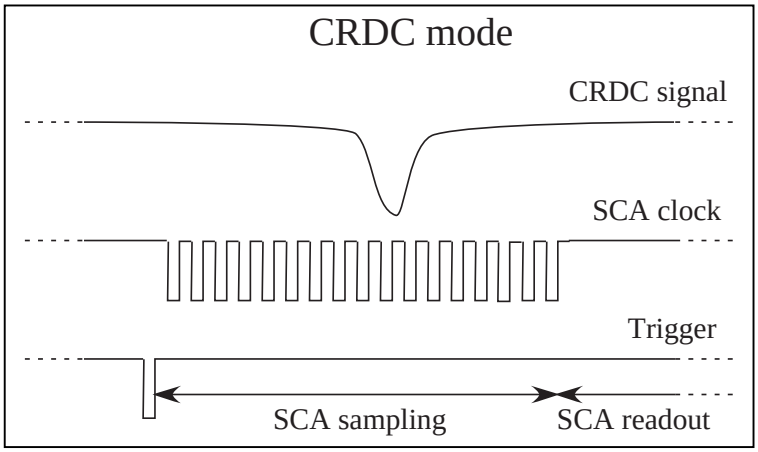
I. Introduction

The Cathode Readout Drift Chambers (CRDC) that measure the positions in the focal plane of the S800, are equipped with Front End Electronics (FEE) designed for the STAR TPC [1]. Each STAR FEE board provides amplification and shaping for 32 channels as well as sample and hold arrays also called Switched Capacitor Arrays (SCA) followed by Analog to Digital Converters (ADC). On the STAR TPC, the SCA samples and stores the signals upon arrival of a valid trigger, and the digitization happens afterwards upon acceptance of the event. In the past, we have disregarded the SCA-ADC part of the board, and extracted the signals directly from the shapers to feed them to FERA Charge to Digital Converters (QDC). While this solution is fast to implement, and worked well for several years, it has a few drawbacks:

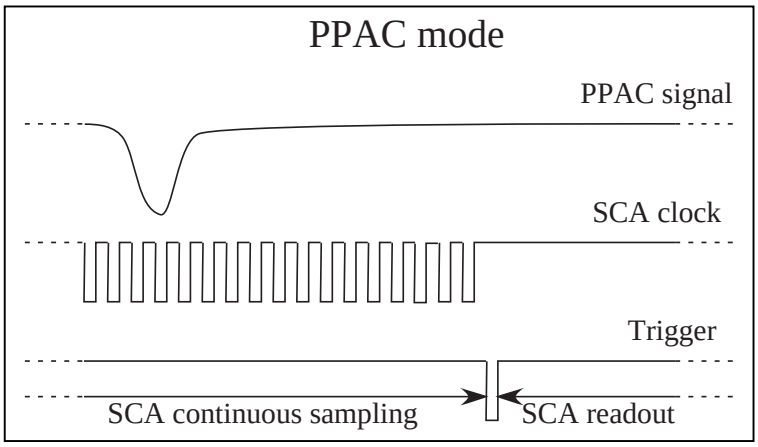
- Necessity to bring all analog signals (448 in the case of the S800) out of the vacuum chamber
- Cost (28 FERA modules are required to digitize the signals from the two S800 CRDC detectors)
- Limited to single hit

These limitations have motivated the modifications described in this article, in which the SCA-ADC installed on the boards are used to store and digitize the signals, and the data is read directly in digital format. In addition to the hardware simplifications, this modification provides greater flexibility on the mode of operation of the detectors. Two modes are implemented so far:

1. For CRDC readout, the SCA starts sampling the signals upon arrival of a valid external trigger. At the same time, a multi-hit Time to Digital Converter (TDC) measures the drift time of the primary electrons from the anode signal of the detector. This drift time is read by the front-end computer and converted into a number of samples, depending on the sampling frequency. The SCA is then scrolled to the corresponding cell, from which the digitization and readout starts until a fixed number of cell have been read, hence creating a sort of digital gate . For experiments where double hits will be detected, this mode can easily be extended to create two gates based on the two hits registered by the multi-hit TDC.



2 . For Parallel Plate Avalanche Counter (PPAC) detectors used for tracking, the mode of operation is quite different. Because this type of detector is fast (about 10ns electron drift time as compared to 10 s for CRDC detectors),



and because valid triggers come typically 1 s later than the signal, these have to be stored in some way while waiting for the trigger. The SCA is an ideal solution to this problem, since it can be used as an analog buffer continuously sampling the signal until a valid trigger occurs. At this point, the sampling stops and the SCA can be scrolled back in time to look at the signal present a fixed amount of time ago. This backwards delay can be adjusted to match the delay between the PPAC signals and the valid trigger, which depends on the flight time of the particles, as well as electronic delays. This mode of operation has the additional advantage of not limiting the dead time of the PPAC itself, which can be run at a high rate (target is up to 10^6 pps) while the trigger rate is much lower. This mode of operation is already being used on the Image2 PPACs of the A1900 fragment separator.

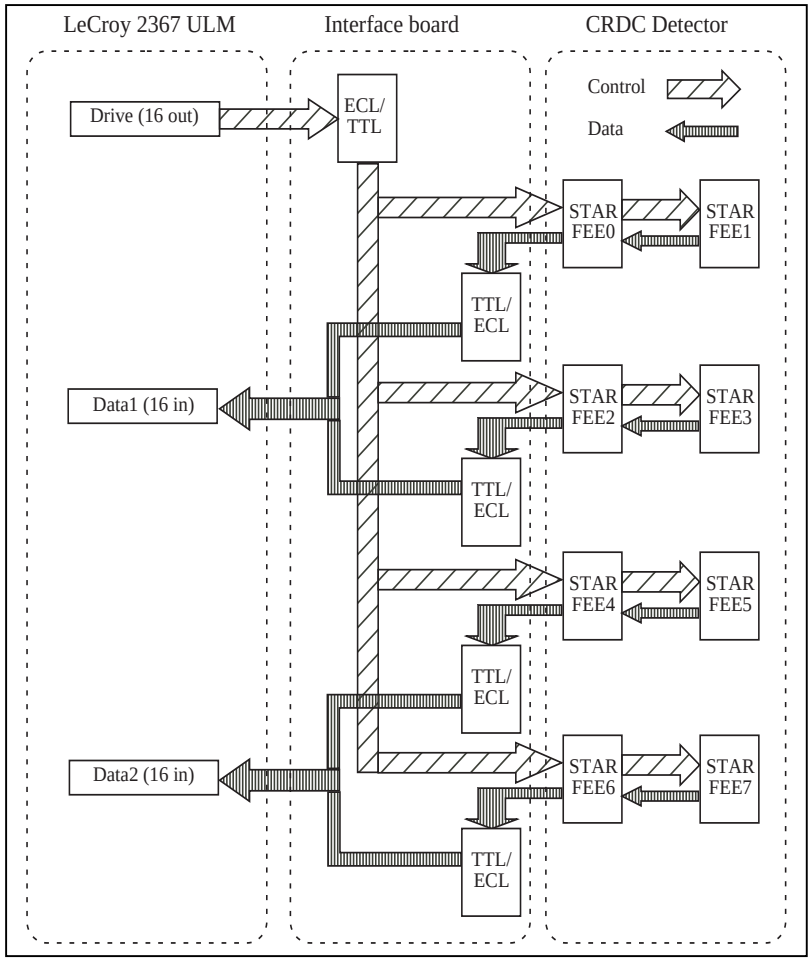
II. Readout

The readout and control of the FEE boards is performed using a LeCroy 2367 Universal Logic Module (ULM) which is composed of 3 elements interfaced with the standard CAMAC bus:

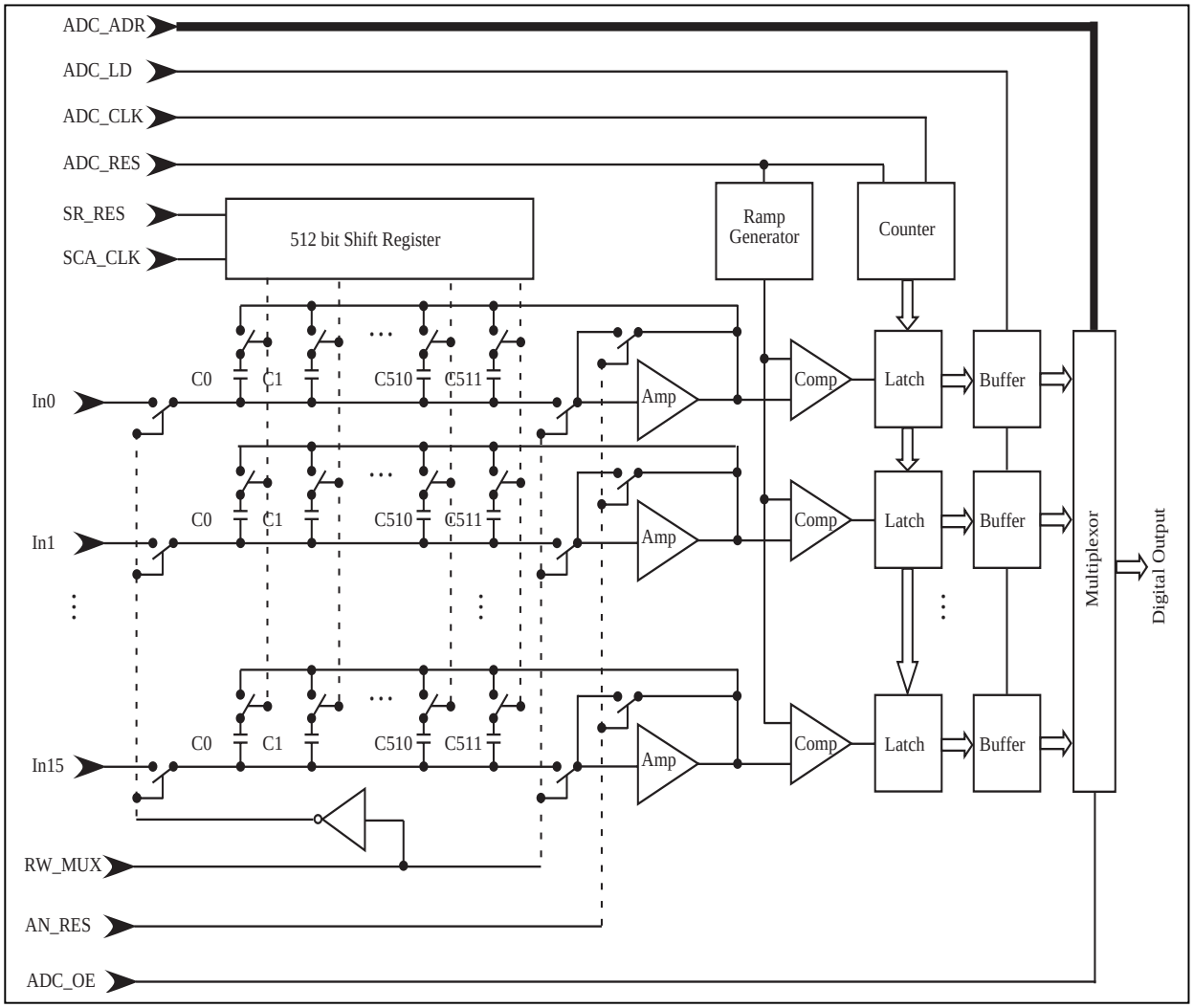
I. A Field Programmable Gate Array (FPGA) programmable via CAMAC

II. 3 Mbytes of static memory

III. A Digital Signal Processor (DSP)



In addition, the module provides 56 external ECL ports which can be configured either as inputs or outputs by groups of 4. The use of a FPGA allows great flexibility in the functionality of the module, as basically any logic circuit can be programmed into the chip, within its size limitation. The drawback is that all functions must implemented by the user, including the CAMAC interface which allows the module to communicate with the external world. The STAR FEE boards require TTL or CMOS logic levels, therefore an interface board has been designed to handle the ECL/TTL and TTL/ECL translations, as well as provide power and parallel readout for up to 8 FEE boards. A simplified schematics of the interface board is shown on the adjacent figure. 16 ECL ports of the ULM are configured as outputs for the FEE control signals, and 32 as inputs for reading the data back. Each FEE generates 8 bit data which are routed together to form a 32 bit data word. This parallel architecture provides a faster readout time than a multiplexed mode in which each FEE would have to be read sequentially. The FEE are grouped by pairs so the total number of channels read in parallel is 64.



The total number of signals necessary to control the FEE boards is 16, one of which used to reset the feedback loop of the preamplifier-shaper chip, and the others used to control the SCA/ADC chip. To better understand the operation of the SCA/ADC, a simplified schematic is shown below.

The SCA part of the circuit is operated by 4 signals, the most important being the RW_MUX which controls the read and write of the capacitor array. During sampling of the inputs, the RW_MUX signal is low and the array is being written by the inputs. During the read sequence, the RW_MUX signal is high to allow the capacitor to be read by the output amplifier. The SCA_CLK and SR_RES signals respectively scroll along the capacitor array and reset the shift register to the first capacitor. They are used during both write and read cycles. The AN_RES signal is used to reset the output amplifiers between each capacitor readout.

The ADC is composed of a ramp generator, a counter and a set of comparators, latches and buffers for each of the 16 channels. This simple architecture allows the digitization of all channels in parallel. A 16 channel multiplexor is then used to read out the data sequentially. Since each FEE board contains 2 of the SCA/ADC chips (for 32 channels), the output enable (ADC_OE) of each SCA/ADC chip is used to select the appropriate bank of 16 channels.

As mentioned earlier, the FEE boards are paired and can be read out sequentially using the CARD_ENA signals for a total of 64 channels. With the present configurations of the FPGA, the time needed to write a single channel is 100ns, therefore a single sample can be written in 6.4 s. The following table lists all the 16 control signals generated by the ULM module as well as their respective functions.

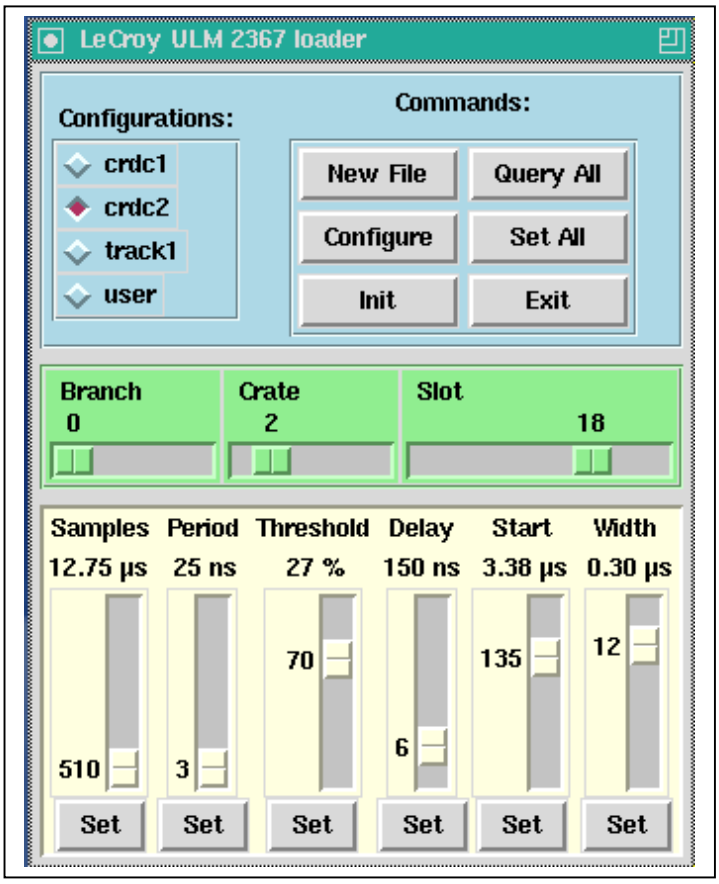
The configurations of the FPGA are designed using a combination of schematics and Verilog language.

Name	Function
RW_MUX	Toggles between write and read of the SCA. Low = write; High = Read
SCA_CLK	Scrolls the SCA shift register. Falling edge = scroll; rising edge = connect
SR_RES	Resets the SCA shift register to the first cell
AN_RES	Reset the SCA buffer amplifier. Active high
ADC_CLK	Clock signal for the ADC counter. Not necessary on FEE Rev. E
ADC_RES	Resets the ADC counter and ramp generator. Active low
ADC_LD	Loads the ADC buffers. Active high
ADC_ADR0	ADC multiplexor address 0. Active low
ADC_ADR1	ADC multiplexor address 1. Active low
ADC_ADR2	ADC multiplexor address 2. Active low
ADC_ADR3	ADC multiplexor address 3. Active low
ADC_OE1	Output enable of the first SCA/ADC chip (channels 1-16)
ADC_OE2	Output enable of the second SCA/ADC chip (channels 17-32)
CARD_ENA1	Card enable first signal
CARD_ENA2	Card enable second signal
SAS_RES	Reset the Preamplifier-shaper chips. Active high

The Verilog language is one of the currently available Hardware Description Languages (HDL) on the market. It was chosen as opposed to VHDL for its greater clarity and ease of use. The design is composed of several modules or macros defined in a highly hierarchy based structure, which makes it easier to debug the functioning of each individual module. The schematic part of the design is used to interconnect the various modules together, as well as define simple logic circuits. The more complex parts of the design are easier defined using the Verilog language, however the user does not have as much control on the final logic circuit since it has to be produced by a synthesis tool. The software used to produce the FPGA configuration files is the Xilinx™ Foundation series. The debugging of a hardware configuration is a rather lengthy process, since the creation of a configuration file involves not only synthesis of the Verilog code, but also placer and router passes which literally wire the circuit on the chip. Once the configuration file has been produced, it has to be downloaded to the FPGA through the CAMAC interface.

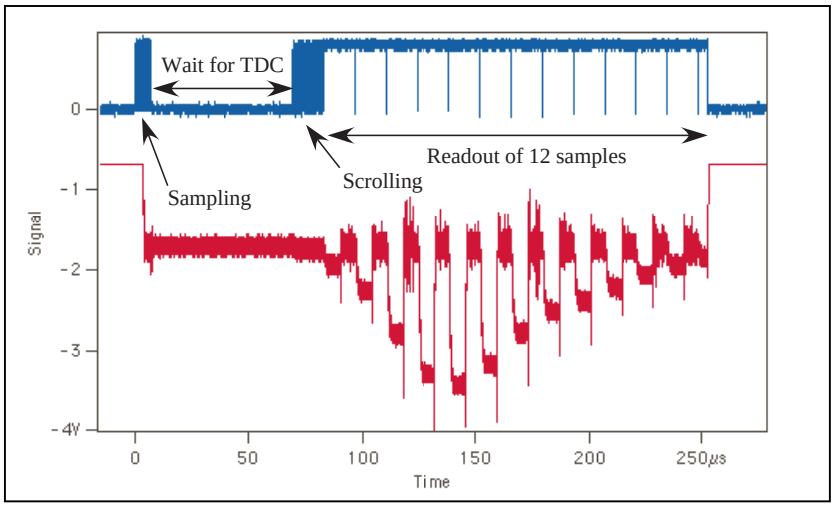
Both PPAC and CRDC configurations use the static memory internal to the ULM module to store the data read out from the FEE boards. The FPGA allow to compare the incoming data to a threshold which can be dynamically modified, and only write to the memory if the data is above the threshold. This reduces greatly the quantity of data, since for a typical event only a few pads are hit only for a few samples, depending on the sampling frequency. The memory can then be read by the readout program using programmed CAMAC functions.

The adjacent figure shows the Tcl/Tk panel used to load and control the configurations on the ULM module. The configuration shown corresponds to the CRDC operation. Several sliders can be used to vary the parameters of the design. The total number of samples, sampling frequency and threshold are adjustable from the leftmost sliders. The delay slider has to be adjusted to match the cable as well as the FEE board internal delays between the control signals going out and the data signals coming back in the FPGA. The start and width correspond to the first sample readout and number of samples read from the SCA. In the crdc2 configuration, the first sample to be read is actually set by the readout program after it has been measured by the multi-hit TDC. The ULM waits until the TDC has finished digitizing the time signal from the CRDC detector, before scrolling to the corresponding cell in the SCA and reading out the samples. This mode of operation is similar to a digital gate implementation.

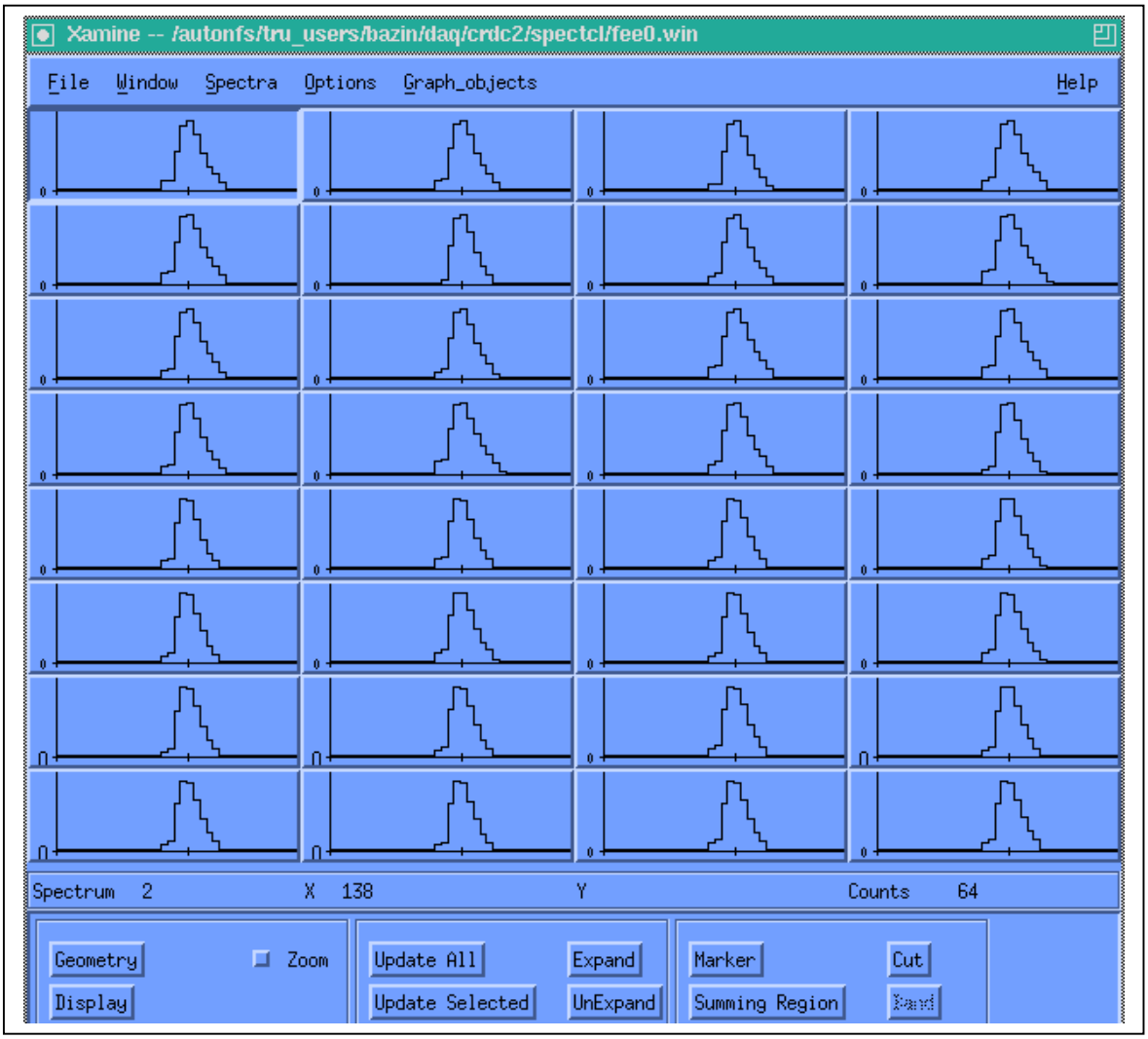


III. Tests

The new readout system has so far been tested with a pulser on the CRDC detectors, and is being used in the A1900 commissioning on the Image2 large PPACs. An example of the whole readout cycle is shown here for a typical CRDC event. The signal shown on top is the SCA_CLK generated by the FPGA. It shows the sampling of the analog signal which occurs in that case in 12.75 s (510 samples of 25ns each), followed by a standby lapse during which the ULM is waiting for the TDC to measure the time from the anode signal of the CRDC, followed then by the scrolling of the SCA up to the first sample of the gate (#135 in that case), and finally ended by the actual readout of 12 samples. The bottom signal shows the output of the SCA during that sequence. The shape of the analog signal which has been stored in the SCA is apparent.



The next figure shows an ensemble of snapshots of the data readout by the acquisition system for one FEE board (32 channels). Only the data above the threshold is read into the data stream, and this threshold has been subtracted from the data. The shape of the pulse recorded on each of the channels can be subsequently processed by either the front-end or back-end computer.



IV. Future

Since the LeCroy ULM module used for this new readout system is being discontinued, a replacement is being designed with better characteristics. This new ULM will be VME based for faster readout of the data written to memory, and it will contain a 900Mflop DSP floating-point processor to allow pre-processing of the data. In many applications, the information contained into the shape of the signals can be treated and reduced in an efficient way using numerical algorithms, hence reducing the CPU load on the front-end and back-end computers, as well as the amount of data put into the data stream. In the case of the CRDC detectors for instance, the basic operations consist of integrating the signals recorded on the pads, and fitting a Gaussian line shape to the obtained pad distribution in order to deduce the centroid as the position where the particle traversed the detector.

V. References

[1] S.R. Klein et al., IEEE Trans. on Nucl. Science, Vol. 43, No. 3, June 1996 (1768-1772)